MT6253 GSM/GPRS Baseband Process Data Sheet

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Specifications are subject to change without notice.

Revision History

Revision	Date	Comments
0.99	May 22, 2009	Initial draft version
0.99 SP1	Jul 30, 2009	Special patch version

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Preface

Acronym for Register Type

R/W	Capable of both read and write access
RO	Read only
RC	Read only. After reading the register bank, each bit which is HIGH(1) will be cleared to LOW(0) automatically.
WO	Write only
W1S	Write only. When writing data bits to register bank, each bit which is HIGH(1) will cause the corresponding bit to be set to 1. Data bits which are LOW(0) has no effect on the corresponding bit.
W1C	Write only. When writing data bits to register bank, each bit which is HIGH(1) will cause the corresponding bit to be cleared to 0. Data bits which are LOW(0) has no effect on the corresponding bit.

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1 System Overview

MT6253 is Mediatek's first monolithic GSM/GPRS handset chip solution which integrates RF, analog baseband, digital baseband as well as Power Management Unit (PMU) and can greatly reduce the component count and make smaller PCB size. Besides, MT6253 is capable of SAIC (Single Antenna Interference Cancellation) and AMR speech. Based on 32 bit ARM7EJ-S™ RISC processor, MT6253 provides an unprecedented platform for high quality modem performance.

The typical application diagram is shown as **Figure 1**.

Platform

MT6253 has the ARM7EJ-S™ RISC processor running up to 104 MHz, thus providing best trade-off between system performance and power consumption.

For large amount of data transfer, high performance DMA (Direct Memory Access) with hardware flow control is implemented, that which greatly enhances the data movement speed while reducing MCU processing load.

Targeted as a modem-centric platform for mobile applications, MT6253 also provides hardware security digital rights management for copyright protection. For further safeguarding, and to protect manufacturer's development investment, hardware flash content protection is also provided to prevent unauthorized porting of software load.

Memory

MT6253 supports up to 3 external state-of-the-art devices through its 16-bit host interface. Devices such as burst mode Flash, SRAM, and Pseudo SRAM are supported. To minimize power consumption and ensure low noise, this interface is designed for flexible I/O voltage and allows lowering of supply voltage down to 1.8V. The driving strength is configurable for signal integrity adjustment. The data bus also employs retention technology to prevent the bus from floating during turn over.

Multi-media

MT6253 utilize high resolution audio DAC, digital audio, and audio synthesis technology to provide superior audio features, e.g. MP3 ring tone.

In order to provide more flexibility and bandwidth for multimedia products, an additional 8/9 bit parallel interface is incorporated. This interface is designed specially for support with Camera companion chip as well as LCD panel. In addition, MT6253 has camera YUV interface that can connect to CMOS sensor of resolution up to VGA. Moreover, it can connect NAND flash device to provide a solution for multimedia data storage. For running multimedia application faster, MT6253 integrates also several hardware-based engines. With hardware based Resizer and advanced display engine, it can display and combine arbitrary size of images with up to 4 blending layers.

Connectivity and Storage

MT6253 supports UART as well as Bluetooth interface. Also, necessary peripheral blocks are embedded for a voice centric phone: Keypad Scanner with the capability to detect multiple key presses, dual SIM Controller, Alerter, Real Time Clock, PWM, Serial LCD Controller, USB 2.0 HS/FS/LS, MMC/SD/MS/MS Pro/SDIO, IrDA and general purpose programmable I/Os.

Audio

Using a highly integrated mixed-signal Audio Front-End architecture of MT6253 allows for easy audio interfacing with direct connection to the audio transducers. The audio interface integrates D/A and A/D Converters for Voice band, as well as high resolution Stereo D/A Converters for Audio band. In addition, MT6253 also

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provides Stereo Input and Analog Mux. MT6253 also supports AMR codec to adaptively optimize speech and audio quality. Moreover, HE-AAC codec is implemented to deliver CD-quality audio at low bit rates.

Also, the 800mW class-D amplifier is also embedded to save the BOM cost of adopting external amplifier.

Radio

MT6253 integrates a mixed-signal Baseband front-end in order to provide a well-organized radio interface with flexibility for efficient customization. It contains gain and offset calibration mechanisms, and filters with programmable coefficients for comprehensive compatibility control on RF modules. MT6253 achieves great MODEM performance by utilizing 14-bit high resolution A/D Converter in the RF downlink path. Furthermore, to reduce the need for extra external current-driving component, the driving strength of some BPI outputs is designed to be configurable.

MT6253 also integrates the RF transceiver for multi-band GSM and GPRS cellular system. In the RF modules in SOC, a high performance quad band differential input LNAs/fully integrated channel filter with f_{3dB}=150kHz receiver is integrated. Also, the transmitter performs integrated TXVCO and loop filter. Furthermore, the frequency synthesizer and Digitally-Controlled Crystal Oscillator (DCXO) are build-in.

Debug Function

The JTAG interface enables in-circuit debugging of software program with the ARM7EJ-S™ core. With this standardized debugging interface, MT6253 provides developers with a wide set of options in choosing ARM development kits from different third party vendors. For security reason, JTAG interface can be disabled by programming internal OTP (one-time programmable) fuse.

Low Power Features

MT6253 offers various low-power features to help reduce system power consumption. These features include Pause Mode of 32KHz clocking at Standby State, Power Down Mode for individual peripherals, and Processor Sleep Mode. In addition, MT6253 are also fabricated in advanced low leakage CMOS process, hence providing an overall ultra low leakage solution.

Power Management

MT6253 integrates all regulators that a voice-centric phone needs. 11 LDOs optimized for Specific GSM/GPRS baseband sub-systems are included. Besides Li-Ion battery charge function, SIM card level shifter interface, two open-drain output switches to control the LED and vibrator are equipped. Other power management schemes such as thermal overload protection, Under Voltage Lock-out Protection (UVLO), over voltage protection and power-on reset and start-up timer are also MT6253 features. Besides, 3 NMOS switches controlling the RGB LEDs are also embedded to reduce BOM count.

Package

The MT6253 device is offered in 11.5mm×11.5mm, 260-ball, 0.47 mm staggered pin pitch, aQFN package

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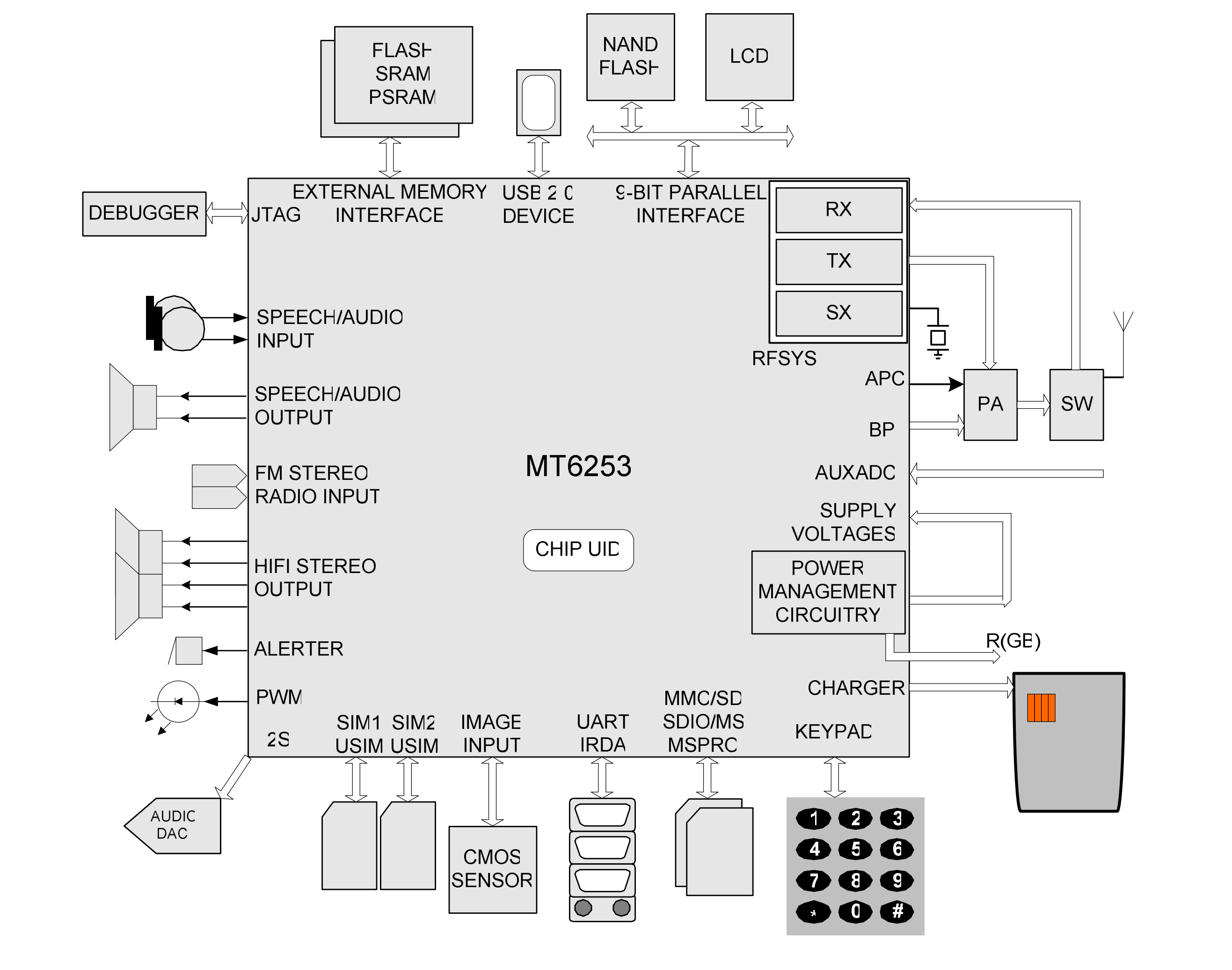

Figure 1 Typical application of MT6253

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1.1 Platform Features

- **General**
  - Integrated voice-band, audio-band and base-band analog front ends
  - aQFN 11.5mm×11.5mm, 260-ball, 0.47 mm pitch package
- **MCU Subsystem**
  - ARM7EJ-S 32-bit RISC processor
  - High performance multi-layer AMBA bus
  - Java hardware acceleration for fast Java-based games and applets
  - Operating frequency: 52/104 MHz
  - Dedicated DMA bus
  - 7 DMA channels
  - 144KB on-chip SRAM
  - On-chip boot ROM for Factory Flash Programming
  - Watchdog timer for system crash recovery
  - 3 sets of General Purpose Timer
  - Circuit Switch Data coprocessor
  - Division coprocessor
- **External Memory Interface**
  - Supports up to 3 external devices
  - Supports 16-bit memory components with maximum size of up to 64M Bytes for each bank
  - Supports Flash and SRAM/PSRAM with Burst Mode
  - Support legacy industry standard parallel LCD Interface
  - Supports multi-media companion chips with 8/16 bits data width
  - Configurable driving strength for memory interface
- **User Interfaces**
  - 6-row × 7-column keypad controller with hardware scanner
  - Supports multiple key presses for gaming
  - SIM/USIM Controller with hardware T=0/T=1 protocol control
  - Real Time Clock (RTC) operating with a separate power supply
  - General Purpose I/Os (GPIOs)
  - 1 set of Pulse Width Modulation (PWM) Output
  - Alerter Output with Enhanced PWM or PDM
  - Maximum 7 external interrupt lines
- **Security**
  - Supports security key and 128 bit chip unique ID
- **Connectivity**
  - 3 sets of UART with hardware flow control and speed up to 921600 bps
  - IrDA modulator/demodulator with hardware framer supports SIR mode of operation
  - HS/FS/LS USB 2.0 Device controller
  - Multi Media Card/Secure Digital Memory Card/Memory Stick/Memory Stick Pro/SDIO host controller

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- Supports SDIO interface for SDIO peripherals as well as WIFI connectivity
- DAI/PCM and I2S interface for Audio application

Low Power Schemes

- Power Down Mode for analog and digital circuits
- Processor Sleep Mode
- Pause Mode of 32KHz clocking at Standby State
- 3-channel Auxiliary 10-bit A/D Converter for application usage other than battery monitoring

Power and Supply Management

- 2.8V to 4.7V Input Range
- Charger Input up to 8V
- 11 sets of LDO Optimized for Specific GSM Sub-systems
- One LDO for RF transceiver
- High Operation Efficiency and Low Stand-by Current
- Li-Ion Battery Charge function
- Dual SIM Card Interface
- One boost regulator and Four Open-Drain Output Current Regulators to Supply/Control the LED
- LDO type Vibrator
- One NMOS switch to control R(GB) LED
- Thermal Overload Protection
- Under Voltage Lock-out Protection
- Over Voltage Protection

Test and Debug

- Built-in digital and analog loop back modes for both Audio and Baseband Front-End
- DAI port complying with GSM Rec.11.10
- JTAG port for debugging embedded MCU

1.2 MODEM Features

Integrated RF Receiver

- Direct conversion architecture
- Quad band differential input LNAs
- Quadrature RF mixers
- Fully integrated channel filter with f_{3dB}=150kHz
- 95 dB gain with 60 dB gain control range
- No IIP2 calibration

Integrated RF Transmitter

- Offset phase lock loop
- IQ modulator DC offset calibration by BB ADC/DAC.
- Precise quadrature by IF divide-by-4.
- Integrated TX VCO
- Integrated loop filter

Integrated RF Frequency Synthesizer

- Programmable fractional-N synthesizer
- Integrated wide range RFVCO
- Integrated loop filter

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- Fast settling time suitable for multi-slot GPRS/EDGE applications

- **Integrated RF Digitally-Controlled Crystal Oscillator (DCXO)**
  - One-pin 26 MHz crystal oscillator
  - On-chip programmable capacitor array for cross tune
  - On-chip programmable capacitor array for fine tune

- **Radio Interface and Baseband Front End**
  - GMSK modulator with analog I and Q channel outputs
  - 10-bit D/A Converter for uplink baseband I and Q signals
  - 14-bit high resolution A/D Converter for downlink baseband I and Q signals
  - Calibration mechanism of offset and gain mismatch for baseband A/D Converter and D/A Converter
  - 10-bit D/A Converter for Automatic Power Control
  - Programmable Radio RX filter with adaptive bandwidth control
  - Dedicated Rx filter for FB acquisition
  - 6-Pin Baseband Parallel Interface (BPI) with programmable driving strength
  - Multi-band support

- **Voice and Modem CODEC**
  - Dial tone generation
  - Voice Memo
  - Noise Reduction
  - Echo Suppression
  - Advanced Sidetone Oscillation Reduction
  - Digital sidetone generator with programmable gain
  - Two programmable acoustic compensation filters
  - GSM/GPRS quad vocoders for adaptive multirate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
  - GPRS GEA1, GEA2 and GEA3 ciphering
  - Programmable GSM/GPRS Modem
  - GSM Circuit Switch Data
  - GPRS Class 12

- **Voice Interface and Voice Front End**
  - Two microphone inputs sharing one low noise amplifier with programmable gain and automatic gain control (AGC) mechanism
  - Voice power amplifier with programmable gain
  - 2nd order Sigma-Delta A/D Converter for voice uplink path
  - D/A Converter for voice downlink path
  - Supports half-duplex hands-free operation
  - Compliant with GSM 03.50

1.3 Multi-Media Features

- **LCD Interface**

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- Dedicated Parallel Interface supports 2 external 8/9 bit Parallel Interface, and Serial interface for LCM

- **LCD Controller**
  - Supports LCM format: RGB332, RGB444, RGB565, RGB666, RGB888
  - Supports LCD module with maximum resolution up to 240x320 at 16bpp
  - Capable of combining display memories with up to 4 blending layers
  - Accelerated Gamma correction with programmable gamma table.
  - Supports hardware display rotation for each layer

- **Audio CODEC**
  - Wavetable synthesis with up to 64 tones
  - Advanced wavetable synthesizer capable of generating simulated stereo
  - Wavetable including GM full set of 128 instruments and 47 sets of percussions
  - PCM Playback and Record
  - Digital Audio Playback

- **Audio Interface and Audio Front End**
  - Supports I2S interface
  - High resolution D/A Converters for Stereo Audio playback
  - Stereo analog input for stereo audio source
  - Analog multiplexer for Stereo Audio
  - FM Radio Recording
  - Stereo to Mono Conversion
  - HE-AAC decode support

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1.4 General Description

Figure 2 details the block diagram of MT6253. Based on a dual-processor architecture, MT6253 integrates both an ARM7EJ-S core and 2 digital signal processor cores. ARM7EJ-S is the main processor that is responsible for running 2G and 2.5G protocol software. Digital signal processors handle the MODEM algorithms as well as advanced audio functions. Except for some mixed-signal circuitries, the other building blocks in MT6253 are connected to either the microcontroller or one of the digital signal processors.

Specifically, MT6253 consist of the following subsystems:

- Highly integrated RF transceiver for multi-band GMS and GPRS cellular systems.
- Microcontroller Unit (MCU) Subsystem - includes an ARM7EJ-S RISC processor and its accompanying memory management and interrupt handling logics.
- Digital Signal Processor (DSP) Subsystem - includes 2 DSP cores and their accompanying memory, memory controller, and interrupt controller.
- MCU/DSP Interface - where the MCU and the DSPs exchange hardware and software information.
- Microcontroller Peripherals - includes all user interface modules and RF control interface modules.
- Microcontroller Coprocessors - runs computing-intensive processes in place of Microcontroller.
- DSP Peripherals - hardware accelerators for GSM/GPRS channel codec.
- Voice Front End - the data path for converting analog speech from and to digital speech.
- Audio Front End - the data path for converting stereo audio from stereo audio source
- Baseband Front End - the data path for converting digital signal from and to analog signal of RF modules.
- Timing Generator - generates the control signals related to the TDMA frame timing.
- Power, Reset and Clock subsystem - manages the power, reset, and clock distribution inside MT6253
- LDOs, Power-on sequences, switches and SIM level shifters.
- Details of the individual subsystems and blocks are described in following Chapters.

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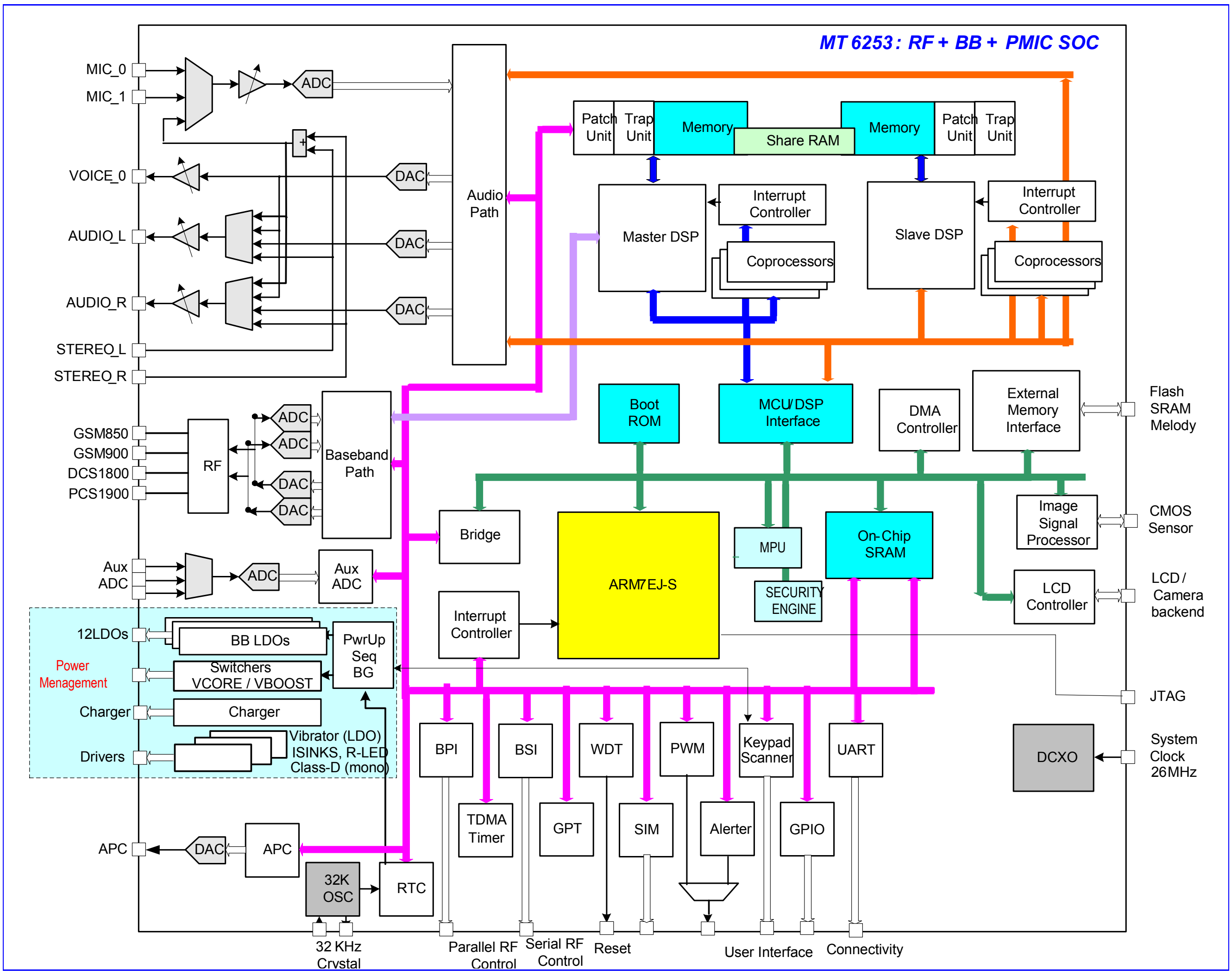

Figure 2 MT6253 block diagram

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2 Product Description

2.1 Pin Outs

One type of package for this product, aQFN 11.5mm * 11.5mm, 260-ball, 0.47mm pitch Package is offered.

Pin-outs and the top view are illustrated in **Figure 3** for this package. Outline and dimension of package is illustrated in **Figure 4**, while the definition of package is shown in **Table 1**.

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
A					XM		ISENSE		BATSNS				BAT_BACK				VSIM				VA														A
B		AU_IN1_P		YP				XP		SIO2		SRST1		VREF		VSIM2		VIO		VM		VRF													B
C	AU_IN1_N		AU_MOUTR		YM		AVDD28_R		BAT_ON		SCLK2		SCLK1		VM_SEL		VCAMD		VBT		VCAMA		GND_RF		TXO_LB		PCS1900N		DCS1800N		GSM900P				C
D		AU_IN0_N		AVDD28_AF		AVDD28_M		AVDD28_PL		AUX_IN1		SRST2		SIO1		VUSB		VBAT_RF		IN		VTCXO		TXO_HB		PCS1900P		DCS1800P		GSM900N		GSM850N			D
E			AU_IN0_P		AU_OUT0_				APC		AUX_IN0		GATEDRV		VBAT_DIGI		VBAT_ANA		QP		VDD28_OP		GND_RF		GND_RF		GND_RF		GND_RF		GSM850P				E
F		VBAT_AMP		AU_FMINR		AU_OUT0_		AU_MOUTL		AUX_IN2		CHRIN		AGND		VBAT_DIGI		QN		IP		VDD28_TX		VDD28_TR		GND_RF		GND_RF		GND_RF		GND_RF			F
G	ISINK2		VBAT_AMP		AU_FMINL																								GND_RF		GND_RF				G
H		ISINK4				AU_VCM																								VDD28_RX		GND_RXIS			H
J	VBL_OUT		SPK1_P		AGND28_AF																										RFVCO_MT		VDD28_RF		J
K		VIBRATOR		SPK1_N		AU_MICBIA																								GND_RFVC		VDD28_SX		XTAL1	K
L			LED		ISINK1																										GND_SX		XTAL2_GN		L
M		VBOOST1		VBOOST1		ISINK3																								VDD28_DC		FREF			M
N	VCORE1		VBAT_SW																												VDD15_RF		BPI_BUS1		N
P		RESETB		PWRKEY																										VDD28_RF		BPI_BUS3		BPI_BUS5	P
R			PAD_VRT		VCORE1_F																								VDD33		BPI_BUS0		EINT1		R
T				AVDD33		AVDD12																								BPI_BUS2		URTS1_B			T
U	XIN		TEST_MOD		DP																								BPI_BUS4		EINT0		CMRST		U
V		XOUT		AVDD_RTC		DM																								UCTS1_B		CMDAT3		CMVREF	V
W			VDDK_1																										CMPCLK		CMPDN		CMDAT7		W
Y		KCOL4		SYSRST_B		PWM																								VDDK_3		CMDAT5			Y
AA	KCOL0		KCOL2		KCOL6																								CMMCLK		CMHREF		CMDAT4		AA
AB		KROW4		KCOL3		KCOL5																								CMDAT6		CMDAT1		CMDAT2	AB
AC			KROW3		KCOL1																								LRSTB		LPCE0B		CMDAT0		AC
AD		KROW1		KROW5		KROW2																								LPA0		LPCE1B			AD
AE	IRDA_PDN		KROW0		SECURITY_																								NLD3		NLD0		LRDB		AE
AF		SRCLKENA		DAIPCMO		DAIRST																								NLD8		NLD5		LWRB	AF
AG			DAICLK		BT_POWE																								NLD6		NLD1		NRNB		AG
AH		DAIPCMIN		SD_PWRE																										NLD4		NREB			AH
AJ	DAISYNC		BT_32K		URXD3		URXD1		JTCK		MCDA1		ECLK		ECS2_B				VDD33_EMI		EUB_B				ED1		ED15		ED13		NLD7		NCEB		AJ
AK		FM_32K		VDD33		EINT3		JTMS		MCDA3		VDDK_2		ERD_B						EWR_B		EA20				ED7		ED0		ED10		NLD2		NCLE	AK
AL			URXD2		JTDO		JTRST_B		MCWP		MCCM0		ECS1_B						EA18		WATCHD		EA23				ED3		ED6		NWEB		NALE		AL
AM		UTXD3		UTXD1		JTDI		VDD33_MS		MCCK		ECS0_B						EA17		ELB_B		EWAIT		EA22		ED9		ED12		ED8					AM
AN			UTXD2		EINT2		MCINS		MCDA2		EADV_B						EA19						EA21		EA16		ED14		ED5		ED2				AN
AP						JRTCK				MCDA0																EA24				ED4		ED11			AP
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	

Figure 3 Top View of MT6253 aQFN 11.5mm * 11.5mm 0.47mm pitch package

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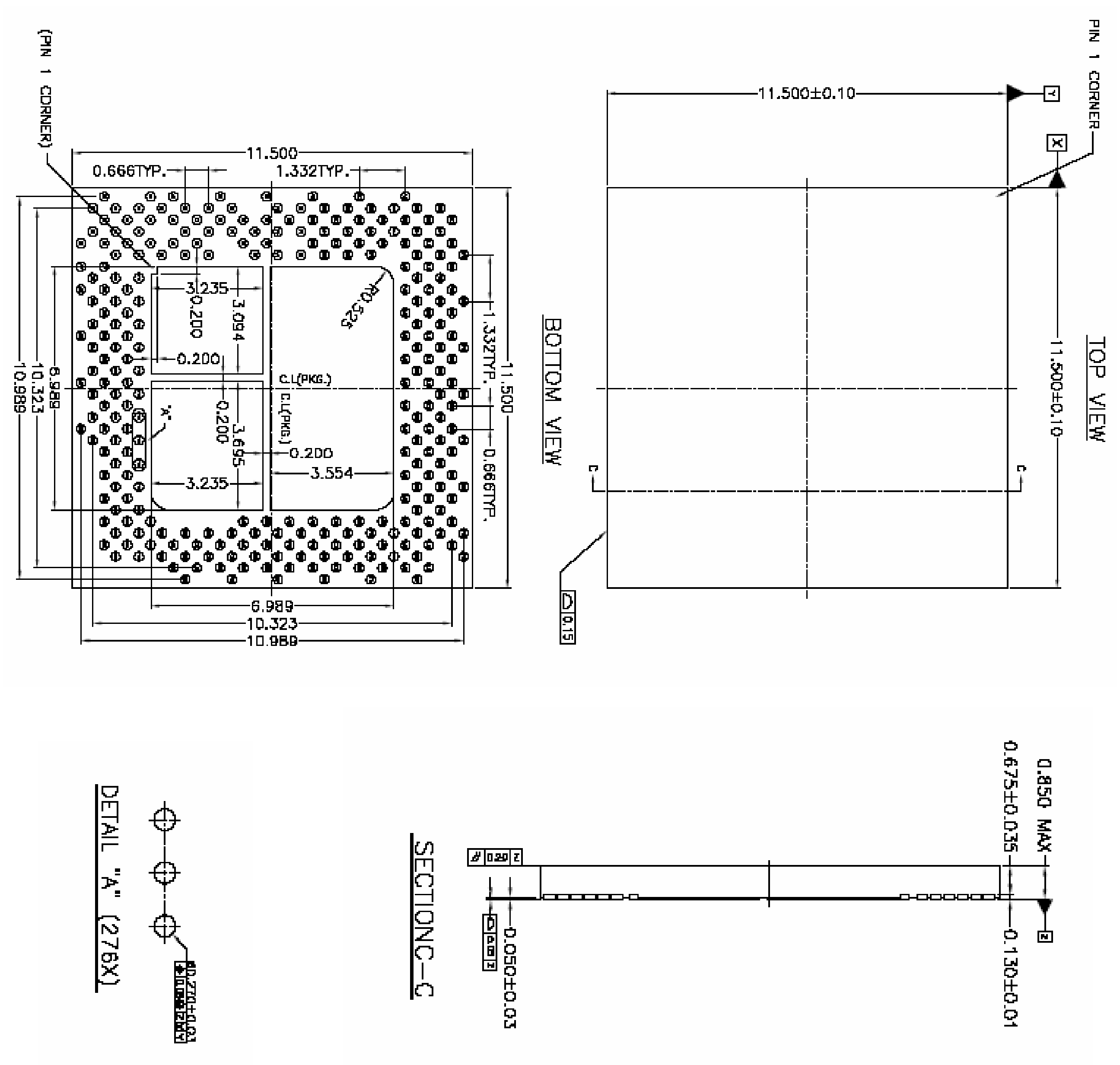

Figure 4 Outlines and Dimension of MT6253 aQFN 11.5mm * 11.5mm 0.47mm pitch package

Body Size	Ball Count	Ball Pitch	Ball Dia.	Package Thk.
11.5 11.5	260	0.47	0.270	0.850

Table 1 Definition of aQFN 11.5mm * 11.5mm 0.47mm pitch package (Unit: mm)

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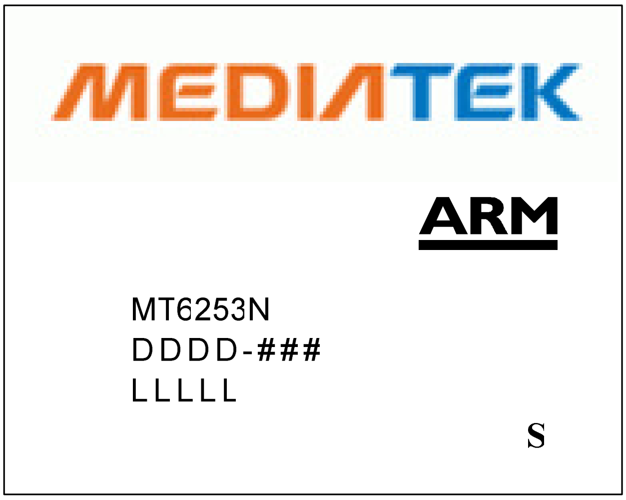
2.2 Top Marking Definition



MT6253N: Part No.
DDDD: Date Code
###: Subcontractor Code
LLLLL: Die Lot No.
S: Special Code

Figure 5 Top Mark of MT6253

2.3 DC Characteristics

2.3.1 Absolute Maximum Ratings

Prolonged exposure to absolute maximum ratings may reduce device reliability. Functional operation at these maximum ratings is not implied.

Item	**Symbol**	**Min**	**Max**	**Unit**
IO power supply	VDD33	-0.3	VDD33+0.3	V
I/O input voltage	VDD33I	-0.3	VDD33+0.3	V
Operating temperature	Topr	-20	80	Celsius
Storage temperature	Tstg	-55	125	Celsius

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2.4 Pin Description

Below pin description is identical for both MT6253, total 260 pins.

aQFN	NAME	Dir	PIN DESCRIPTION	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	PU/PD	Reset
			Analog Baseband Interface (20 pins)						
F8	AU_MOUTL		Audio analog output left channel						
C3	AU_MOUTR		Audio analog output right channel						
F4	AU_FMINR		FM radio analog input right channel						
G5	AU_FMINL		FM radio analog input left channel						
F6	AU_OUT0_N		Earphone 0 amplifier output (-)						
E5	AU_OUT0_P		Earphone 0 amplifier output (+)						
B2	AU_IN1_P		Microphone 1 amplifier input (+)						
C1	AU_IN1_N		Microphone 1 amplifier input (-)						
D2	AU_IN0_N		Microphone 0 amplifier input (+)						
E3	AU_IN0_P		Microphone 0 amplifier input (-)						
E11	AUX_IN0		Auxiliary ADC input 0						
D10	AUX_IN1		Auxiliary ADC input 1						
F10	AUX_IN2		Auxiliary ADC input 2						
E9	APC		Automatic power control DAC output						
B8	XP		Touch panel X-axis positive input						
A5	XM		Touch panel X-axis negative input						
B4	YP		Touch panel Y-axis positive input						
C5	YM		Touch panel Y-axis negative input						
H6	AU_VCM		Clean VCM for reference buffer						
K6	AU_MICBIAS		Microphone bias source P						
			RF Interface (17 pins)						
E31	GSM850P		Differential RF input pad for RX GSM850 band						
D32	GSM850N		Differential RF input pad for RX GSM850 band						
D30	GSM900N		Differential RF input pad for RX GSM900 band						
C31	GSM900P		Differential RF input pad for RX GSM900 band						
D28	DCS1800P		Differential RF input pad for RX DCS1800 band						
C29	DCS1800N		Differential RF input pad for RX DCS1800 band						
C27	PCS1900N		Differential RF input pad for RX PCS1900 band						
D26	PCS1900P		Differential RF input pad for RX PCS1900 band						
C25	TXO_LB		RF output pad for TX LB (GSM900/GSM850)						
D24	TXO_HB		RF output pad for TX HB (DCS/PCS)						
F20	IP		I/O pad for BB analog IQ						
D20	IN		I/O pad for BB analog IQ						

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E19	QP		I/O pad for BB analog IQ						
F18	QN		I/O pad for BB analog IQ						
J31	RFVCO_MT		Monitor pad for RFVCO output						
M32	FREF		Monitor pad for DCXO output						
K34	XTAL1		Input pad for DCXO crystal						
			RF Control Circuitry (6 pins)						
P34	BPI_BUS5	IO	RF hard-wire control bus bit 5	GPIO82	BPI_BUS5				Output
U29	BPI_BUS4	IO	RF hard-wire control bus bit 4	GPIO81	BPI_BUS4				Output
P32	BPI_BUS3	IO	RF hard-wire control bus bit 3						Output
T30	BPI_BUS2	IO	RF hard-wire control bus bit 2						Output
N33	BPI_BUS1	IO	RF hard-wire control bus bit 1						Output
R31	BPI_BUS0	IO	RF hard-wire control bus bit 0						Output
			Digital Audio Interface (5 pins)						
AG3	DAICLK	IO	DAI interface clock output	GPIO15	DAICLK	clko5		PU/PD	Output
AF4	DAIPCMOUT	IO	DAI PCM data output	GPIO16	DAIPCMOUT			PU/PD	Output
AH2	DAIPCMIN	IO	DAI PCM data input	GPIO17		DAIPCMIN	IRDA_PDN	PU/PD	Input
AF6	DAIRST	IO	DAI reset signal input	GPIO18	DAIRST	clko0	IRDA_TX	PU/PD	Input
AJ1	DAISYNC	IO	DAI frame synchronization input	GPIO19	DAISYNC	XADMUX		PU/PD	Input
			PWM Interface (1 pins)						
Y6	PWM	IO	Pulse-width modulated signal	GPIO0	PWM	CLKSQ_SEL	Alerter	PU/PD	Input
			JTAG Interface (6 pins)						
AK8	JTMS	I	JTAG test port mode switch		JTMS			PU	Input
AM6	JTDI	I	JTAG test port data input		JTDI			PU	Input
AJ9	JTCK	I	JTAG test port clock input		JTCK			PU	Input
AL7	JTRST_B	I	JTAG test port reset input		JTRST_B			PD	Input
AP6	JRTCK	IO	JTAG test port returned clock output		JRTCK				Output
AL5	JTDO	IO	JTAG test port data output		JTDO				Output
			Parallel LCD and NAND Interface (21 pins)						
AF30	NLD8	IO	LCM Data Port 8	GPIO40	NLD8	EDICK	RF_AUXOU	PU/PD	Input
AJ31	NLD7	IO	Nand Flash / LCM Data Port 7	GPIO39	NLD7			PU/PD	Input
AG29	NLD6	IO	Nand Flash / LCM Data Port 6	GPIO38	NLD6			PU/PD	Input
AF32	NLD5	IO	Nand Flash / LCM Data Port 5	GPIO37	NLD5			PU/PD	Input
AH30	NLD4	IO	Nand Flash / LCM Data Port 4	GPIO36	NLD4			PU/PD	Input
AE29	NLD3	IO	Nand Flash / LCM Data Port 3	GPIO35	NLD3			PU/PD	Input
AK32	NLD2	IO	Nand Flash / LCM Data Port 2	GPIO34	NLD2			PU/PD	Input
AG31	NLD1	IO	Nand Flash / LCM Data Port 1	GPIO33	NLD1			PU/PD	Input
AE31	NLD0	IO	Nand Flash / LCM Data Port 0	GPIO32	NLD0			PU/PD	Input
AF34	LWRB	IO	Parallel display interface Write Strobe	GPIO41	LWRB			PU/PD	Output
AD30	LPA0	IO	Parallel display interface address output	GPIO42	LPA0		BSI_CLK	PU/PD	Output

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AE33	LRDB	IO	Parallel display interface Read Strobe	GPIO43	LRDB			PU/PD	Output
AC29	LRSTB	IO	Parallel display interface Reset Signal	GPIO44	LRSTB		BSI_EN	PU/PD	Output
AD32	LPCE1B	IO	Parallel display interface chip select 1 output	GPIO46	LPCE1B	NCEB[1]	BSI_DATI	PU/PD	Output
AC31	LPCE0B	IO	Parallel display interface chip select 0 output	GPIO45	LPCE0B		BSI_DATO	PU/PD	Output
AL31	NWEB	IO	NAND Flash Write Enable Output	GPIO28	NWEB			PU/PD	Output
AL33	NALE	IO	NAND Flash Address Latch Enable Output	GPIO29	NALE			PU/PD	Output
AK34	NCLE	IO	NAND Flash Command Latch Enable Output	GPIO30	NCLE			PU/PD	Output
AJ33	NCEB	IO	NAND Flash Chip Enable Output	GPIO26	NCEB[0]			PU/PD	Output
AH32	NREB	IO	NAND Flash Read Enable Output	GPIO27	NREB			PU/PD	Output
AG33	NRNB	IO	NAND Flash Read/Busy Status Input	GPIO31	NRNB			PU/PD	Input
			External Memory Interface (35 pins)						
AN11	EADV_B	IO	External memory address valid, active low						Output
AK14	ERD_B	IO	External memory read strobe, active low						Output
AK20	EWR_B	IO	External memory write strobe, active low						Output
AM20	ELB_B	IO	External memory lower byte strobe						Output
AJ21	EUB_B	IO	External memory upper byte strobe						Output
AM12	ECS0_B	IO	External memory chip select 0						Output
AL13	ECS1_B	IO	External memory chip select 1						Output
AJ15	ECS2_B	IO	External memory chip select 2	GPIO14	ECS2_B	MFIQ		PU/PD	Output
AJ13	ECLK	IO	Flash, PSRAM and CellularRAM clock						Output
AN25	EA16	IO	External memory address bus 16						Output
AM18	EA17	IO	External memory address bus 17						Output
AL19	EA18	IO	External memory address bus 18						Output
AN17	EA19	IO	External memory address bus 19						Output
AK22	EA20	IO	External memory address bus 20						Output
AN23	EA21	IO	External memory address bus 21						Output
AM24	EA22	IO	External memory address bus 22						Output
AL23	EA23	IO	External memory address bus 23						Output
AP26	EA24	IO	External memory address bus 24						Output
AK28	ED0	IO	External memory data bus 0						Output
AJ25	ED1	IO	External memory data bus 1						Output
AN31	ED2	IO	External memory data bus 2						Output
AL27	ED3	IO	External memory data bus 3						Output
AP30	ED4	IO	External memory data bus 4						Output
AN29	ED5	IO	External memory data bus 5						Output
AL29	ED6	IO	External memory data bus 6						Output
AK26	ED7	IO	External memory data bus 7						Output
AM30	ED8	IO	External memory data bus 8						Output
AM26	ED9	IO	External memory data bus 9						Output
AK30	ED10	IO	External memory data bus 10						Output

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AP32	ED11	IO	External memory data bus 11						Output
AM28	ED12	IO	External memory data bus 12						Output
AJ29	ED13	IO	External memory data bus 13						Output
AN27	ED14	IO	External memory data bus 14						Output
AJ27	ED15	IO	External memory data bus 15						Output
AM22	EWAIT	IO	Flash, PSRAM and CellularRAM data ready						Output
			Keypad Interface (13 pins)						
AA5	KCOL6	IO	Keypad column 6	GPIO1	KCOL6	EINT4		PU/PD	Input
AB6	KCOL5	IO	Keypad column 5	GPIO2	KCOL5			PU/PD	Input
Y2	KCOL4	IO	Keypad column 4	GPIO3	KCOL4	clko1		PU/PD	Input
AB4	KCOL3	IO	Keypad column 3	GPIO4	KCOL3			PU/PD	Input
AA3	KCOL2	IO	Keypad column 2	GPIO5	KCOL2			PU/PD	Input
AC5	KCOL1	IO	Keypad column 1	GPIO6	KCOL1			PU/PD	Input
AA1	KCOL0	IO	Keypad column 0	GPIO7	KCOL0			PU/PD	Input
AD4	KROW5	IO	Keypad row 5	GPIO8	KROW5	EINT5		PU/PD	Output
AB2	KROW4	IO	Keypad row 4	GPIO9	KROW4		SRCLKENA	PU/PD	Output
AC3	KROW3	IO	Keypad row 3	GPIO10	KROW3			PU/PD	Output
AD6	KROW2	IO	Keypad row 2	GPIO11	KROW2			PU/PD	Output
AD2	KROW1	IO	Keypad row 1	GPIO12	KROW1			PU/PD	Output
AE3	KROW0	IO	Keypad row 0	GPIO13	KROW0			PU/PD	Output
			Sensor Interface (14 pins)						
AC33	CMDAT0	IO	CMOS sensor data input 0	GPIO47	CMDAT0			PU/PD	Input
AB32	CMDAT1	IO	CMOS sensor data input 1	GPIO48	CMDAT1			PU/PD	Input
AB34	CMDAT2	IO	CMOS sensor data input 2	GPIO49	CMDAT2			PU/PD	Input
V32	CMDAT3	IO	CMOS sensor data input 3	GPIO50	CMDAT3			PU/PD	Input
AA33	CMDAT4	IO	CMOS sensor data input 4	GPIO51	CMDAT4			PU/PD	Input
Y32	CMDAT5	IO	CMOS sensor data input 5	GPIO52	CMDAT5			PU/PD	Input
AB30	CMDAT6	IO	CMOS sensor data input 6	GPIO53	CMDAT6			PU/PD	Input
W33	CMDAT7	IO	CMOS sensor data input 7	GPIO54	CMDAT7			PU/PD	Input
AA31	CMHREF	IO	CMOS sensor horizontal reference signal input	GPIO55	CMHREF			PU/PD	Input
AA29	CMMCLK	IO	CMOS sensor master clock output	GPIO58	CMMCLK			PU/PD	Input
V34	CMVREF	IO	CMOS sensor vertical reference signal input	GPIO56	CMVREF			PU/PD	Input
U33	CMRST	IO	CMOS sensor reset signal output	GPIO60	CMRST			PU/PD	Input
W31	CMPDN	IO	CMOS sensor power down control	GPIO57	CMPDN			PU/PD	Input
W29	CMPCLK	IO	CMOS sensor pixel clock input	GPIO59	CMPCLK			PU/PD	Input
			MSDC Interface (8 pins)						
AP10	MCDA0	IO	SD Serial Data IO 0/Memory Stick Serial Data IO	GPIO71	MCDA0			PU/PD	Input
AJ11	MCDA1	IO	SD Serial Data IO 1	GPIO70	MCDA1			PU/PD	Input
AN9	MCDA2	IO	SD Serial Data IO 2	GPIO69	MCDA2			PU/PD	Input
AK10	MCDA3	IO	SD Serial Data IO 3	GPIO68	MCDA3			PU/PD	Input

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AN7	MCINS	IO	SD Card Detect Input	GPIO65	MCINS			PU/PD	Input
AL9	MCWP	IO	SD Write Protect Input	GPIO66	MCWP			PU/PD	Input
AM10	MCCK	IO	SD Serial Clock/Memory Stick Serial Clock	GPIO67	MCCK			PU/PD	Output
AL11	MCCM0	IO	SD Command Output/Memory Stick Bus State Output		MCCM0			PD	Output
			External Interrupt Inputs (4 pins)						
AK6	EINT3	IO	External interrupt 3	GPIO61	EINT3	clko4		PU/PD	Input
AN5	EINT2	IO	External interrupt 2	GPIO62	EINT2	MIRQ	clko3	PU/PD	Input
R33	EINT1	IO	External interrupt 1	GPIO63	EINT1			PU/PD	Input
U31	EINT0	IO	External interrupt 0	GPIO64	EINT0			PU/PD	Input
			UART and IRDA Interface (9 pins)						
AJ5	URXD3	IO	UART3 receive data	GPIO20	URXD3	UCTS2_B		PU/PD	Input
AM2	UTXD3	IO	UART3 transmit data	GPIO21	UTXD3	URTS2_B		PU/PD	Output
AL3	URXD2	IO	UART2 receive data	GPIO22	URXD2	LCD_TE	IRDA_RX	PU/PD	Input
AN3	UTXD2	IO	UART2 transmit data	GPIO23	UTXD2	EDIDAT	IRDA_TX	PU/PD	Output
AJ7	URXD1	IO	UART1 receive data		URXD1			PU	Input
AM4	UTXD1	IO	UART1 transmit data		UTXD1			PU	Output
T32	URTS1_B	IO	UART1 request to send, active low	GPIO25	URTS1_B	CAM_SDA		PU/PD	Output
V30	UCTS1_B	IO	UART1 clear to send, active low	GPIO24	UCTS1_B	CAM_SCL		PU/PD	Input
AE1	IRDA_PDN	IO	IRDA power down	GPIO76	IRDA_PDN	EINT6	EDIWS	PU/PD	Input
			SIM Card Interface (6 pins)						
D14	SIO1		SIM Data Input / Outputs						
B12	SRST1		SIM card reset output						
C13	SCLK1		SIM card clock output						
B10	SIO2		SIM 2 Data Input / Outputs						
D12	SRST2		SIM 2 card reset output						
C11	SCLK2		SIM 2 card clock output						
			Charger and LED Driving Interface (9 pins)						
E13	GATEDRV		External PFET gate driver. Control charge current.						
F12	CHRIN		Charger input						
J1	VBL_OUT		Regulated output for backlight						
K2	VIBRATOR		Vibrator driving output						
L3	LED		Keypad LED driver input						
L5	ISINK1		Current sink1 for B/L LED						
M6	ISINK3		Current sink3 for B/L LED						
G1	ISINK2		Current sink2 for B/L LED						
H2	ISINK4		Current sink4 for B/L LED						
			LDO Outputs (11 pins)						
D22	VTCXO		Crystal or VCTCXO LDO output						
B22	VRF		RF LDO output						

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C21	VCAMA		Camera module analog/io power						
A21	VA		Analog LDO output						
B20	VM		External memory LDO output						
C19	VBT		BT power (MT6601/MT6611)						
B18	VIO		Digital I/O voltage LDO output						
C17	VCAMD		Camera module core/io power						
D16	VUSB		USB power						
A17	VSIM		LDO output to SIM card						
B16	VSIM2		LDO output to SIM 2 card						
			PMIC Miscellaneous (21 pins)						
D18	VBAT_RF		RF used battery voltage input						
E17	VBAT_Analog								
E15	VBAT_Digital								
F16	VBAT_Digital								
B14	VREF		Reference voltage for PMIC						
A13	BAT_BACKUP		Backup battery for RTC						
A9	BATSNS		Battery sense input						
A7	ISENSE		Current sense input						
C15	VM_SEL		Memory supply voltage level select input						
C9	BAT_ON		Battery insertion test						
P4	PWRKEY		Power key press input (low active)						
P2	RESETB		Power on reset (low active)						
M2	VBOOST1_SW		Switch pin of boost converter						
M4	VBOOST1								
N3	VBAT_SWREG								
N1	VCORE1								
R5	VCORE1_FB								
F2	VBAT_AMP								
G3	VBAT_AMP								
J3	SPK1_P		Speaker positive output						
K4	SPK1_N		Speaker negative output						
			System Miscellaneous (11 pins)						
U3	TEST_MODE	IO	Factory test mode enable input						
AL21	WATCHDOG	IO	Watchdog reset output, active low					PD	Output
U1	XIN		32.768 KHz crystal input						
V2	XOUT		32.768 KHz crystal output						
Y4	SYSRST_B	I	System reset input active low					PU	Input
AE5	SECURITY_EN	I	Security Enable						Input
AF2	SRCLKENAI	IO	26MHz Clock Enable	GPIO77	SRCLKENAI			PU/PD	Input
AG5	BT_POWEN	IO	Bluetooth Power Enable	GPIO72				PU/PD	Input

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AH4	SD_PWREN	IO	SD Power Enable	GPIO73				PU/PD	Input
AJ3	BT_32K	IO	Bluetooth 32KHz clk	GPIO74	clko6		SRCLKENA	PU/PD	Input
AK2	FM_32K	IO	FM 32KHz clk	GPIO75			clko2	PU/PD	Input
			USB Interface (3 pins)						
R3	PAD_VRT								
U5	DP								
V6	DM								
			Digital Power (7 pins)						
W3	VDDK_1								
AK12	VDDK_2								
Y30	VDDK_3								
AK4	VDD33								
R29	VDD33								
AM8	VDD33_MSDC								
AJ19	VDD33_EMI		Supply voltage of external memory interface						
			Analog Power and Ground (33 pins)						
J5	AGND28_AFE		AFE AGND (clean reference ground)						
T6	AVDD12		1.2V for USB digital						
T4	AVDD33		3.3V for USB analog						
V4	AVDD_RTC		Supply voltage of real time clock circuitry						
P30	VDD28_RFD		VDD28 pad for digital block						
N31	VDD15_RFD		VDD15 pad for SDM and 3-wire						
L33	XTAL2_GND		Ground pad for DCXO output buffer						
M30	VDD28_DCXO								
L31	GND_SX		Ground pad for SX MMD						
K32	VDD28_SX		VDD28 pad for SX CP/PFD/MMD circuits						
J33	VDD28_RFVCO		VDD28 pad for SX RFVCO circuit						
K30	GND_RFVCO		Ground pad for RFVCO circuit						
H32	GND_RXISO							—	
H30	VDD28_RXFE								
F24	VDD28_TRXIF		VDD28 pad for RX IF circuit						
F22	VDD28_TXVCO		VDD28 pad for TXVCO					—	
E21	VDD28_OPLL		VDD28 pad for TX OPLL PFD/CP/APD/MMD						
F14	AGND								
D8	AVDD28_PLL								
C7	AVDD28_RFE								
D6	AVDD28_MBUF		Audio buffer AVDD						
D4	AVDD28_AFE		AFE AVDD						
C23	GND_RF		RF ground						
E23	GND_RF		RF ground						

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E25	GND_RF		RF ground						
F26	GND_RF		RF ground						
E27	GND_RF		RF ground						
F28	GND_RF		RF ground						
E29	GND_RF		RF ground						
G29	GND_RF		RF ground						
F30	GND_RF		RF ground						
G31	GND_RF		RF ground						
F32	GND_RF		RF ground						

Table 2 Pin Descriptions

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3 Micro-Controller Unit Subsystem

Figure 6 illustrates the block diagram of the Micro-Controller Unit Subsystem in MT6253. The subsystem utilizes a main 32-bit ARM7EJ-S RISC processor, which plays the role of the main bus master controlling the whole subsystem. All processor transactions go to code cache first. The code cache controller accesses TCM (128KB memory dedicated to ARM7EJS core), cache memory, or bus according to the processor's request address. If the requested content is found in TCM or in cache, no bus transaction is required. If the code cache hit rate is high enough, bus traffic can be effectively reduced and processor core performance maximized. In addition to the benefits of reuse of memory contents, code cache also has a MPU (Memory Protection Unit), which allows cacheable and protection settings of predefined regions. The contents of code cache are only accessible to MCU, and only MCU instructions are kept in the cache memory (thus the name "code" cache).

The bus comprises of two-level system buses: Advanced High-Performance Bus (AHB) and Advanced Peripheral Bus (APB). All bus transactions originate from bus masters, while slaves can only respond to requests from bus masters. Before data transfer can be established, the bus master must ask for bus ownership, accomplished by request-grant handshaking protocol between masters and arbiters.

Two levels of bus hierarchy are designed to provide optimum usage for different performance requirements. Specifically, AHB Bus, the main system bus, is tailored toward high-speed requirements and provides 32-bit data path with multiplex scheme for bus interconnections. The APB Bus, on the other hand, is designed to reduce interface complexity for lower data transfer rate, and so it is isolated from high bandwidth AHB Bus by APB Bridge. APB Bus supports 16-bit addressing and both 16-bit and 32-bit data paths. APB Bus is also optimized for minimal power consumption by turning off the clock when there is no APB bus activity.

During operation, if the target slave is located on AHB Bus, the transaction is conducted directly on AHB Bus. However, if the target slave is a peripheral and is attached to the APB bus, then the transaction is conducted between AHB and APB bus through the use of APB Bridge.

The MT6253 MCU subsystem supports only memory addressing method. Therefore all components are mapped onto the MCU 32-bit address space. A Memory Management Unit is employed to allow for a central decode scheme. The MMU generates appropriate selection signals for each memory-addressed module on the AHB Bus.

In order to off-load the processor core, a DMA Controller is designated to act as a master and share the bus resources on AHB Bus to do fast data movement between modules. This controller comprises thirteen DMA channels.

The Interrupt Controller provides a software interface to manipulate interrupt events. It can handle up to 32 interrupt sources asserted at the same time. In general, it generates 2 levels of interrupt requests, FIQ and IRQ, to the processor.

A 128K Byte SRAM is provided for acting as system memory for high-speed data access. For factory programming purpose, a Boot ROM module is used. These two modules use the same Internal Memory Controller to connect to AHB Bus.

External Memory Interface supports both 8-bit and 16-bit devices. Since AHB Bus is 32-bit wide, all the data transfer will be converted into several 8-bit or 16-bit cycles depending on the data width of target device. Note that, this interface is

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specific to both synchronous and asynchronous components, like Flash, SRAM and parallel LCD. This interface supports also burst mode type of Flash.

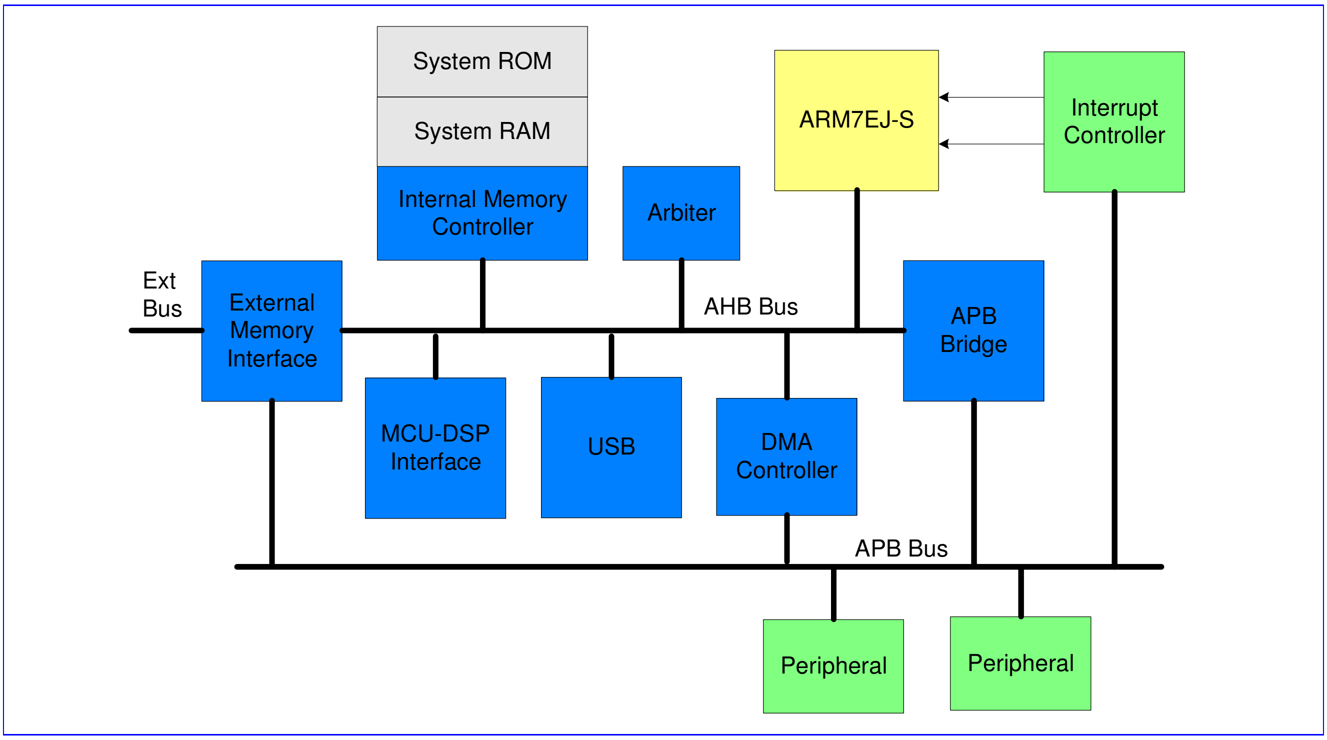

Figure 6 Block Diagram of the Micro-Controller Unit Subsystem in MT6253

3.1 Processor Core

3.1.1 General Description

The Micro-Controller Unit Subsystem in MT6253 is built up with a 32-bit RISC core, ARM7EJ-S that is based on Von Neumann architecture with a single 32-bit data bus carrying both instructions and data. The memory interface of ARM7EJ-S is totally compliant to AMBA based bus system. Basically, it can be connected to AHB Bus directly.

3.2 Memory Management

3.2.1 General Description

The processor core of MT6253, ARM7EJ-S, supports only memory addressing method for instruction fetch and data access. It manages a 32-bit address space that has addressing capability up to 4GB. System RAM, System ROM, Registers, MCU Peripherals and external components are all mapped onto such 32-bit address space, as depicted in **Figure 7**.

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MCU 32-bit Addressing Space			
	Reserved		
A3FF_FFFh | A300_0000h	DSP IDMA2		
A2FF_FFFh | A200_0000h	DSP IDMA1		
A1FF_FFFh | A100_0000h	MCU-DSP Share RAM2		
A0FF_FFFh | A000_0000h	MCU-DSP Share RAM1		
9FFF_FFFh | 9000_0000h	9800_0000h	Reserved	
	9000_0000h	LCD	
8FFF_FFFFh | 8000_0000h	APB Peripherals		
7FFF_FFFFh | 7000_0000h	7800_0000h	Virtual FIFO	
	7000_0000h	USB	
5FFF_FFFFh | 5000_0000h	TCM		
4FFF_FFFFh | 4000_0000h	Internal Memory		
3FFF_FFFFh | 0000_0000h	External Memroy		EA[25:0] Addressing Space

Figure 7 The Memory Layout of MT6253

The address space is organized as basis of blocks with size of 256M Bytes for each. Memory blocks MB0-MB12 are determined and currently dedicated to specific functions, as shown in **Table 3**, while the others are reserved for future usage. Essentially, the block number is uniquely selected by address line A31-A28 of internal system bus.

Memory Block	Block Address A31-A28	Address Range	Description
MB0	0h	00000000h-07FFFFFFh	Boot Code, EXT SRAM or EXT Flash/MISC
		08000000h-0FFFFFFFh	EXT SRAM or EXT Flash/MISC
MB1	1h	10000000h-17FFFFFFh	EXT SRAM or EXT Flash/MISC
		18000000h-1FFFFFFFh	EXT SRAM or EXT Flash/MISC

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MB2	2h	20000000h-27FFFFFFh	EXT SRAM or EXT Flash/MISC
		28000000h-2FFFFFFFh	EXT SRAM or EXT Flash/MISC
MB3	3h	30000000h-37FFFFFFh	EXT SRAM or EXT Flash/MISC
		38000000h-3FFFFFFFh	EXT SRAM or EXT Flash/MISC
MB4	4h	40000000h-47FFFFFFh	System RAM
		48000000h-4FFFFFFFh	System ROM
MB5	5h	50000000h-5FFFFFFFh	TCM
MB6	7h	70000000h-77FFFFFFh	USB
		78000000h-7FFFFFFFh	Virtual FIFO
MB7	8h	80000000h-8FFFFFFFh	APB Slaves
MB8	9h	90000000h-97FFFFFFh	LCD
		98000000h-9FFFFFFFh	Reserved
MB9	Ah	A0000000h-A0FFFFFFh	MCU-DSP Share RAM1
MB10	Ah	A1FFFFFFh-A1000000h	MCU-DSP Share RAM2
MB11	Ah	A2FFFFFFh-A2000000h	DSP IDMA1
MB12	Ah	A3FFFFFFh-A3000000h	DSP IDMA2

Table 3 Definitions of Memory Blocks in MT6253

3.2.1.1 External Access

To have external access, the MT6253 outputs 25 bits (A25-A1) of address lines along with 3 selection signals that correspond to associated memory blocks. That is, MT6253 can support at most 3 MCU addressable external components. The data width of internal system bus is fixed as 32-bit wide, while the data width of the external components is fixed as 16 bit.

Since devices are usually available with variety operating grades, adaptive configurations for different applications are needed. MT6253 provides software programmable registers to configure to adapt operating conditions in terms of different wait-states.

3.2.1.2 Memory Re-mapping Mechanism

To permit system being configured with more flexible, a memory re-mapping mechanism is provided. It allows software program to swap BANK0 (ECS0#) and BANK1 (ECS1#) dynamically. Whenever the bit value of RM0 in register EMI_REMAP is changed, these two banks will be swapped accordingly. Besides, it also permits system being boot in different sequence as detailed in 3.2.1.3 Boot Sequence.

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3.2.1.3 Boot Sequence

Since the ARM7EJ-S core always starts to fetch instructions from the lowest memory address at 00000000h after system has been reset, the system is designed to have a dynamic mapping architecture capable of associating Boot Code, external Flash or external SRAM with the memory block 0000_0000h – 07ff_ffffh.

By default, the Boot Code is mapped onto 0000_0000h – 07ff_ffffh after a system reset. In this special boot mode, External Memory Controller does not access external memory; instead, the EMI Controller send predefined Boot Code back to the ARM7EJS-S core, which instructs the processor to execute the program in System ROM. This configuration can be changed by programming bit value of RM1 in register EMI_REMAP directly.

MT6253 system provides one boot up scheme:

- Start up system of running codes from Boot Code for factory programming or NAND flash boot.

3.2.1.3.1 Boot Code

The Boot Code is placed together with Memory Re-Mapping Mechanism in External Memory Controller, and comprises of just two words of instructions as shown below. A jump instruction leads the processor to run the code starting at address 48000000h where the System ROM is placed.

```
ADDRESS        BINARY CODE      ASSEMBLY
00000000h      E51FF004h        LDR  PC, 0x4
00000004h      48000000h        (DATA)
```

3.2.1.3.2 Factory Programming

The configuration for factory programming is shown in **Figure 8**. Usually the Factory Programming Host connects with MT6253 by way of UART interface. To have it works properly, the system should boot up from Boot Code. That is the IBOOT should be tied to GND. The down load speed can be up to 921K bps while MCU is running at 26MHz.

After system being reset, the Boot Code will guide the processor to run the Factory Programming software placed in System ROM. Then, MT6253 will start and continue to poll the UART1 port until valid information is detected. The first information received on the UART1 will be used to configure the chip for factory programming. The Flash down loader program is then transferred into System RAM or external SRAM.

Further information will be detailed in MT6253 Software Programming Specification.

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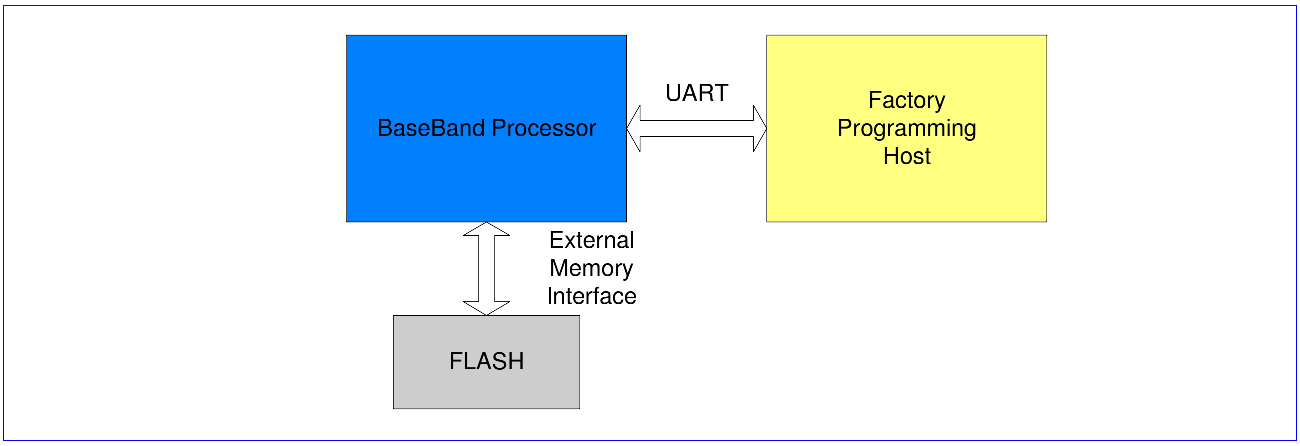

Figure 8 System configuration required for factory programming

3.2.1.3.3 NAND Flash Booting

If MT6253 cannot receive data from UART1 for a certain amount of time, the program in System ROM checks if any valid boot loader exists in NAND flash. If found, the boot loader code is copied from NAND flash to RAM (internal or external) and executed to start the real application software. If no valid boot loader can be found in NAND flash, MT6253 starts executing code in EMI bank0 memory. The whole boot sequence is shown in the following figure.

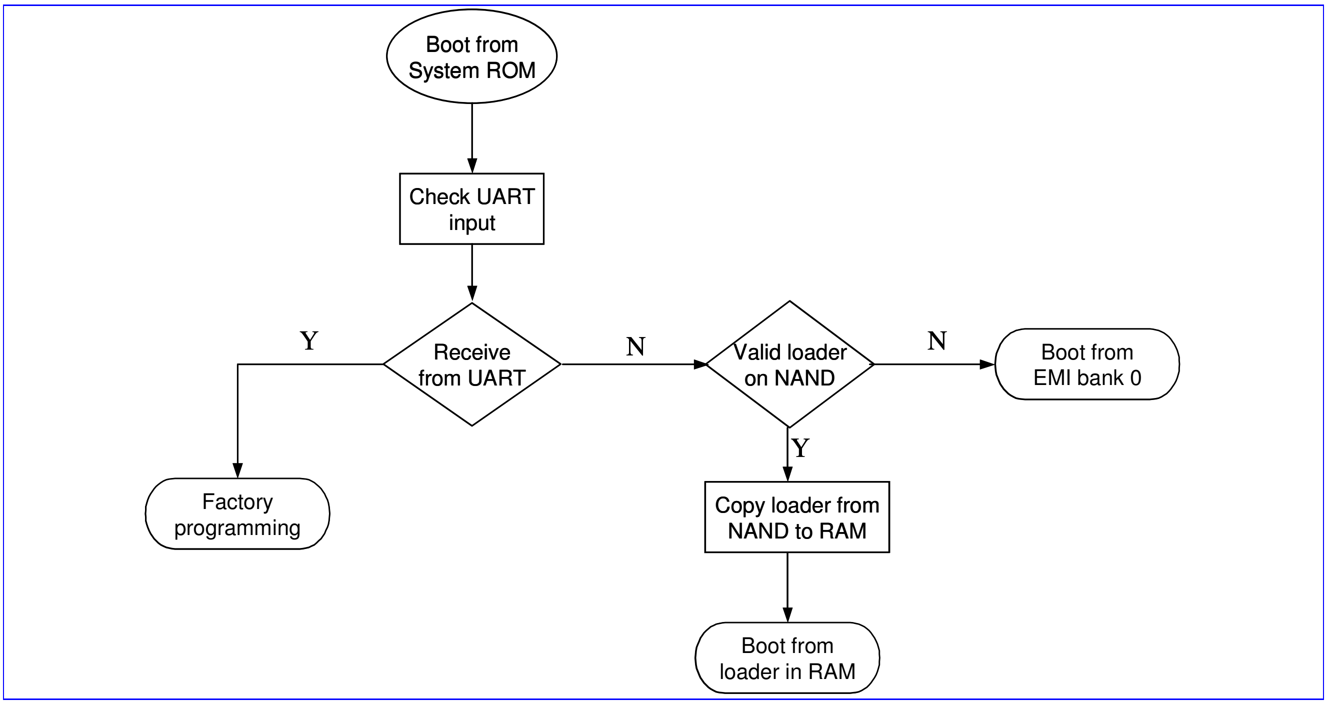

Figure 9 Boot sequence

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3.2.1.4 Little Endian Mode

The MT6253 system always treats 32-bit words of memory in Little Endian format. In Little Endian mode, the lowest numbered byte in a word is stored in the least significant byte, and the highest numbered byte in the most significant position. Byte 0 of the memory system is therefore connected to data lines 7 through 0.

3.3 Bus System

3.3.1 General Description

Two levels of bus hierarchy are employed in constructing the Micro-Controller Unit Subsystem of MT6253. As depicted in **Figure 6**, AHB Bus and APB Bus serve for system backbone and peripheral buses, while an APB bridge connects these two buses. Both AHB and APB Buses operate at the same clock rate as processor core.

The APB Bridge is the only bus master resided on the APB bus. All APB slaves are mapped onto memory block MB8 in MCU 32-bit addressing space. A central address decoder is implemented inside the bridge to generate those select signals for individual peripheral. In addition, since the base address of each APB slave has been associated with select signals, the address bus on APB will contains only the value of offset address.

The maximum address space that can be allocated to a single APB slave is 64KB, i.e. 16-bit address lines. The width of data bus is mainly constrained to 16-bit to minimize the design complexity and power consumption while some of them uses 32-bit data bus to accommodate more bandwidth. In the case where an APB slave needs large amount of transfers, the device driver can also request a DMA resource or channel to conduct a burst of data transfer. The base address and data width of each peripheral are listed in **Table 4**.

Base Address	Description	Data Width	Software Base ID
8000_0000h	Efuse controller	32	EFUSE Base
8001_0000h	Configuration Registers (Clock, Power Down, Version and Reset)	16	CONFG Base
8002_0000h	General Purpose Inputs/Outputs	16	GPIO Base
8003_0000h	Reset Generation Unit	16	RGU Base
8100_0000h	External Memory Interface	32	EMI Base
8101_0000h	Interrupt Controller	32	CIRQ Base
8102_0000h	DMA Controller	32	DMA Base
8103_0000h	UART 1	16	UART1 Base
8104_0000h	UART 2	16	UART2 Base
8105_0000h	UART 3	16	UART3 Base
8106_0000h	General Purpose Timer	16	GPT Base
8107_0000h	Alerter Interface	16	ALTER Base
8108_0000h	Keypad Scanner	16	KP Base

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8109_0000h	Pulse-Width Modulation Outputs	16	PWM Base
810A_0000h	SIM Interface	16	SIM Base
810B_0000h			
810C_0000h	Real Time Clock	16	RTC Base
810D_0000h	Security Engine for JTAG protection	32	SEJ Base
810E_0000h	Software Debug	16	SWDBG Base
810F_0000h	IrDA	16	IRDA Base
8110_0000h	I2C	16	I2C Base
8111_0000h	MS/SD Controller	32	MSDC Base
8112_0000h	NAND Flash Interface	32	NFI base
8113_0000h	SIM2 Interface	16	SIM2 Base
8200_0000h	TDMA Timer	32	TDMA Base
8201_0000h	Base-Band Serial Interface	32	BSI Base
8202_0000h	Base-Band Parallel Interface	16	BPI Base
8204_0000h	Automatic Power Control Unit	32	APC Base
8205_0000h	Auxiliary ADC Unit	16	AUXADC Base
8206_0000h	Divider/Modulus Coprocessor	32	DIVIDER Base
8207_0000h	Frame Check Sequence	16	FCS Base
8208_0000h	GPRS Cipher Unit	32	GCU Base
8209_0000h	CSD Format Conversion Coprocessor	32	CSD_ACC Base
820A_0000h	MCU-DSP Shared 1 Register	16	SHARE Base
820B_0000h	IRDBG1	16	IRDBG Base
820C_0000h	MCU-DSP Shared 2 Register	16	SHARE2 Base
820D_0000h	IRDBG 2	16	IRDBG2 Base
820E_0000h	DSP Patch Unit	16	PATCH Base
820F_0000h	Audio Front End	16	AFE Base
8210_0000h	Base-Band Front End	16	BFE Base
8300_0000h			
8301_0000h	Analog Chip Interface Controller	16	MIXED Base
8400_0000h	GMC Controller		GMC Base
8401_0000h	Resizer	32	RESZ Base
8402_0000h	Camera	32	CAM Base

Table 4 Register Base Addresses for MCU Peripherals

REGISTER ADDRESS	REGISTER NAME	SYNONYM
0x8001_0000h	Hardware Version Register	HW_VER

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0x8001_0004h	Software Version Register	SW_VER
0x8001_0008h	Hardware Code Register	HW_CODE
0x8001_0404h	APB Bus Control Register	APB_CON
0x8001_0710h	Layer 2 AHB Bus Control Register	LYR2_BUS_OPTION
0x8001_0714h	Arbitration 1T enable	ARB_1T_EN

Table 5 APB Bridge Register Map

3.3.2 Register Definitions

0x8001_0404h APB Bus Control Register APB_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		APBW6		APBW4	APBW3	APBW2	APBW1	APBW0		APBR6		APBR4	APBR3	APBR2	APBR1	APBR0
Type		R/W		R/W	R/W	R/W	R/W	R/W		R/W		R/W	R/W	R/W	R/W	R/W
Reset		0		0	0	0	0	0		1		1	1	1	1	1

This register is used to control the timing of Read Cycle and Write Cycle on APB Bus. Note that APB Bridge 5 is different from other bridges. The access time is varied, and access is not completed until acknowledge signal from APB slave is asserted.

APBR0-APBR6 Read Access Time on APB Bus

- **0** 1-Cycle Access
- **1** 2-Cycle Access

APBW0-APBW6 Write Access Time on APB Bus

- **0** 1-Cycle Access
- **1** 2-Cycle Access

0x8001_0710h AHB Bus Control Register LYR2_BUS_OPTION

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LYR2_ULTRA_ONLY	LYR2_ULTRA_EN8	LYR2_ULTRA_EN7	LYR2_ULTRA_EN6	LYR2_ULTRA_EN5	LYR2_ULTRA_EN4	LYR2_ULTRA_EN3	LYR2_ULTRA_EN2	LYR2_ULTRA_EN1	LYR2_ULTRA_EN0
Type		R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0		0	0	0	0	0	0	0	0	0	0	0	0	0

LYR2_ULTRA_EN0-LYR2_ULTRA_EN8 The 9 bits are used to control the ultra high ability of each master on layer2.

LYR2_ULTRA_EN[8:0] = {USB, IRDBG2, IRDBG1, WAVE, IR, DMA, VPORT, LCD, GMC}

- **0** the master has normal priority
- **1** the master has ultra high priority

LYR2_ULTRA_ONLY This register is used to control if normal priority master's request can join into arbitration when there is an ultra high request exist.

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0 Can't join

1 Can join

0x8001_0714h Arbitration 1T Enable ARB_1T_EN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WRAP_DIS	EMI_SPPED_104MHZ	EMI_SPPED_52MHZ	EMI_SPPED_13MHZ												ARB_1T_EN
Type	RO	RO	RO	RO												R/W
Reset	1	0	0	1												0

ARB_1T_EN This register is used to control the AHB bus arbiter to using hreq or hreq_lat to join arbitration. Using hreq directly will gain 1T better performance.

0 Using hreq_lat

1 Using hreq

EMI_SPEED_104MHz Indicate the EMI runs at 104MHz, useful for DCM latency before new EMI setting can apply

0 not 104MHz

1 104MHz

EMI_SPEED_52MHz Indicate the EMI runs at 52MHz, useful for DCM latency before new EMI setting can apply

0 not 52MHz

1 52MHz

EMI_SPEED_13MHz Indicate the EMI runs at 13MHz, useful for DCM latency before new EMI setting can apply

0 not 13MHz

1 13MHz

WRAP_DIS Indicate the MCU/BUS clock ratio is whether 1:1 or 2:1

0 1:2

1 1:1

3.4 Direct Memory Access

3.4.1 General Description

A generic DMA Controller is placed on Layer 2 AHB Bus to support fast data transfers and to off-load the processor. With this controller, specific devices on AHB or APB buses can benefit greatly from quick completion of data movement from or to memory modules such as Internal System RAM or External SRAM. Such Generic DMA Controller can also be used to connect any two devices other than memory module as long as they can be addressed in memory space.

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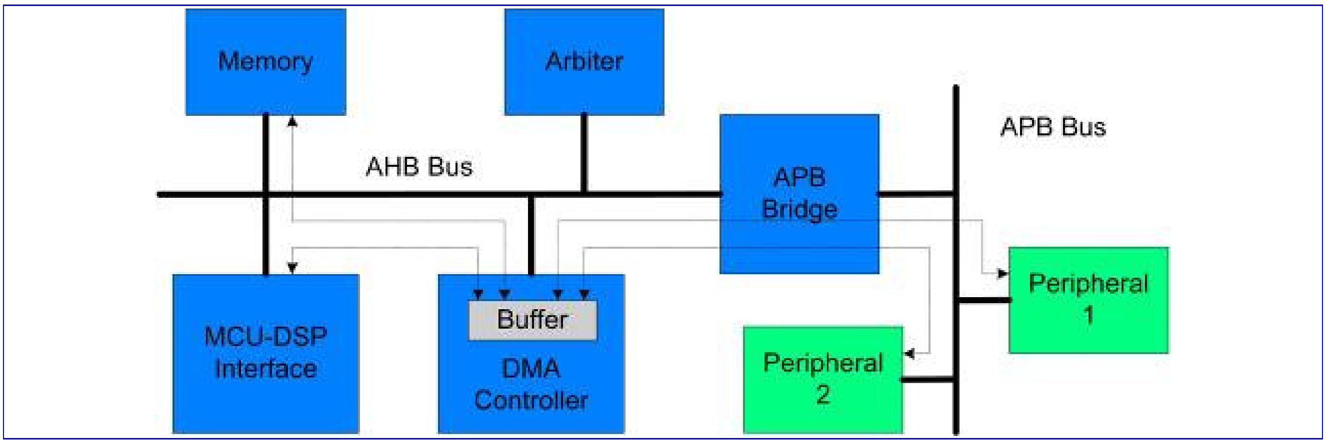

Figure 10 Variety Data Paths of DMA Transfers

Up to fourteen channels of simultaneous data transfers are supported. Each channel has a similar set of registers to be configured to different scheme as desired. If more than fourteen devices are requesting the DMA resources at the same time, software based arbitration should be employed. Once the service candidate is decided, the responsible device driver should configure the Generic DMA Controller properly in order to conduct DMA transfers. Both Interrupt and Polling based schemes in handling the completion event are supported. The block diagram of such generic DMA Controller is illustrated in **Figure 11**.

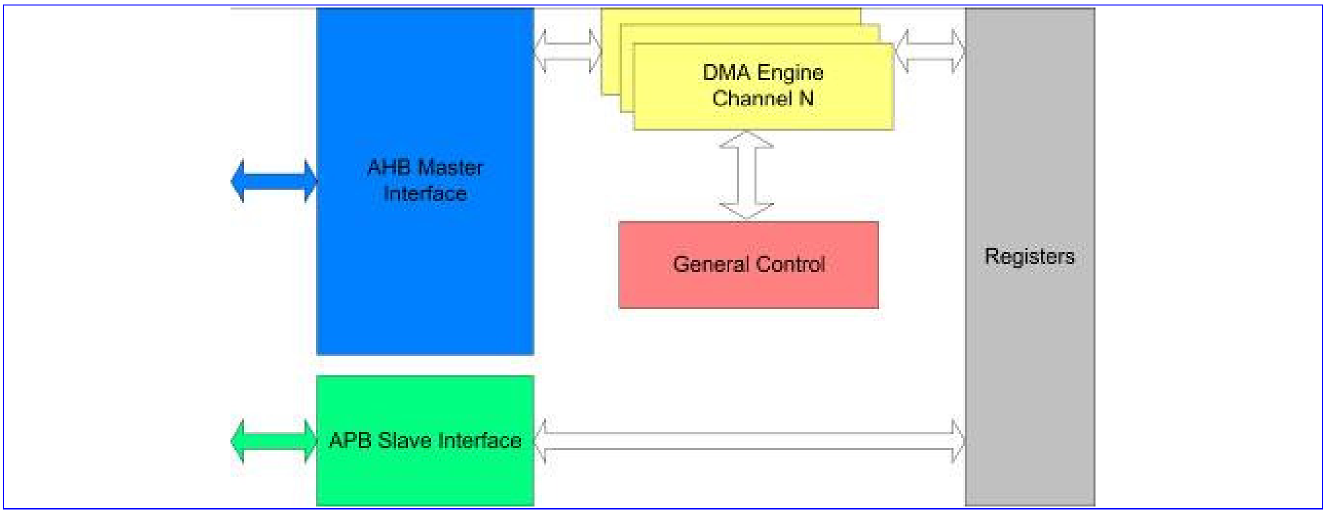

Figure 11 Block Diagram of Direct memory Access Module

3.4.1.1 Full-Size & Half-Size DMA Channels

There are three types of DMA channels in the DMA controller. The first one is called a full-size DMA channel, the second one is called a half-size DMA channel, and the last is Virtual FIFO DMA. Channels 1 through 4 are full-size DMA channels; channels 5 through 11 are half-size ones; and channels 12 through 17 are Virtual FIFO DMAs. The difference

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between the first two types of DMA channels is that both source and destination address are programmable in full-size DMA channels, but only the address of one side can be programmed in half-size DMA channel. In half-size channels, only either the source or destination address can be programmed, while the addresses of the other side is preset. Which preset address is used depends on the setting of MAS in DMA Channel Control Register. Refer to the Register Definition section for more detail.

3.4.1.2 Ring Buffer & Double Buffer Memory Data Movement

DMA channels 1 through 10 support ring-buffer and double-buffer memory data movement. This can be achieved by programming DMA_WPPT and DMA_WPTO, as well as setting WPEN in DMA_CON register to enable. **Figure 12** illustrates how this function works. Once the transfer counter reaches the value of WPPT, the next address jumps to the WPTO address after completing the WPPT data transfer. Note that only one side can be configured as ring-buffer or double-buffer memory, and this is controlled by WPSD in DMA_CON register.

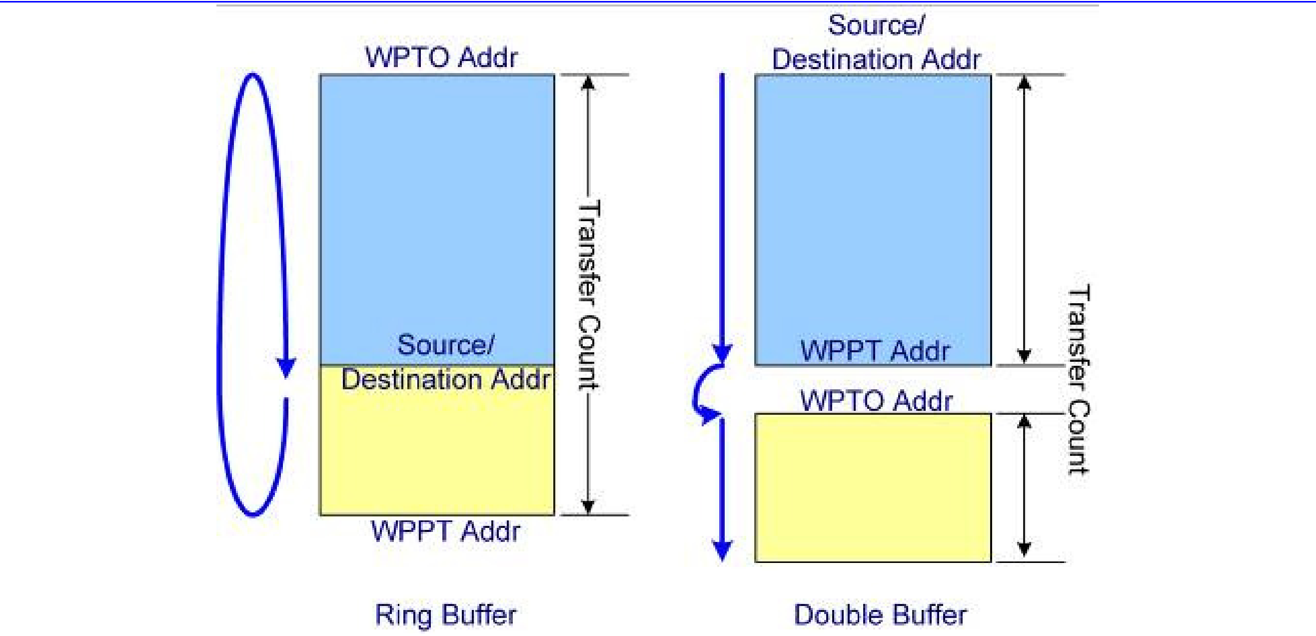

Figure 12 Ring Buffer and Double Buffer Memory Data Movement

3.4.1.3 Unaligned Word Access

The address of word access on AHB bus must be aligned to word boundary, or the 2 LSB is truncated to 00b. If programmers do not notice this, it may cause an incorrect data fetch. In the case where data is to be moved from unaligned addresses to aligned addresses, the word is usually first split into four bytes and then moved byte by byte. This results in four read and four write transfers on the bus.

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To improve bus efficiency, unaligned-word access is provided in DMA5~11. While this function is enabled, DMAs move data from unaligned address to aligned address by executing four continuous byte-read access and one word-write access, reducing the number of transfers on the bus by three.

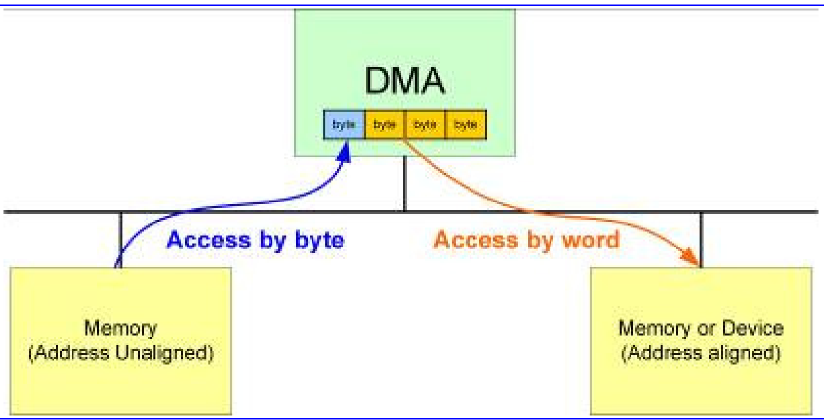

Figure 13 Unaligned Word Accesses

3.4.1.4 Virtual FIFO DMA

Virtual FIFO DMA is used to ease UART control. The difference between the Virtual FIFO DMAs and the ordinary DMAs is that Virtual FIFO DMA contains additional FIFO controller. The read and write pointers are kept in the Virtual FIFO DMA. During a read from the FIFO, the read pointer points to the address of the next data. During a write to the FIFO, the write pointer moves to the next address. If the FIFO is empty, a FIFO read is not allowed. Similarly, data is not written into the FIFO if the FIFO is full. Due to UART flow control requirements, an alert length is programmed. Once the FIFO Space is less than this value, an alert signal is issued to enable UART flow control. The type of flow control performed depends on the setting in UART.

Each Virtual FIFO DMA can be programmed as RX or TX FIFO. This depends on the setting of DIR in DMA_CON register. If DIR is “0”(READ), it means TX FIFO. On the other hand, if DIR is “1”(WRITE), the Virtual FIFO DMA is specified as a RX FIFO.

Virtual FIFO DMA provides an interrupt to MCU. This interrupt informs MCU that there is data in the FIFO, and the amount of data is over or under the value defined in DMA_COUNT register. With this, MCU does not need to poll DMA to know when data must be removed from or put into the FIFO.

Note that Virtual FIFO DMAs cannot be used as generic DMAs, i.e. DMA1~11.

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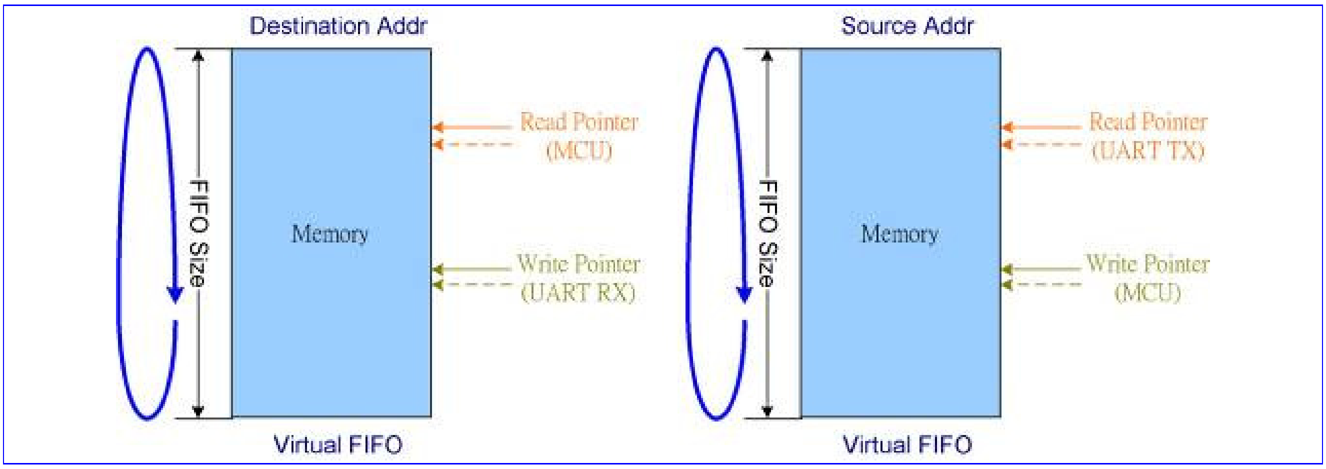

Figure 14 Virtual FIFO DMA

DMA number	Address of Virtual FIFO Access Port	Reference UART
DMA12	7800_0000h	UART1 RX
DMA13	7800_0100h	UART2 RX
DMA14	7800_0200h	UART3 RX
DMA15	7800_0300h	UART1 TX
DMA16	7800_0400h	UART2 TX
DMA17	7800_0500h	UART3 TX

Table 6 Virtual FIFO Access Port

DMA number	Type	Ring Buffer	Double Buffer	Burst Mode	Unaligned Word Access
DMA1	Full Size	●	●	●	
DMA2	Full Size	●	●	●	
DMA3	Full Size	●	●	●	
DMA4	Full Size	●	●	●	
DMA5	Half Size	●	●	●	●
DMA6	Half Size	●	●	●	●
DMA7	Half Size	●	●	●	●
DMA8	Half Size	●	●	●	●
DMA9	Half Size	●	●	●	●
DMA10	Half Size	●	●	●	●
DMA11	Half Size	●	●	●	●
DMA12	Virtual FIFO	●			

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DMA13	Virtual FIFO	●			
DMA14	Virtual FIFO	●			
DMA15	Virtual FIFO	●			
DMA16	Virtual FIFO	●			
DMA17	Virtual FIFO	●			

Table 7 Function List of DMA channels

REGISTER ADDRESS	REGISTER NAME	SYNONYM
0x8102_0000h	DMA Global Status Register	DMA_GLBSTA
0x8102_0028h	DMA Global Bandwidth Limiter Register	DMA_GLBLIMITER
0x8102_0100h	DMA Channel 1 Source Address Register	DMA1_SRC
0x8102_0104h	DMA Channel 1 Destination Address Register	DMA1_DST
0x8102_0108h	DMA Channel 1 Wrap Point Address Register	DMA1_WPPT
0x8102_010Ch	DMA Channel 1 Wrap To Address Register	DMA1_WPTO
0x8102_0110h	DMA Channel 1 Transfer Count Register	DMA1_COUNT
0x8102_0114h	DMA Channel 1 Control Register	DMA1_CON
0x8102_0118h	DMA Channel 1 Start Register	DMA1_START
0x8102_011Ch	DMA Channel 1 Interrupt Status Register	DMA1_INTSTA
0x8102_0120h	DMA Channel 1 Interrupt Acknowledge Register	DMA1_ACKINT
0x8102_0124h	DMA Channel 1 Remaining Length of Current Transfer	DMA1_RLCT
0x8102_0128h	DMA Channel 1 Bandwidth Limiter Register	DMA1_LIMITER
0x8102_0200h	DMA Channel 2 Source Address Register	DMA2_SRC
0x8102_0204h	DMA Channel 2 Destination Address Register	DMA2_DST
0x8102_0208h	DMA Channel 2 Wrap Point Address Register	DMA2_WPPT
0x8102_020Ch	DMA Channel 2 Wrap To Address Register	DMA2_WPTO
0x8102_0210h	DMA Channel 2 Transfer Count Register	DMA2_COUNT
0x8102_0214h	DMA Channel 2 Control Register	DMA2_CON
0x8102_0218h	DMA Channel 2 Start Register	DMA2_START
0x8102_021Ch	DMA Channel 2 Interrupt Status Register	DMA2_INTSTA
0x8102_0220h	DMA Channel 2 Interrupt Acknowledge Register	DMA2_ACKINT
0x8102_0224h	DMA Channel 2 Remaining Length of Current Transfer	DMA2_RLCT
0x8102_0228h	DMA Channel 2 Bandwidth Limiter Register	DMA2_LIMITER
0x8102_0300h	DMA Channel 3 Source Address Register	DMA3_SRC
0x8102_0304h	DMA Channel 3 Destination Address Register	DMA3_DST
0x8102_0308h	DMA Channel 3 Wrap Point Address Register	DMA3_WPPT
0x8102_030Ch	DMA Channel 3 Wrap To Address Register	DMA3_WPTO

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0x8102_0310h	DMA Channel 3 Transfer Count Register	DMA3_COUNT
0x8102_0314h	DMA Channel 3 Control Register	DMA3_CON
0x8102_0318h	DMA Channel 3 Start Register	DMA3_START
0x8102_031Ch	DMA Channel 3 Interrupt Status Register	DMA3_INTSTA
0x8102_0320h	DMA Channel 3 Interrupt Acknowledge Register	DMA3_ACKINT
0x8102_0324h	DMA Channel 3 Remaining Length of Current Transfer	DMA3_RLCT
0x8102_0328h	DMA Channel 3 Bandwidth Limiter Register	DMA3_LIMITER
0x8102_0400h	DMA Channel 4 Source Address Register	DMA4_SRC
0x8102_0404h	DMA Channel 4 Destination Address Register	DMA4_DST
0x8102_0408h	DMA Channel 4 Wrap Point Address Register	DMA4_WPPT
0x8102_040Ch	DMA Channel 4 Wrap To Address Register	DMA4_WPTO
0x8102_0410h	DMA Channel 4 Transfer Count Register	DMA4_COUNT
0x8102_0414h	DMA Channel 4 Control Register	DMA4_CON
0x8102_0418h	DMA Channel 4 Start Register	DMA4_START
0x8102_041Ch	DMA Channel 4 Interrupt Status Register	DMA4_INTSTA
0x8102_0420h	DMA Channel 4 Interrupt Acknowledge Register	DMA4_ACKINT
0x8102_0424h	DMA Channel 4 Remaining Length of Current Transfer	DMA4_RLCT
0x8102_0428h	DMA Channel 4 Bandwidth Limiter Register	DMA4_LIMITER
0x8102_0508h	DMA Channel 5 Wrap Point Address Register	DMA5_WPPT
0x8102_050Ch	DMA Channel 5 Wrap To Address Register	DMA5_WPTO
0x8102_0510h	DMA Channel 5 Transfer Count Register	DMA5_COUNT
0x8102_0514h	DMA Channel 5 Control Register	DMA5_CON
0x8102_0518h	DMA Channel 5 Start Register	DMA5_START
0x8102_051Ch	DMA Channel 5 Interrupt Status Register	DMA5_INTSTA
0x8102_0520h	DMA Channel 5 Interrupt Acknowledge Register	DMA5_ACKINT
0x8102_0524h	DMA Channel 5 Remaining Length of Current Transfer	DMA5_RLCT
0x8102_0528h	DMA Channel 5 Bandwidth Limiter Register	DMA5_LIMITER
0x8102_052Ch	DMA Channel 5 Programmable Address Register	DMA5_PGMADDR
0x8102_0608h	DMA Channel 6 Wrap Point Address Register	DMA6_WPPT
0x8102_060Ch	DMA Channel 6 Wrap To Address Register	DMA6_WPTO
0x8102_0610h	DMA Channel 6 Transfer Count Register	DMA6_COUNT
0x8102_0614h	DMA Channel 6 Control Register	DMA6_CON
0x8102_0618h	DMA Channel 6 Start Register	DMA6_START
0x8102_061Ch	DMA Channel 6 Interrupt Status Register	DMA6_INTSTA
0x8102_0620h	DMA Channel 6 Interrupt Acknowledge Register	DMA6_ACKINT
0x8102_0624h	DMA Channel 6 Remaining Length of Current Transfer	DMA6_RLCT

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0x8102_0628h	DMA Channel 6 Bandwidth Limiter Register	DMA6_LIMITER
0x8102_062Ch	DMA Channel 6 Programmable Address Register	DMA6_PGMADDR
0x8102_0708h	DMA Channel 7 Wrap Point Address Register	DMA7_WPPT
0x8102_070Ch	DMA Channel 7 Wrap To Address Register	DMA7_WPTO
0x8102_0710h	DMA Channel 7 Transfer Count Register	DMA7_COUNT
0x8102_0714h	DMA Channel 7 Control Register	DMA7_CON
0x8102_0718h	DMA Channel 7 Start Register	DMA7_START
0x8102_071Ch	DMA Channel 7 Interrupt Status Register	DMA7_INTSTA
0x8102_0720h	DMA Channel 7 Interrupt Acknowledge Register	DMA7_ACKINT
0x8102_0724h	DMA Channel 7 Remaining Length of Current Transfer	DMA7_RLCT
0x8102_0728h	DMA Channel 7 Bandwidth Limiter Register	DMA7_LIMITER
0x8102_072Ch	DMA Channel 7 Programmable Address Register	DMA7_PGMADDR
0x8102_0808h	DMA Channel 8 Wrap Point Address Register	DMA8_WPPT
0x8102_080Ch	DMA Channel 8 Wrap To Address Register	DMA8_WPTO
0x8102_0810h	DMA Channel 8 Transfer Count Register	DMA8_COUNT
0x8102_0814h	DMA Channel 8 Control Register	DMA8_CON
0x8102_0818h	DMA Channel 8 Start Register	DMA8_START
0x8102_081Ch	DMA Channel 8 Interrupt Status Register	DMA8_INTSTA
0x8102_0820h	DMA Channel 8 Interrupt Acknowledge Register	DMA8_ACKINT
0x8102_0824h	DMA Channel 8 Remaining Length of Current Transfer	DMA8_RLCT
0x8102_0828h	DMA Channel 8 Bandwidth Limiter Register	DMA8_LIMITER
0x8102_082Ch	DMA Channel 8 Programmable Address Register	DMA8_PGMADDR
0x8102_0908h	DMA Channel 9 Wrap Point Address Register	DMA9_WPPT
0x8102_090Ch	DMA Channel 9 Wrap To Address Register	DMA9_WPTO
0x8102_0910h	DMA Channel 9 Transfer Count Register	DMA9_COUNT
0x8102_0914h	DMA Channel 9 Control Register	DMA9_CON
0x8102_0918h	DMA Channel 9 Start Register	DMA9_START
0x8102_091Ch	DMA Channel 9 Interrupt Status Register	DMA9_INTSTA
0x8102_0920h	DMA Channel 9 Interrupt Acknowledge Register	DMA9_ACKINT
0x8102_0924h	DMA Channel 9 Remaining Length of Current Transfer	DMA9_RLCT
0x8102_0928h	DMA Channel 9 Bandwidth Limiter Register	DMA9_LIMITER
0x8102_092Ch	DMA Channel 9 Programmable Address Register	DMA9_PGMADDR
0x8102_0A08h	DMA Channel 10 Wrap Point Address Register	DMA10_WPPT
0x8102_0A0Ch	DMA Channel 10 Wrap To Address Register	DMA10_WPTO
0x8102_0A10h	DMA Channel 10 Transfer Count Register	DMA10_COUNT
0x8102_0A14h	DMA Channel 10 Control Register	DMA10_CON

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0x8102_0A18h	DMA Channel 10 Start Register	DMA10_START
0x8102_0A1Ch	DMA Channel 10 Interrupt Status Register	DMA10_INTSTA
0x8102_0A20h	DMA Channel 10 Interrupt Acknowledge Register	DMA10_ACKINT
0x8102_0A24h	DMA Channel 10 Remaining Length of Current Transfer	DMA10_RLCT
0x8102_0A28h	DMA Channel 10 Bandwidth Limiter Register	DMA10_LIMITER
0x8102_0A2Ch	DMA Channel 10 Programmable Address Register	DMA10_PGMADDR
0x8102_0B08h	DMA Channel 11 Wrap Point Address Register	DMA11_WPPT
0x8102_0B0Ch	DMA Channel 11 Wrap To Address Register	DMA11_WPTO
0x8102_0B10h	DMA Channel 11 Transfer Count Register	DMA11_COUNT
0x8102_0B14h	DMA Channel 11 Control Register	DMA11_CON
0x8102_0B18h	DMA Channel 11 Start Register	DMA11_START
0x8102_0B1Ch	DMA Channel 11 Interrupt Status Register	DMA11_INTSTA
0x8102_0B20h	DMA Channel 11 Interrupt Acknowledge Register	DMA11_ACKINT
0x8102_0B24h	DMA Channel 11 Remaining Length of Current Transfer	DMA11_RLCT
0x8102_0B28h	DMA Channel 11 Bandwidth Limiter Register	DMA11_LIMITER
0x8102_0B2Ch	DMA Channel 11 Programmable Address Register	DMA11_PGMADDR
0x8102_0C10h	DMA Channel 12 Transfer Count Register	DMA12_COUNT
0x8102_0C14h	DMA Channel 12 Control Register	DMA12_CON
0x8102_0C18h	DMA Channel 12 Start Register	DMA12_START
0x8102_0C1Ch	DMA Channel 12 Interrupt Status Register	DMA12_INTSTA
0x8102_0C20h	DMA Channel 12 Interrupt Acknowledge Register	DMA12_ACKINT
0x8102_0C28h	DMA Channel 12 Bandwidth Limiter Register	DMA12_LIMITER
0x8102_0C2Ch	DMA Channel 12 Programmable Address Register	DMA12_PGMADDR
0x8102_0C30h	DMA Channel 12 Write Pointer	DMA12_WRPTR
0x8102_0C34h	DMA Channel 12 Read Pointer	DMA12_RDPTR
0x8102_0C38h	DMA Channel 12 FIFO Count	DMA12_FFCNT
0x8102_0C3Ch	DMA Channel 12 FIFO Status	DMA12_FFSTA
0x8102_0C40h	DMA Channel 12 Alert Length	DMA12_ALTLEN
0x8102_0C44h	DMA Channel 12 FIFO Size	DMA12_FFSIZE
0x8102_0D10h	DMA Channel 13 Transfer Count Register	DMA13_COUNT
0x8102_0D14h	DMA Channel 13 Control Register	DMA13_CON
0x8102_0D18h	DMA Channel 13 Start Register	DMA13_START
0x8102_0D1Ch	DMA Channel 13 Interrupt Status Register	DMA13_INTSTA
0x8102_0D20h	DMA Channel 13 Interrupt Acknowledge Register	DMA13_ACKINT

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0x8102_0D28h	DMA Channel 13 Bandwidth Limiter Register	DMA13_LIMITER
0x8102_0D2Ch	DMA Channel 13 Programmable Address Register	DMA13_PGMADDR
0x8102_0D30h	DMA Channel 13 Write Pointer	DMA13_WRPTR
0x8102_0D34h	DMA Channel 13 Read Pointer	DMA13_RDPTR
0x8102_0D38h	DMA Channel 13 FIFO Count	DMA13_FFCNT
0x8102_0D3Ch	DMA Channel 13 FIFO Status	DMA13_FFSTA
0x8102_0D40h	DMA Channel 13 Alert Length	DMA13_ALTLEN
0x8102_0D44h	DMA Channel 13 FIFO Size	DMA13_FFSIZE
0x8102_0E10h	DMA Channel 14 Transfer Count Register	DMA14_COUNT
0x8102_0E14h	DMA Channel 14 Control Register	DMA14_CON
0x8102_0E18h	DMA Channel 14 Start Register	DMA14_START
0x8102_0E1Ch	DMA Channel 14 Interrupt Status Register	DMA14_INTSTA
0x8102_0E20h	DMA Channel 14 Interrupt Acknowledge Register	DMA14_ACKINT
0x8102_0E28h	DMA Channel 14 Bandwidth Limiter Register	DMA14_LIMITER
0x8102_0E2Ch	DMA Channel 14 Programmable Address Register	DMA14_PGMADDR
0x8102_0E30h	DMA Channel 14 Write Pointer	DMA14_WRPTR
0x8102_0E34h	DMA Channel 14 Read Pointer	DMA14_RDPTR
0x8102_0E38h	DMA Channel 14 FIFO Count	DMA14_FFCNT
0x8102_0E3Ch	DMA Channel 14 FIFO Status	DMA14_FFSTA
0x8102_0E40h	DMA Channel 14 Alert Length	DMA14_ALTLEN
0x8102_0E44h	DMA Channel 14 FIFO Size	DMA14_FFSIZE
0x8102_0F10h	DMA Channel 15 Transfer Count Register	DMA15_COUNT
0x8102_0F14h	DMA Channel 15 Control Register	DMA15_CON
0x8102_0F18h	DMA Channel 15 Start Register	DMA15_START
0x8102_0F1Ch	DMA Channel 15 Interrupt Status Register	DMA15_INTSTA
0x8102_0F20h	DMA Channel 15 Interrupt Acknowledge Register	DMA15_ACKINT
0x8102_0F28h	DMA Channel 15 Bandwidth Limiter Register	DMA15_LIMITER
0x8102_0F2Ch	DMA Channel 15 Programmable Address Register	DMA15_PGMADDR
0x8102_0F30h	DMA Channel 15 Write Pointer	DMA15_WRPTR
0x8102_0F34h	DMA Channel 15 Read Pointer	DMA15_RDPTR
0x8102_0F38h	DMA Channel 15 FIFO Count	DMA15_FFCNT
0x8102_0F3Ch	DMA Channel 15 FIFO Status	DMA15_FFSTA
0x8102_0F40h	DMA Channel 15 Alert Length	DMA15_ALTLEN
0x8102_0F44h	DMA Channel 15 FIFO Size	DMA15_FFSIZE
0x8102_1010h	DMA Channel 16 Transfer Count Register	DMA16_COUNT
0x8102_1014h	DMA Channel 16 Control Register	DMA16_CON

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0x8102_1018h	DMA Channel 16 Start Register	DMA16_START
0x8102_101Ch	DMA Channel 16 Interrupt Status Register	DMA16_INTSTA
0x8102_1020h	DMA Channel 16 Interrupt Acknowledge Register	DMA16_ACKINT
0x8102_1028h	DMA Channel 16 Bandwidth Limiter Register	DMA16_LIMITER
0x8102_102Ch	DMA Channel 16 Programmable Address Register	DMA16_PGMADDR
0x8102_1030h	DMA Channel 16 Write Pointer	DMA16_WRPTR
0x8102_1034h	DMA Channel 16 Read Pointer	DMA16_RDPTR
0x8102_1038h	DMA Channel 16 FIFO Count	DMA16_FFCNT
0x8102_103Ch	DMA Channel 16 FIFO Status	DMA16_FFSTA
0x8102_1040h	DMA Channel 16 Alert Length	DMA16_ALTLEN
0x8102_1044h	DMA Channel 16 FIFO Size	DMA16_FFSIZE
0x8102_1110h	DMA Channel 17 Transfer Count Register	DMA17_COUNT
0x8102_1114h	DMA Channel 17 Control Register	DMA17_CON
0x8102_1118h	DMA Channel 17 Start Register	DMA17_START
0x8102_111Ch	DMA Channel 17 Interrupt Status Register	DMA17_INTSTA
0x8102_1120h	DMA Channel 17 Interrupt Acknowledge Register	DMA17_ACKINT
0x8102_1128h	DMA Channel 17 Bandwidth Limiter Register	DMA17_LIMITER
0x8102_112Ch	DMA Channel 17 Programmable Address Register	DMA17_PGMADDR
0x8102_1130h	DMA Channel 17 Write Pointer	DMA17_WRPTR
0x8102_1134h	DMA Channel 17 Read Pointer	DMA17_RDPTR
0x8102_1138h	DMA Channel 17 FIFO Count	DMA17_FFCNT
0x8102_113Ch	DMA Channel 17 FIFO Status	DMA17_FFSTA
0x8102_1140h	DMA Channel 17 Alert Length	DMA17_ALTLEN
0x8102_1144h	DMA Channel 17 FIFO Size	DMA17_FFSIZE

Table 8 DMA Controller Register Map

3.4.2 Register Definitions

Register programming tips:

- Start registers shall be cleared, when associated channels are being programmed.
- PGMADDR, i.e. programmable address, only exists in half-size DMA channels. If DIR in Control Register is high, PGMADDR represents Destination Address. Conversely, If DIR in Control Register is low, PGMADDR represents Source Address.
- Functions of ring-buffer and double-buffer memory data movement can be activated on either source side or destination side by programming DMA_WPPT & and DMA_WPTO, as well as setting WPEN in DMA_CON register high. WPSD in DMA_CON register determines the activated side.

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0x8102_0000h DMA Global Status Register DMA_GLBSTA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IT16	RUN16	IT15	RUN15	IT14	RUN14	IT13	RUN13	IT12	RUN12	IT11	RUN11	IT10	RUN10	IT9	RUN9
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IT8	RUN8	IT7	RUN7	IT6	RUN6	IT5	RUN5	IT4	RUN4	IT3	RUN3	IT2	RUN2	IT1	RUN1
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8102_0004h DMA Global Status Register DMA_GLBSTA2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															IT17	RUN17
Type															RO	RO
Reset															0	0

This register helps software program keep track of the global status of DMA channels.

RUN_N DMA channel n status

- **0** Channel n is stopped or has completed the transfer already.
- **1** Channel n is currently running.

IT_N Interrupt status for channel n

- **0** No interrupt is generated.
- **1** An interrupt is pending and waiting for service.

0x8102_0028h DMA Global Bandwidth limiter Register DMA_GLBLIMITER

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									GLBLIMITER							
Type									WO							
Reset									0							

Please refer to the expression in DMAn_LIMITER for detailed note. The value of DMA_GLBLIMITER is set to all DMA channels, from 1 to 17.

0x8102_0n00h DMA Channel n Source Address Register DMAn_SRC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	SRC[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC[15:0]															
Type	R/W															
Reset	0															

The above registers contain the base or current source address that the DMA channel is currently operating on. Writing to this register specifies the base address of transfer source for a DMA channel. Before programming these registers, the software program should make sure that STR in DMAn_START is set to 0; that is, the DMA channel is stopped and disabled completely. Otherwise, the DMA channel may run out of order. Reading this register returns the address value from which the DMA is reading.

Note that n is from 1 to 4 and SRC can't be TCM address. TCM is not accessible by DMA.

SRC **SRC**[31:0] specifies the base or current address of transfer source for a DMA channel, i.e. channel 1 - 4.

WRITE Base address of transfer source

READ Address from which DMA is reading

0x8102_0n04h DMA Channel n Destination Address Register DMAn_DST

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DST[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DST[15:0]															
Type	R/W															
Reset	0															

The above registers contain the base or current destination address that the DMA channel is currently operating on.. Writing to this register specifies the base address of the transfer destination for a DMA channel. Before programming these registers, the software should make sure that STR in DMAn_START is set to '0'; that is, the DMA channel is stopped and disabled completely. Otherwise, the DMA channel may run out of order. Reading this register returns the address value to which the DMA is writing.

Note that n is from 1 to 4 and DST can't be TCM address. TCM is not accessible by DMA.

DST **DST**[31:0] specifies the base or current address of transfer destination for a DMA channel, i.e. channel 1 - 4.

WRITE Base address of transfer destination.

READ Address to which DMA is writing.

0x8102_0n08h DMA Channel n Wrap Point Count Register DMAn_WPPT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	WPPT[15:0]
Type	R/W
Reset	0

The above registers are to specify the transfer count required to perform before the jump point. This can be used to support ring buffer or double buffer style memory accesses. To enable this function, two control bits, WPEN and WPSD, in DMA control register must be programmed. See the following register description for more details. If the transfercounter in the DMA engine matches this value, an address jump occurs, and the next address is the address specified in DMAn_WPTO. Before programming these registers, the software should make sure that STR in DMAn_START is set to '0', that is the DMA channel is stopped and disabled completely. Otherwise, the DMA channel may run out of order. To enable this function, WPEN in DMA_CON is set.

Note that n is from 1 to 11.

WPPT **WPPT**[15:0] specifies the amount of the transfer count from start to jumping point for a DMA channel, i.e. channel 1 – 11.

WRITE Wrap point count.

READ Value set by the programmer.

0x8102_0n0Ch DMA Channel n Wrap To Address Register DMAn_WPTO

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WPTO[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WPTO[15:0]															
Type	R/W															
Reset	0															

The above registers specify the address of the jump destination of a given DMA transfer to support ring buffer or double buffer style memory accesses. To enable this function, set the two control bits, WPEN and WPSD, in the DMA control register . See the following register description for more details. Before programming these registers, the software should make sure that STR in DMAn_START is set to '0', that is the DMA channel is stopped and disabled completely. Otherwise, the DMA channel may run out of order. To enable this function, WPEN in DMA_CON should be set.

Note that n is from 1 to 11.

WPTO **WPTO**[31:0] specifies the address of the jump point for a DMA channel, i.e. channel 1 – 11.

WRITE Address of the jump destination.

READ Value set by the programmer.

0x8102_0n10h DMA Channel n Transfer Count Register DMAn_COUNT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	LEN
Type	R/W
Reset	0

This register specifies the amount of total transfer count that the DMA channel is required to perform. Upon completion, the DMA channel generates an interrupt request to the processor while ITEN in DMAn_CON is set as '1'. Note that the total size of data being transferred by a DMA channel is determined by LEN together with the SIZE in DMAn_CON, i.e. LEN x SIZE.

For virtual FIFO DMA, this register is used to configure the RX threshold and TX threshold. Interrupt is triggered while FIFO count >= RX threshold in RX path or FIFO count =< TX threshold in TX path. Note that ITEN bit in DMA_CON register shall be set, or no interrupt is issued.

Note that n is from 1 to 17.

LEN The amount of total transfer count

0x8102_0n14h DMA Channel n Control Register DMAn_CON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								MAS						DIR	WPEN	WPSD
Type								R/W						R/W	R/W	R/W
Reset								0						0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ITEN					BURST					B2W	DRQ	DINC	SINC	SIZE	
Type	R/W					R/W					R/W	R/W	R/W	R/W	R/W	
Reset	0					0					0	0	0	0	0	

This register contains all the available control schemes for a DMA channel that is ready for software programmer to configure. Note that all these fields cannot be changed while DMA transfer is in progress or an unexpected situation may occur.

Note that n is from 1 to 17.

SIZE Data size within the confine of a bus cycle per transfer.
These bits confines the data transfer size between source and destination to the specified value for individual bus cycle. The size is in terms of byte and has maximum value of 4 bytes. It is mainly decided by the data width of a DMA master.
- **00** Byte transfer/1 byte
- **01** Half-word transfer/2 bytes
- **10** Word transfer/4 bytes
- **11** Reserved

SINC Incremental source address. Source addresses increase every transfer. If the setting of SIZE is Byte, Source addresses increase by 1 every single transfer. If Half-Word, increase by 2; and if Word, increase by 4.
- **0** Disable
- **1** Enable

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DINC Incremental destination address. Destination addresses increase every transfer. If the setting of SIZE is Byte, Destination addresses increase by 1 every single transfer. If Half-Word, increase by 2; and Iif Word, increase by 4.

0 Disable

1 Enable

DREQ Throttle and handshake control for DMA transfer

0 No throttle control during DMA transfer or transfers occurred only between memories

1 Hardware handshake management

The DMA master is able to throttle down the transfer rate by way of request-grant handshake.

B2W Word to Byte or Byte to Word transfer for the applications of transferring non-word-aligned-address data to word-aligned-address data. Note that BURST is set to 4-beat burst while enabling this function, and the SIZE is set to Byte.

NO effect on channel 1 – 4 & 12 - 17.

0 Disable

1 Enable

BURST Transfer Type. Burst-type transfers have better bus efficiency. Mass data movement is recommended to use this kind of transfer. However, note that burst-type transfer does not stop until all of the beats in a burst are completed or transfer length is reached. FIFO threshold of peripherals must be configured carefully while being used to move data from/to the peripherals.

What transfer type can be used is restricted by the SIZE. If SIZE is 00b, i.e. byte transfer, all of the four transfer types can be used. If SIZE is 01b, i.e. half-word transfer, 16-beat incrementing burst cannot be used. If SIZE is 10b, i.e. word transfer, only single and 4-beat incrementing burst can be used.

NO effect on channel 12 - 17.

000 Single

001 Reserved

010 4-beat incrementing burst

011 Reserved

100 8-beat incrementing burst

101 Reserved

110 16-beat incrementing burst

111 Reserved

ITEN DMA transfer completion interrupt enable.

0 Disable

1 Enable

WPSD The side using address-wrapping function. Only one side of a DMA channel can activate address-wrapping function at a time.

NO effect on channel 12 - 17.

0 Address-wrapping on source .

1 Address-wrapping on destination.

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WPEN Address-wrapping for ring buffer and double buffer. The next address of DMA jumps to WRAP TO address when the current address matches WRAP POINT count.

NO effect on channel 12 - 17.

0 Disable

1 Enable

DIR Directions of DMA transfer for half-size and Virtual FIFO DMA channels, i.e. channels 5~17. The direction is from the perspective of the DMA masters. WRITE means read from master and then write to the address specified in DMA_PGMADDR, and vice versa.

NO effect on channel 1 - 4.

0 Read

1 Write

MAS Master selection. Specifies which master occupies this DMA channel. Once assigned to certain master, the corresponding DREQ and DACK are connected. For half-size and Virtual FIFO DMA channels, i.e. channels 5 ~ 17, a predefined address is assigned as well.

00000 SIM
00001 MSDC
00010 IrDA TX
00011 IrDA RX
00100 Reserved
00101 Reserved
00110 Reserved
00111 Reserved
01000 UART1 TX
01001 UART1 RX
01010 UART2 TX
01011 UART2 RX
01100 UART3 TX
01101 UART3 RX
01110 DSP-DMA
01111 NFI TX
10000 NFI RX
10001 I2C TX
10010 I2C RX
10011 SIM2
OTHERS Reserved

0x8102_0n18h DMA Channel n Start Register — DMAn_START

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**STR**															
Type	R/W															
Reset	0															

This register controls the activity of a DMA channel. Note that prior to setting STR to "1", all the configurations should be done by giving proper value to the registers. Note also that once the STR is set to "1", the hardware does not clear it automatically no matter if the DMA channel accomplishes the DMA transfer or not. In other works, the value of **STR** stays "1" regardless of the completion of DMA transfer. Therefore, the software program should be sure to clear **STR** to "0" before restarting another DMA transfer.

Note that n is from 1 to 17.

STR Start control for a DMA channel.

- **0** The DMA channel is stopped.
- **1** The DMA channel is started and running.

0x8102_0n1Ch DMA Channel n Interrupt Status Register DMAn_INTSTA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**INT**															
Type	RO															
Reset	0															

This register shows the interrupt status of a DMA channel. It has the same value as DMA_GLBSTA.

Note that n is from 1 to 17.

INT Interrupt Status for DMA Channel

- **0** No interrupt request is generated.
- **1** One interrupt request is pending and waiting for service.

0x8102_0n20h DMA Channel n Interrupt Acknowledge Register DMAn_ACKINT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ACK**															
Type	WO															
Reset	0															

This register is used to acknowledge the current interrupt request associated with the completion event of a DMA channel by software program. Note that this is a write-only register, and any read to it returns a value of "0".

Note that n is from 1 to 17.

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ACK Interrupt acknowledge for the DMA channel

- **0** No effect
- **1** Interrupt request is acknowledged and should be relinquished.

0x8102_0n24h DMA Channel n Remaining Length of Current Transfer DMAn_RLCT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLCT															
Type	RO															
Reset	0															

This register is to reflect the left count of the transfer.

Note that n is from 1 to 11.

0x8102_0n28h DMA Bandwidth limiter Register DMAn_LIMITER

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LIMITER							
Type									R/W							
Reset									0							

This register is to suppress the Bus utilization of the DMA channel. The value is from 0 to 255. 0 means no limitation, and 255 means totally banned. The value between 0 and 255 means certain DMA can have permission to use AHB every (4 X n) AHB clock cycles.

Note that it is not recommended to limit the Bus utilization of the DMA channels because this increases the latency of response to the masters, and the transfer rate decreases as well. Before using it, programmer must make sure that the bus masters have some protective mechanism to avoid entering the wrong states.

Note that n is from 1 to 17.

LIMITER from 0 to 255. 0 means no limitation, 255 means totally banned, and others mean Bus access permission every (4 X n) AHB clock.

0x8102_0n2Ch DMA Channel n Programmable Address Register DMAn_PGMADDR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PGMADDR[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PGMADDR[15:0]															

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Type	R/W
Reset	0

The above registers specify the address for a half-size DMA channel. This address represents a source address if DIR in DMA_CON is set to 0, and represents a destination address if DIR in DMA_CON is set to 1. Before being able to program these register, the software should make sure that STR in DMAn_START is set to '0', that is the DMA channel is stopped and disabled completely. Otherwise, the DMA channel may run out of order.

Note that n is from 5 to 17 and PGMADDR can't be TCM address. TCM is not accessible by DMA.

PGMADDR **PGMADDR**[31:0] specifies the addresses for a half-size or a Virtual FIFO DMA channel, i.e. channel 4 – 14.

WRITE Base address of transfer source or destination according to DIR bit

READ Current address of the transfer.

0x8102_0n30h DMA Channel n Virtual FIFO Write Pointer Register DMAn_WRPTR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WRPTR[31:16]															
Type	RO															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WRPTR[15:0]															
Type	RO															

Note that n is from 12 to 17.

WRPTR Virtual FIFO Write Pointer.

0x8102_0n34h DMA Channel n Virtual FIFO Read Pointer Register DMAn_RDPTR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDPTR[31:16]															
Type	RO															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDPTR[15:0]															
Type	RO															

Note that n is from 12 to 17.

RDPTR Virtual FIFO Read Pointer.

0x8102_0n38h DMA Channel n Virtual FIFO Data Count Register DMAn_FFCNT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FFCNT															
Type	RO															

Note that n is from 12 to 17.

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FFCNT To display the number of data stored in FIFO. 0 means FIFO empty, and FIFO is full if FFCNT is equal to FFSIZE.

0x8102_0n3Ch DMA Channel n Virtual FIFO Status Register DMAn_FFSTA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														ALT	EMPTY	FULL
Type														RO	RO	RO
Reset														1	1	1

Note that n is from 12 to 17.

FULL To indicate FIFO is full.

- **0** Not Full
- **1** Full

EMPTY To indicate FIFO is empty.

- **0** Not Empty
- **1** Empty

ALT To indicate FIFO Count is larger than ALTLEN. DMA issues an alert signal to UART to enable UART flow control.

- **0** Not reach alert region.
- **1** Reach alert region.

0x8102_0n40h DMA Channel n Virtual FIFO Alert Length Register DMAn_ALTLEN

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ALTLEN					
Type											R/W					
Reset											0					

Note that n is from 12 to 17.

ALTLEN Specifies the Alert Length of Virtual FIFO DMA. Once the remaining FIFO space is less than ALTLEN, an alert signal is issued to UART to enable flow control. Normally, ALTLEN shall be larger than 16 for UART application.

0x8102_0n44h DMA Channel n Virtual FIFO Size Register DMAn_FFSIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FFSIZE															
Type	R/W															
Reset	0															

Note that n is from 12 to 17.

FFSIZE Specifies the FIFO Size of Virtual FIFO DMA.

3.5 Code Cache controller

3.5.1 General Description

A new subsystem consisting of cache and TCM (tightly coupled memory) will be implemented in MT6253. This subsystem is placed between MCU core and AHB bus interface, as shown in **Figure 15**.

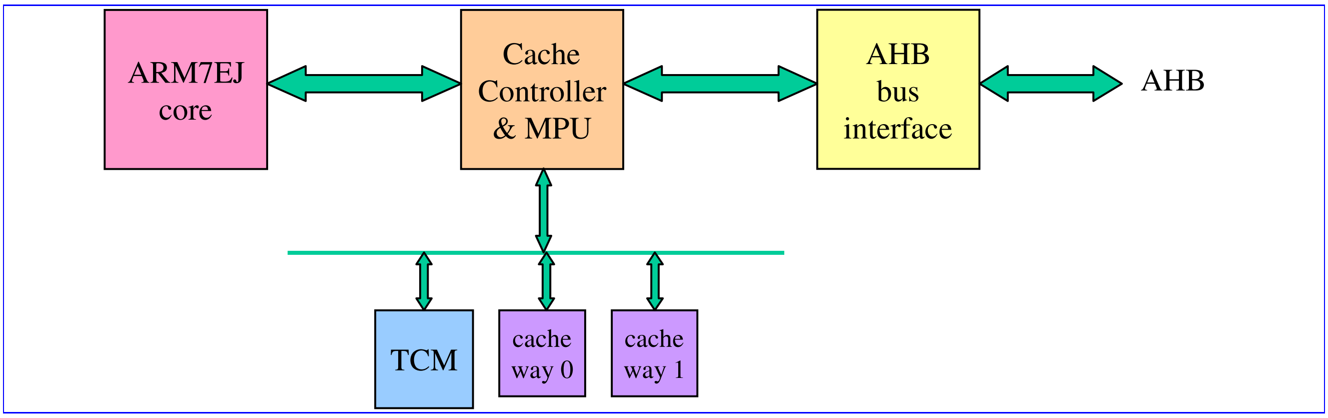

Figure 15 Cache and TCM subsystem

TCM is a high-speed (zero wait state) dedicated memory accessed by MCU exclusively. Because MCU can run at 104MHz and on-chip bus runs at maximum 52MHz, there will be latency penalty when MCU accesses memory or peripherals through on-chip bus. By moving timing critical code and data into TCM, MCU performance can be increased and the response to particular events can be guaranteed.

Another method to increase MCU performance is the introduction of cache. Cache is a small memory, keeping the copy of external memory. If MCU reads a cacheable data, the data will be copied to cache. Once MCU needs the same data later, it can get it directly from cache (called cache hit) instead of from external memory, which takes long time compared to high-speed (zero wait state) cache memory.

Since a large external memory maps to a small cache, cache can hold only a small portion of external memory. If MCU accesses a data not found in cache (called cache miss), some contents of cache must be dropped (flushed) and the required data is transferred from external memory (called cache line fill) and stored to cache. On the other hand, TCM is not the copy of anything else. The best way to use TCM is to put critical code/data in TCM in the memory usage plan. After power

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on reset, the boot loader copies TCM contents from external storage (such like flash) to internal TCM. If necessary, MCU can replace a portion of TCM content with other data on external storage in the runtime to implement a mechanism such like “overlay”. TCM is also an ideal place to put stack data.

The sizes of TCM and cache can be set to one of 3 configurations:

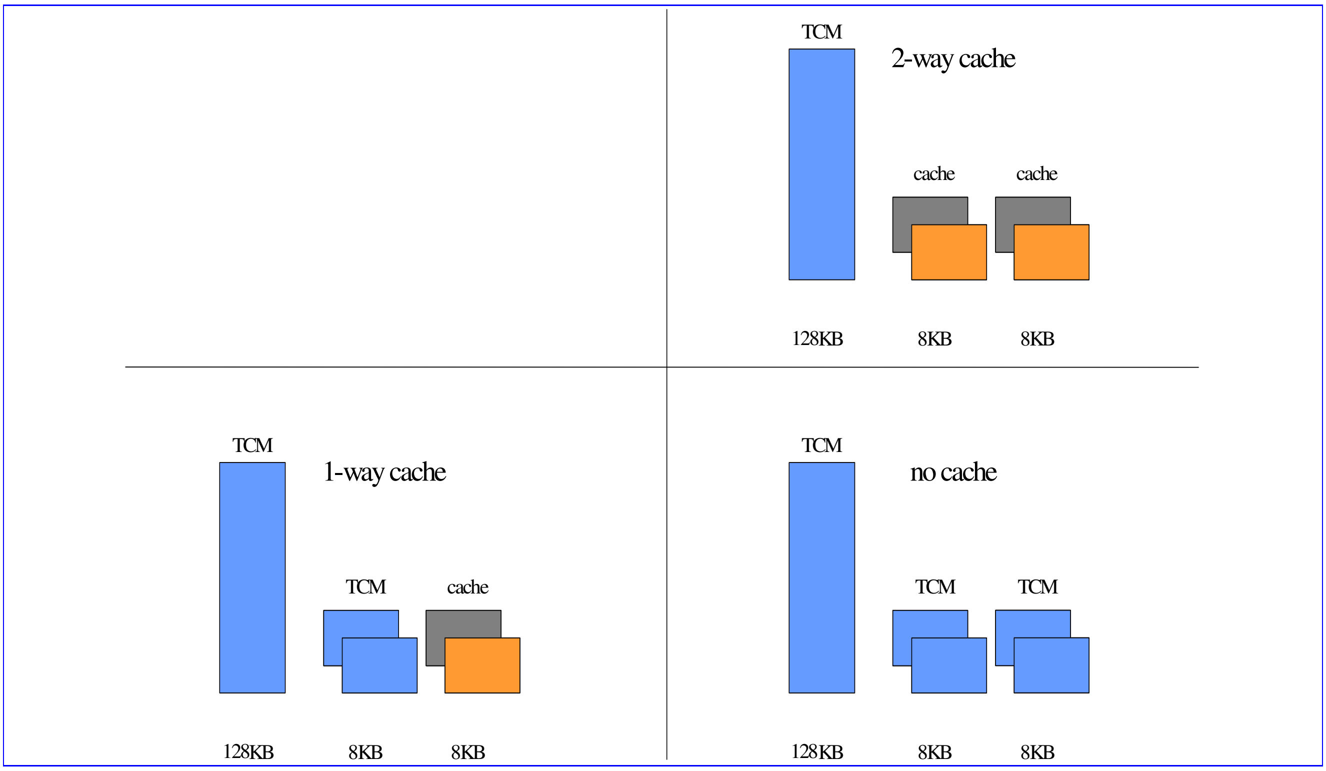

Figure 16 Configurations of TCM and cache

- 128KB TCM, 16KB cache
- 136KB TCM, 8KB cache
- 144KB TCM, 0KB cache

These configurations provide flexibility for software to adjust for optimum system performance.

The address mapping of these memories is like the following:

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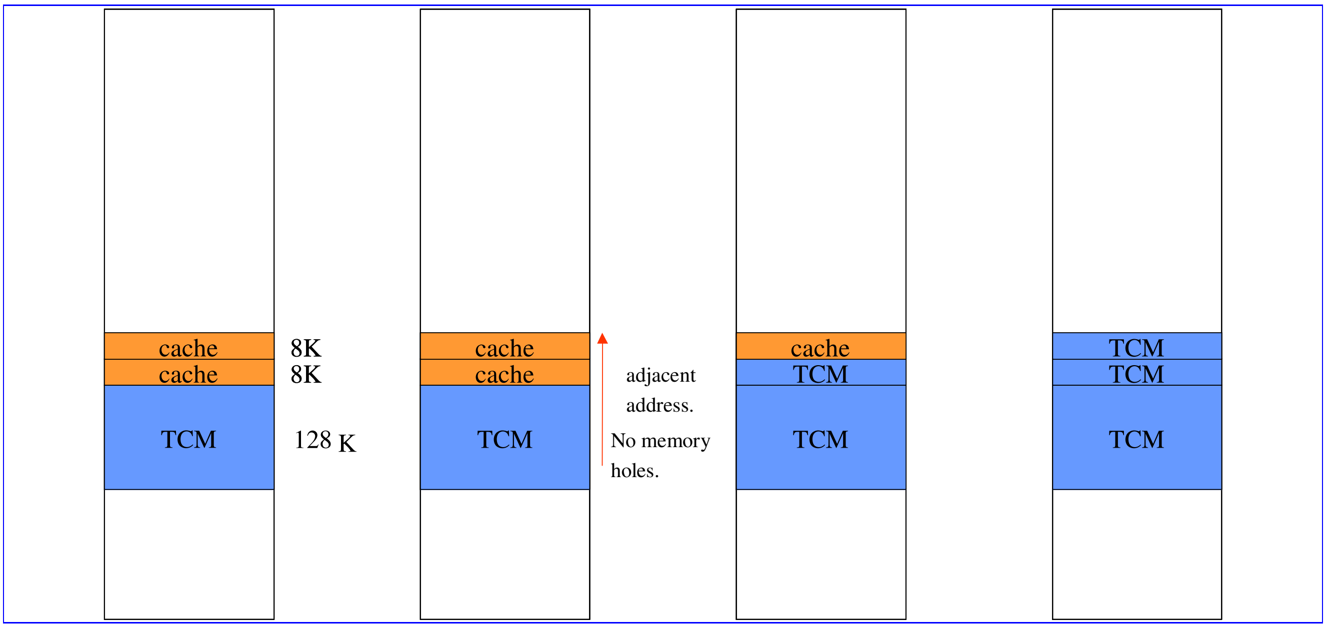

Figure 17 Memory mapping of TCM and cache

In **Figure 17**, MCU could only access TCM explicitly. Cache is transparent to MCU.

3.5.2 Organization of Cache

The cache system has the following features:

- Write through (no write allocation)
- Configurable 1/2 way set associative (8K/16K)
- Each way has 256 cache lines with 8 word line size (256*8*4=8KB)
- 19-bit tag address and 1 valid bit for each cache line.

One way of cache comprises of two memory: tag memory and data memory. Tag memory stores each line's valid bit, dirty bit and tag (upper part of address). Data memory stores line data. When MCU accesses memory, the address is compared to the contents of tag memory. First the line index (address bit [12:5]) is used to locate a line, and then the tag of the line is compared to upper part of address (bit [31:13]). If two parts match and valid bit is 1, it is said a cache hit and data from that particular way is sent back to MCU. This process is illustrated in the following figure:

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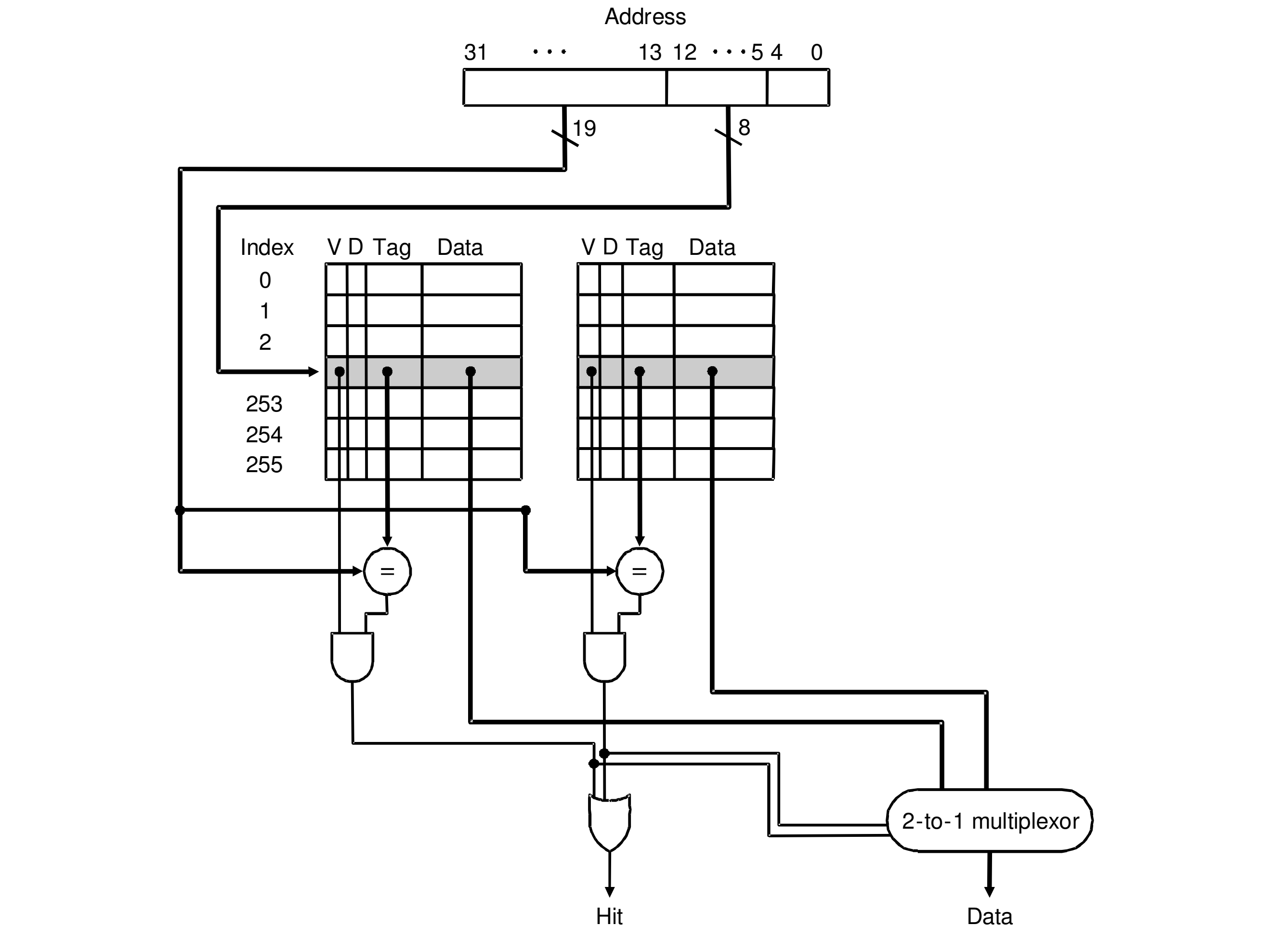

Figure 18 Tag comparison of 2-way cache

If most memory accesses are cache hit, MCU could get data immediately without wait states and the overall system performance is higher. There are several factors that may affect cache hit rate:

- Cache size and the organization

  The larger the cache size is, the higher the hit rate is. But the hit rate starts to saturate when cache size is larger than a threshold size. Normally the size of 16KB and above and two or four way can achieve a good hit rate.

- Program behavior

  If the system has several numbers of tasks that switch fast, it may cause cache contents to flush frequently. Because each time a new task is run, the cache will hold its data after some time. If next task uses data in the memory that occupy the same cache entries as previous task, it will cause cache contents to be flushed to store data of the new task. Interrupts also cause program flow to change dynamically. The interrupt handler code itself and

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the data it processes may cause cache to flush some data used by current task. Thus after exiting interrupt handler and returning to current task, the flushed data may need to be filled to cache again, resulting performance degradation.

To help software engineer tune system performance, the cache controller in MT6253 records the numbers of cache hit count and cacheable memory accesses. Cache hit rate can be obtained from these two numbers.

The cache sub system also has a module called MPU (memory protection unit). MPU can prevent illegal memory accesses and specify which memory region is cacheable or non-cacheable. Two fields in CACHE_CON register control the enable of MPU functions. MPU has its own registers to define memory region and associated regions. These settings only take effect after the enable bits in CACHE_CON are set to 1. For more details on the settings, please refer to MPU part of the specification.

3.5.3 Cache Operations

Upon power on, cache memory contains random numbers and can't be used by MCU. Therefore MCU must have some means to "clean" cache memory before enabling them. Both above cases need a mechanism for MCU to perform operations on cache. The cache controller provides a register which, when written, could do operations on cache memory. These are called cache operations, including

- Invalidate one cache line

  The user must give a memory address. If it is found within cache, that particular line is invalidated (clear valid bit to 0). Alternatively, the user can specify which set/way of cache to be invalidated.

- Invalidate all cache lines

  The user needs not to specify an address. The cache controller hardware automatically clears valid bits in each tag memory.

3.5.4 Cache Controller Register Definition

CACHE base address is assumed 0x8500_0000 (subject to change).

0x8500_0000 Cache General Control Register CACHE_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							CACHESIZE						CNTEN1	CNTEN0	MPEN	MCEN
Type							RW						RW	RW	R/W	R/W
Reset							00						0	0	0	0

This register determines the cache size, cache hit counter and the enable of MPU.

CACHESIZE Cache Size Select

00 no cache (144KB TCM)

01 8KB, 1-way cache (136KB TCM)

10 16KB, 2-way cache (128KB TCM)

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CNTEN1 Enable cache hit counter 1

If enabled, cache controller will increase a 48-bit counter each time a cache hit occurs. This number can provide a reference of performance measurement for tuning of application programs. This counter increments only when the cacheable information is from MPU cacheable region 8~15.

0 disable

1 enable

CNTEN0 Enable cache hit counter 0

If enabled, cache controller will increase a 48-bit counter each time a cache hit occurs. This number can provide a reference of performance measurement for tuning of application programs. This counter increments only when the cacheable information is from MPU cacheable region 0~7.

0 disable

1 enable

MPEN Enable MPU comparison of read/write permission setting

If disabled, MCU could access any memory without any restriction. If enabled, MPU would compare the address of MCU to its setting. If an address falls into a restricted region, MPU would stop this memory access and send "ABORT" signal to MCU. Please refer to MPU part of the specification for more details.

0 disable

1 enable

MCEN Enable MPU comparison of cacheable/non-cacheable setting

If disabled, MCU memory accesses are all non-cacheable, i.e., they will go through AHB bus (except for TCM). If enabled, the setting in MPU will take effect. If MCU accesses a cacheable memory region, the cache controller will return the data in cache if it's found in cache, and will get the data through AHB bus only if a cache miss occurs. Please refer to MPU part of the specification for more details.

0 disable

1 enable

0x8500_0004 Cache Operation CACHE_OP

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TADDR[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TADDR[15:5]											OP[3:0]				EN
Type	R/W											W				W1
Reset	0											0				0

This register defines the address and/or which kinds of cache operations to be taken. When MCU writes this register, the pipeline of MCU will be stopped for the cache controller to complete the operation. Bit 0 of the register must be written 1 to enable the command.

TADDR[31:5] Target Address

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This field contains the address of invalidation operation. If OP[3:0]=0010, TADDR[31:5] is the address[31:5] of a memory whose line will be invalidated if it exists in the cache. If OP[3:0]=0100, TADDR[12:5] indicates the set, while TADDR[19:16] indicates which way to clear:

0001 way #0
0010 way #1
0100 way #2
1000 way #3

OP[3:0] Operation
This field determines which cache operations will be performed.

0001 invalidate all cache lines
0010 invalidate one cache line using address
0100 invalidate one cache line using set/way

EN Enable command
This enable bit must be written 1 to enable the command.

1 enable
0 not enable

0x8500_0008 Cache Hit Count 0 Lower Part CACHE_HCNT0L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHIT_CNT0[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHIT_CNT0[15:0]															
Type	R/W															
Reset	0															

0x8500_000C Cache Hit Count 0 Upper Part CACHE_HCNT0U

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVED															
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHIT_CNT0[47:32]															
Type	R/W															
Reset	0															

When CNTEN0 bit in CACHE_CON register is set to 1 (enabled), this register starts to record cache hit count until it is disabled. If the value increases to over maximum value (0xffffffffffff), it will be rolled over to 0 and continue counting. The 48 bit counter can provide a recording time of 31 days even if MCU runs at 104MHz and every cycle is a cache hit.

Note that before enabling the counter, it is recommended to write the initial value of zero to the counter.

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CHIT_CNT0[47:0] Cache Hit Count 0

WRITE writing any value to CACHE_HCNT0L or CACHE_HCNT0U clears CHIT_CNT0 to all zeros

READ current counter value

0x8500_0010 Cacheable Access Count 0 Lower Part — CACHE_CCNT0L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CACC_CNT0[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CACC_CNT0[15:0]															
Type	R/W															
Reset	0															

0x8500_0014 Cacheable Access Count 0 Upper Part — CACHE_CCNT0U

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVED															
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CACC_CNT0[47:32]															
Type	R/W															
Reset	0															

When CNTEN0 bit in CACHE_CON register is set to 1 (enabled), this register is incremented at each cacheable memory access (no matter it's a cache miss or a cache hit). If the value increases to over maximum value (0xffffffffffff), it will be rolled over to 0 and continue counting. For 104MHz MCU speed, if all memory accesses are cacheable and cache hit, this counter will overflow after (2^48) * 9.6ns = 31 days. This is the shortest time for the counter to overflow. In a more realistic case, the system will have cache misses, non-cacheable accesses, idle mode that makes the counter overflow at later time.

CACC_CNT0[47:0] Cache Access Count 0

WRITE writing any value to CACHE_CCNT0L or CACHE_CCNT0U clears CACC_CNT0 to all zeros

READ current counter value

The best way to use CACHE_HCNT0 and CACHE_CCNT0 is to set zero as initial value in both registers, enable both counters (set CNTEN0 to 1), run a portion of program to be benchmarked, stop the counters and get their values. Therefore during this period

$$Cache\ hit\ rate = \frac{CACHE_HCNT}{CACHE_CCNT} \times 100\% .$$

The cache hit rate value may help tune the performance of application program.

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Note that CHIT_CNT0 and CACC_CNT0 only increment if the cacheable attribute is defined in MPU cacheable region 0~7.

0x8500_0018 Cache Hit Count 1 Lower Part CACHE_HCNT1L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHIT_CNT1[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHIT_CNT1[15:0]															
Type	R/W															
Reset	0															

0x8500_001C Cache Hit Count 1 Upper Part CACHE_HCNT1U

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVED															
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHIT_CNT1[47:32]															
Type	R/W															
Reset	0															

When CNTEN1 bit in CACHE_CON register is set to 1 (enabled), this register starts to record cache hit count until it is disabled. If the value increases to over maximum value (0xffffffffffff), it will be rolled over to 0 and continue counting. The 48 bit counter can provide a recording time of 31 days even if MCU runs at 104MHz and every cycle is a cache hit.

Note that before enabling the counter, it is recommended to write the initial value of zero to the counter.

CHIT_CNT1[47:0] Cache Hit Count

WRITE writing any value to CACHE_HCNT1L or CACHE_HCNT1U clears CHIT_CNT1 to all zeros

READ current counter value

0x8500_0020 Cacheable Access Count 1 Lower Part CACHE_CCNT1L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CACC_CNT1[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CACC_CNT1[15:0]															
Type	R/W															
Reset	0															

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0x8500_0024 Cacheable Access Count 1 Upper Part CACHE_CCNT1U

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVED															
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CACC_CNT1[47:32]															
Type	R/W															
Reset	0															

When CNTEN1 bit in CACHE_CON register is set to 1 (enabled), this register is incremented at each cacheable memory access (no matter it's a cache miss or a cache hit). If the value increases to over maximum value (0xffffffffffff), it will be rolled over to 0 and continue counting. For 104MHz MCU speed, if all memory accesses are cacheable and cache hit, this counter will overflow after (2^48) * 9.6ns = 31 days. This is the shortest time for the counter to overflow. In a more realistic case, the system will have cache misses, non-cacheable accesses, idle mode that makes the counter overflow at later time.

CACC_CNT1[47:0] Cache Access Count 1

WRITE writing any value to CACHE_CCNT1L or CACHE_CCNT1U clears CACC_CNT1 to all zeros

READ current counter value

The best way to use CACHE_HCNT1 and CACHE_CCNT1 is to set zero as initial value in both registers, enable both counters (set CNTEN1 to 1), run a portion of program to be benchmarked, stop the counters and get their values. Therefore during this period

$$Cache\ hit\ rate = \frac{CACHE_HCNT}{CACHE_CCNT} \times 100\% .$$

The cache hit rate value may help tune the performance of application program.

Note that CHIT_CNT1 and CACC_CNT1 only increment if the cacheable attribute is defined in MPU cacheable region 7~15.

3.6 Interrupt Controller

3.6.1 General Description

Figure 19 outlines the major functionality of the MCU Interrupt Controller. The interrupt controller processes all interrupt sources coming from external lines and internal MCU peripherals. Since ARM7EJ-S core supports two levels of interrupt latency, this controller generates two request signals: FIQ for fast, low latency interrupt request and IRQ for more general interrupts with lower priority.

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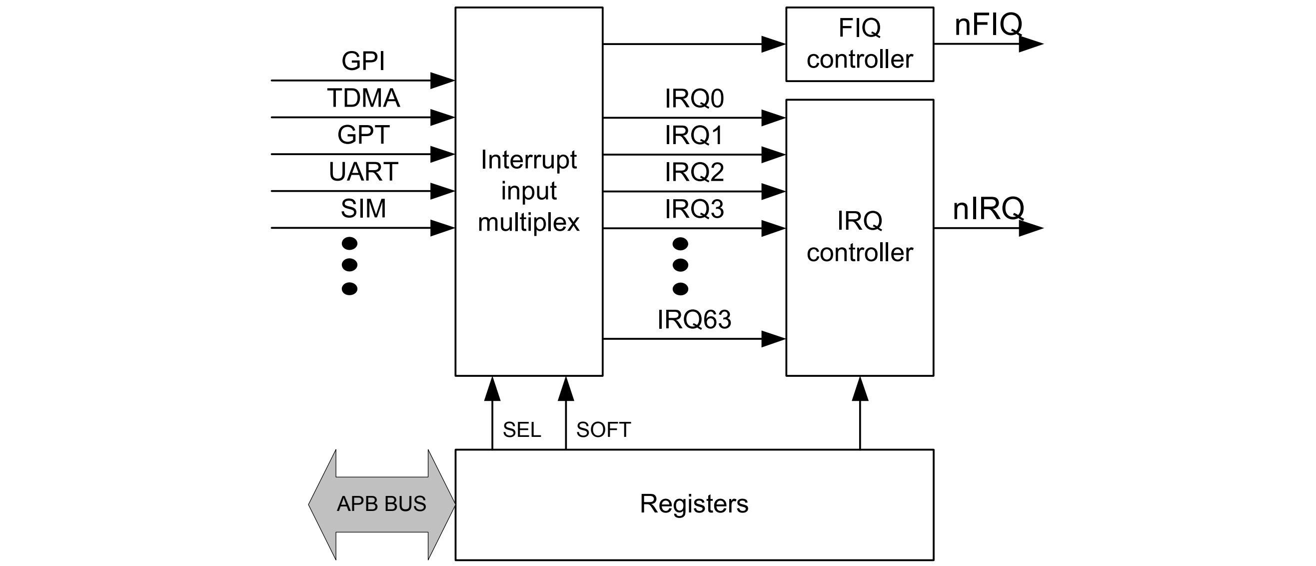

Figure 20 Block Diagram of the Interrupt Controller

One and only one of the interrupt sources can be assigned to FIQ Controller and have the highest priority in requesting timing critical service. All the others share the same IRQ signal by connecting them to IRQ Controller. The IRQ Controller manages up 64 interrupt lines of IRQ0 to IRQ63 with fixed priority in descending order.

The Interrupt Controller provides a simple software interface by mean of registers to manipulate the interrupt request shared system. IRQ Selection Registers and FIQ Selection Register determine the source priority and connecting relation among sources and interrupt lines. IRQ Source Status Register allows software program to identify the source of interrupt that generates the interrupt request. IRQ Mask Register provides software to mask out undesired sources some time. End of Interrupt Register permits software program to indicate to the controller that a certain interrupt service routine has been finished.

Binary coded version of IRQ Source Status Register is also made available for software program to helpfully identify the interrupt source. Note that while taking advantage of this feature, it should also take the binary coded version of End of Interrupt Register coincidently.

The essential Interrupt Table of ARM7EJ-S core is shown as Table **9**.

Address	Description
00000000h	System Reset
00000018h	IRQ
0000001Ch	FIQ

Table 10 Interrupt Table of ARM7EJ-S

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3.6.1.1 Interrupt Source Masking

Interrupt controller provides the function of Interrupt Source Masking by the way of programming MASK register. Any of them can be masked individually.

However, because of the bus latency, the masking takes effect no earlier than 3 clock cycles later. In this time, the to-be-masked interrupts could come in and generate an IRQ pulse to MCU, and then disappear immediately. This IRQ forces MCU going to Interrupt Service Routine and polling Status Register (IRQ_STA2), but the register shows there is no interrupt. This might cause MCU malfunction.

There are two ways for programmer to protect their software.

1. Return from ISR (Interrupt Service Routine) immediately while the Status register shows no interrupt.
2. Set I bit of MCU before doing Interrupt Masking, and then clear it after Interrupt Masking done.

Both avoid the problem, but the first item is recommended in the ISR.

3.6.1.2 External Interrupt

This interrupt controller also integrates an External Interrupt Controller that can support up to 7 interrupt requests coming from external sources, the EINT0~6, and 7 WakeUp interrupt requests, i.e. EINT7~13, coming from peripherals used to inform system to resume the system clock. EINT0~EINT6 interrupt source can be configured as from external pin or internal peripherals.

The external interrupts can be used for different kind of applications, mainly for event detections: detection of hand free connection, detection of hood opening, detection of battery charger connection.

Since the external event may be unstable in a certain period, a de-bounce mechanism is introduced to ensure the functionality. The circuitry is mainly used to verify that the input signal remains stable for a programmable number of periods of the clock. When this condition is satisfied, for the appearance or the disappearance of the input, the output of the de-bounce logic changes to the desired state. Note that, because it uses the 32768Hz slow clock for performing the de-bounce process, the parameter of de-bounce period and de-bounce enable takes effect no sooner than one 32768Hz clock cycle (~30.52us) after the software program sets them. When the sources of External Interrupt Controller are used to resume the system clock in sleep mode, the de-bounce mechanism must be enabled. However, the polarities of EINTs are clocked with the system clock. Any changes to them take effect immediately.

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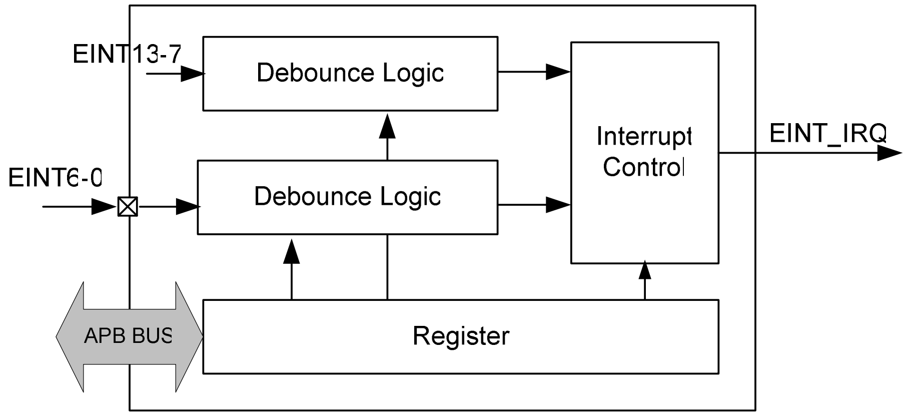

Figure 21 Block Diagram of External Interrupt Controller

3.6.1.3 External Interrupt Input Pins

EINT	Edge / Level HW Debounce	SOURCE PIN	SUPPLEMENT
EINT0	Edge / Level Yes	if(GPIO64_M==1) then EINT0=GPIO64 else EINT0=1	1. GPIOs should be in the input mode and are effected by GPIO data input inversion registers. 2. GPIOxx_M is the GPIO mode control registers, please refer to GPIO segment.
EINT1	Edge / Level Yes	if(GPIO63_M==1) then EINT1=GPIO63 else EINT1=1	
EINT2	Edge / Level Yes	if(GPIO62_M==1) then EINT2=GPIO62 else EINT2=1	
EINT3	Edge / Level Yes	if(GPIO61_M==1) then EINT3=GPIO62 else EINT3=1	
EINT4	Edge / Level Yes	if(GPIO1_M==2) then EINT4=GPIO1 else EINT4=1	
EINT5	Edge / Level Yes	if(GPIO8_M==2) then EINT5=GPIO8 else EINT5=1	
EINT6	Edge / Level Yes	if(GPIO76_M==2) then EINT6=GPIO76 else EINT6=1	
EINT7	Edge / Level Yes	Charger detect interrupt (Active low)	
EINT8	Edge / Level Yes	PMU OC interrupt (Active low)	
EINT9	Edge / Level Yes	PMU OV protection interrupt (Active low)	
EINT10	Edge / Level Yes	Reserved	
EINT11	Edge / Level Yes	Reserved	
EINT12	Edge / Level Yes	Reserved	
EINT13	Edge / Level Yes	Reserved	

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REGISTER ADDRESS	REGISTER NAME	SYNONYM
0x8101_0000h	IRQ Selection 0 Register	IRQ_SEL0
0x8101_0004h	IRQ Selection 1 Register	IRQ_SEL1
0x8101_0008h	IRQ Selection 2 Register	IRQ_SEL2
0x8101_000ch	IRQ Selection 3 Register	IRQ_SEL3
0x8101_0010h	IRQ Selection 4 Register	IRQ_SEL4
0x8101_0014h	IRQ Selection 5 Register	IRQ_SEL5
0x8101_0018h	IRQ Selection 6 Register	IRQ_SEL6
0x8101_001ch	IRQ Selection 7 Register	IRQ_SEL7
0x8101_0020h	IRQ Selection 8 Register	IRQ_SEL8
0x8101_0024h	IRQ Selection 9 Register	IRQ_SEL9
0x8101_0028h	IRQ Selection 10 Register	IRQ_SEL10
0x8101_002ch	IRQ Selection 11 Register	IRQ_SEL11
0x8101_0030h	IRQ Selection 12 Register	IRQ_SEL12
0x8101_0034h	IRQ Selection 13 Register	IRQ_SEL13
0x8101_0038h	IRQ Selection 14 Register	IRQ_SEL14
0x8101_003ch	IRQ Selection 15 Register	IRQ_SEL15
0x8101_006ch	FIQ Selection Register	FIQ_SEL
0x8101_0070h	IRQ Mask Register (low)	IRQ_MASKL
0x8101_0074h	IRQ Mask Register (high)	IRQ_MASKH
0x8101_0080h	IRQ Mask Clear Register (low)	IRQ_MASK_CLRL
0x8101_0084h	IRQ Mask Clear Register (high)	IRQ_MASK_CLRH
0x8101_0090h	IRQ Mask Set Register (low)	IRQ_MASK_SETL
0x8101_0094h	IRQ Mask Set Register (high)	IRQ_MASK_SETH
0x8101_00a0h	IRQ End of Interrupt Register (low)	IRQ_EOIL
0x8101_00a4h	IRQ End of Interrupt Register (high)	IRQ_EOIH
0x8101_00b0h	IRQ Sensitive Register (low)	IRQ_SENSL
0x8101_00b4h	IRQ Sensitive Register (high)	IRQ_SENSH
0x8101_00c0h	IRQ Software Interrupt Register (low)	IRQ_SOFTL
0x8101_00c4h	IRQ Software Interrupt Register (high)	IRQ_SOFTH
0x8101_00d0h	FIQ Control Register	FIQ_CON
0x8101_00d4h	FIQ End of Interrupt Register	FIQ_EOI
0x8101_00d8h	Binary Coded Value of IRQ_STATUS	IRQ_STA2
0x8101_00dch	Binary Coded Value of IRQ_EOI	IRQ_EOI2
0x8101_0100h	EINT Status Register	EINT_STA

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0x8101_0104h	EINT Mask Register	EINT_MASK
0x8101_0108h	EINT Mask Clear Register	EINT_MASK_CLR
0x8101_010ch	EINT Mask Set Register	EINT_MASK_SET
0x8101_0110h	EINT Interrupt Acknowledge Register	EINT_INTACK
0x8101_0114h	EINT Sensitive Register	EINT_SENS
0x8101_0118h	EINT Software Interrupt Register	EINT_SOFT
0x8101_0120h	EINT0 De-bounce Control Register	EINT0_CON
0x8101_0130h	EINT1 De-bounce Control Register	EINT1_CON
0x8101_0140h	EINT2 De-bounce Control Register	EINT2_CON
0x8101_0150h	EINT3 De-bounce Control Register	EINT3_CON
0x8101_0160h	EINT4 De-bounce Control Register	EINT4_CON
0x8101_0170h	EINT5 De-bounce Control Register	EINT5_CON
0x8101_0180h	EINT6 De-bounce Control Register	EINT6_CON
0x8101_0190h	EINT7 De-bounce Control Register	EINT7_CON
0x8101_01a0h	EINT8 De-bounce Control Register	EINT8_CON
0x8101_01b0h	EINT9 De-bounce Control Register	EINT9_CON
0x8101_01c0h	EINT10 De-bounce Control Register	EINT10_CON
0x8101_01d0h	EINT11 De-bounce Control Register	EINT11_CON
0x8101_01e0h	EINT12 De-bounce Control Register	EINT12_CON
0x8101_01f0h	EINT13 De-bounce Control Register	EINT13_CON

Table 11 Interrupt Controller Register Map

3.6.2 Register Definitions

0x8101_0000 IRQ Selection 0 Register IRQ_SEL0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ3								IRQ2					
Type			R/W								R/W					
Reset			3								2					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ1								IRQ0					
Type			R/W								R/W					
Reset			1								0					

0x8101_0004 IRQ Selection 1 Register IRQ_SEL1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ7								IRQ6					
Type			R/W								R/W					
Reset			7								6					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name			IRQ5								IRQ4					
Type			R/W								R/W					
Reset			5								4					

0x8101_0008 IRQ Selection 2 Register IRQ_SEL2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQB								IRQA					
Type			R/W								R/W					
Reset			0xb								0xa					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ9								IRQ8					
Type			R/W								R/W					
Reset			9								8					

0x8101_000c IRQ Selection 3 Register IRQ_SEL3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQF								IRQE					
Type			R/W								R/W					
Reset			0xf								0xe					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQD								IRQC					
Type			R/W								R/W					
Reset			0xd								0xc					

0x8101_0010 IRQ Selection 4 Register IRQ_SEL4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ13								IRQ12					
Type			R/W								R/W					
Reset			0x13								0x12					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ11								IRQ10					
Type			R/W								R/W					
Reset			0x11								0x10					

0x8101_0014 IRQ Selection 5 Register IRQ_SEL5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ17								IRQ16					
Type			R/W								R/W					
Reset			0x17								0x16					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ15								IRQ14					
Type			R/W								R/W					
Reset			0x15								0x14					

0x8101_0018 IRQ Selection 6 Register IRQ_SEL6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ1B								IRQ1A					
Type			R/W								R/W					
Reset			0x1b								0x1a					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name			IRQ19								IRQ18					
Type			R/W								R/W					
Reset			0x19								0x18					

0x8101_001c IRQ Selection 7 Register IRQ_SEL7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ1F								IRQ1E					
Type			R/W								R/W					
Reset			0x1f								0x1e					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ1D								IRQ1C					
Type			R/W								R/W					
Reset			0x1d								0x1c					

0x8101_0020 IRQ Selection 8 Register IRQ_SEL8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ23								IRQ22					
Type			R/W								R/W					
Reset			0x23								0x22					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ21								IRQ20					
Type			R/W								R/W					
Reset			0x21								0x20					

0x8101_0024 IRQ Selection 9 Register IRQ_SEL9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ27								IRQ26					
Type			R/W								R/W					
Reset			0x27								0x26					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ25								IRQ24					
Type			R/W								R/W					
Reset			0x25								0x24					

0x8101_0028 IRQ Selection 10 Register IRQ_SEL10

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ2B								IRQ2A					
Type			R/W								R/W					
Reset			0x2b								0x2a					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ29								IRQ28					
Type			R/W								R/W					
Reset			0x29								0x28					

0x8101_002c IRQ Selection 11 Register IRQ_SEL11

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ2F								IRQ2E					
Type			R/W								R/W					
Reset			0x2f								0x2e					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name			IRQ2D								IRQ2C					
Type			R/W								R/W					
Reset			0x2d								0x2c					

0x8101_0030 IRQ Selection 12 Register IRQ_SEL12

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ33								IRQ32					
Type			R/W								R/W					
Reset			0x33								0x32					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ31								IRQ30					
Type			R/W								R/W					
Reset			0x31								0x30					

0x8101_0034 IRQ Selection 13 Register IRQ_SEL13

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ37								IRQ36					
Type			R/W								R/W					
Reset			0x37								0x36					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ35								IRQ34					
Type			R/W								R/W					
Reset			0x35								0x34					

0x8101_0038 IRQ Selection 14 Register IRQ_SEL14

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ3B								IRQ3A					
Type			R/W								R/W					
Reset			0x3b								0x3a					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ39								IRQ38					
Type			R/W								R/W					
Reset			0x39								0x38					

0x8101_003c IRQ Selection 15 Register IRQ_SEL15

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ3F								IRQ3E					
Type			R/W								R/W					
Reset			0x3f								0x3e					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ3D								IRQ3C					
Type			R/W								R/W					
Reset			0x3d								0x3c					

0x8101_006c FIQ Selection Register FIQ_SEL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name							FIQ
Type							R/W
Reset							0

The IRQ/FIQ Selection Registers provide system designers with a flexible routing scheme to make various mappings of priority among interrupt sources possible. The registers allow the interrupt sources to be mapped onto interrupt requests of either FIQ or IRQ. While only one interrupt source can be assigned to FIQ, the other ones share IRQs by mapping them onto IRQ0 to IRQ1F connected to IRQ controller. The priority sequence of IRQ0~IRQ3F is fixed, i.e. IRQ0 > IRQ1 > IRQ2 > … > IRQ1E > IRQ3F. During the software configuration process, the Interrupt Source Code of desired interrupt source should be written into source field of the corresponding IRQ_SEL0-IRQ_SEL15/FIQ_SEL. 6-bit Interrupt Source Codes for all interrupt sources are fixed and defined.

Interrupt Source	STA2 (Hex)	STA
GPI_FIQ	0	00000001
TDMA_CTIRQ1	1	00000002
TDMA_CTIRQ2	2	00000004
DSP12CPU	3	00000008
SIM	4	00000010
DMA	5	00000020
TDMA	6	00000040
UART1	7	00000080
KP	8	00000100
UART2	9	00000200
GPTimer	A	00000400
EINT	B	00000800
USB	C	00001000
MSDC	D	00002000
RTC	E	00004000
IRDA	F	00008000
LCD	10	00010000
UART3	11	00020000
GPI	12	00040000
WDT	13	00080000
DSP22CPU	14	00100000
RESIZER	15	00200000
NFI	16	00400000
USB1	17	00800000
IRDBG1	18	01000000
MSDC_CD	19	02000000

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I2C	1A	04000000
IRDBG2	1B	08000000
SIM2	1C	10000000
SWDBG	1D	20000000
CAM	1E	40000000
Touch Panel	1F	80000000
Sysram/rom	20	100000000
Reserved	21~3F	

Table 12 Interrupt Source Code for Interrupt Sources

FIQ, IRQ0-1F The 6-bit content of this field corresponds to an Interrupt Source Code shown above.

0x8101_0070 IRQ Mask Register (low) IRQ_MASKL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F	IRQ1E	IRQ1D	IRQ1C	IRQ1B	IRQ1A	IRQ19	IRQ18	IRQ17	IRQ16	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF	IRQE	IRQD	IRQC	IRQB	IRQA	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

0x8101_0074 IRQ Mask Register (high) IRQ_MASKH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ3F	IRQ3E	IRQ3D	IRQ3C	IRQ3B	IRQ3A	IRQ39	IRQ38	IRQ37	IRQ36	IRQ35	IRQ34	IRQ33	IRQ32	IRQ31	IRQ30
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ2F	IRQ2E	IRQ2D	IRQ2C	IRQ2B	IRQ2A	IRQ29	IRQ28	IRQ27	IRQ26	IRQ25	IRQ24	IRQ23	IRQ22	IRQ21	IRQ20
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

This register contains a mask bit for each interrupt line in IRQ Controller. The register allows each interrupt source IRQ0 to IRQ3F to be disabled or masked separately under software control. After a system reset, all bit values are set to 1 to indicate that interrupt requests are prohibited.

IRQ0-3F Mask control for the associated interrupt source in the IRQ controller

0 Interrupt is enabled

1 Interrupt is disabled

0x8101_0080 IRQ Mask Clear Register (low) IRQ_MASK_CLRL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F	IRQ1E	IRQ1D	IRQ1C	IRQ1B	IRQ1A	IRQ19	IRQ18	IRQ17	IRQ16	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10

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Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF	IRQE	IRQD	IRQC	IRQB	IRQA	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C

0x8101_0084 IRQ Mask Clear Register (high) IRQ_MASK_CLRH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ3F	IRQ3E	IRQ3D	IRQ3C	IRQ3B	IRQ3A	IRQ39	IRQ38	IRQ37	IRQ36	IRQ35	IRQ34	IRQ33	IRQ32	IRQ31	IRQ30
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ2F	IRQ2E	IRQ2D	IRQ2C	IRQ2B	IRQ2A	IRQ29	IRQ28	IRQ27	IRQ26	IRQ25	IRQ24	IRQ23	IRQ22	IRQ21	IRQ20
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C

This register is used to clear bits in IRQ Mask Register. When writing to this register, the data bits that are HIGH cause the corresponding bits in IRQ Mask Register to be cleared. Data bits that are LOW have no effect on the corresponding bits in IRQ Mask Register.

IRQ0-3F Clear corresponding bits in IRQ Mask Register.

- **0** No effect
- **1** Disable the corresponding MASK bit

0x8101_0090 IRQ Mask SET Register (low) IRQ_MASK_SETL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F	IRQ1E	IRQ1D	IRQ1C	IRQ1B	IRQ1A	IRQ19	IRQ18	IRQ17	IRQ16	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10
Type	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF	IRQE	IRQD	IRQC	IRQB	IRQA	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
Type	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S

0x8101_0094 IRQ Mask SET Register (high) IRQ_MASK_SETH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ3F	IRQ3E	IRQ3D	IRQ3C	IRQ3B	IRQ3A	IRQ39	IRQ38	IRQ37	IRQ36	IRQ35	IRQ34	IRQ33	IRQ32	IRQ31	IRQ30
Type	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ2F	IRQ2E	IRQ2D	IRQ2C	IRQ2B	IRQ2A	IRQ29	IRQ28	IRQ27	IRQ26	IRQ25	IRQ24	IRQ23	IRQ22	IRQ21	IRQ20
Type	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S

This register is used to set bits in the IRQ Mask Register. When writing to this register, the data bits that are HIGH cause the corresponding bits in IRQ Mask Register to be set. Data bits that are LOW have no effect on the corresponding bits in IRQ Mask Register.

IRQ0-3F Set corresponding bits in IRQ Mask Register.

- **0** No effect
- **1** Enable corresponding MASK bit

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0x8101_00a0 IRQ End of Interrupt Register (low) IRQ_EOIL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F	IRQ1E	IRQ1D	IRQ1C	IRQ1B	IRQ1A	IRQ19	IRQ18	IRQ17	IRQ16	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF	IRQE	IRQD	IRQC	IRQB	IRQA	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8101_00a4 IRQ End of Interrupt Register (high) IRQ_EOIH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ3F	IRQ3E	IRQ3D	IRQ3C	IRQ3B	IRQ3A	IRQ39	IRQ38	IRQ37	IRQ36	IRQ35	IRQ34	IRQ33	IRQ32	IRQ31	IRQ30
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ2F	IRQ2E	IRQ2D	IRQ2C	IRQ2B	IRQ2A	IRQ29	IRQ28	IRQ27	IRQ26	IRQ25	IRQ24	IRQ23	IRQ22	IRQ21	IRQ20
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register provides a mean for software to relinquish and to refresh the interrupt controller. Writing a 1 to a specific bit position results in an End of Interrupt command issued internally to the corresponding interrupt line.

IRQ0-3F End of Interrupt command for the associated interrupt line.

- **0** No service is currently in progress or pending
- **1** Interrupt request is in-service

0x8101_00b0 IRQ Sensitive Register (low) IRQ_SENSL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F	IRQ1E	IRQ1D	IRQ1C	IRQ1B	IRQ1A	IRQ19	IRQ18	IRQ17	IRQ16	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF	IRQE	IRQD	IRQC	IRQB	IRQA	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8101_00b4 IRQ Sensitive Register (high) IRQ_SENSH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ3F	IRQ3E	IRQ3D	IRQ3C	IRQ3B	IRQ3A	IRQ39	IRQ38	IRQ37	IRQ36	IRQ35	IRQ34	IRQ33	IRQ32	IRQ31	IRQ30
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ2F	IRQ2E	IRQ2D	IRQ2C	IRQ2B	IRQ2A	IRQ29	IRQ28	IRQ27	IRQ26	IRQ25	IRQ24	IRQ23	IRQ22	IRQ21	IRQ20
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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All interrupt lines of IRQ Controller, IRQ0~IRQ3F can be programmed as either edge or level sensitive. By default, all the interrupt lines are edge sensitive and should be active LOW. Once a interrupt line is programmed as edge sensitive, an interrupt request is triggered only at the falling edge of interrupt line, and the next interrupt is not accepted until the EOI command is given. However, level sensitive interrupts trigger is according to the signal level of the interrupt line. Once the interrupt line become from HIGH to LOW, an interrupt request is triggered, and another interrupt request is triggered if the signal level remain LOW after an EOI command. Note that in edge sensitive mode, even if the signal level remains LOW after EOI command, another interrupt request is not triggered. That is because edge sensitive interrupt is only triggered at the falling edge.

IRQ0-3F Sensitivity type of the associated Interrupt Source

0 Edge sensitivity with active LOW

1 Level sensitivity with active LOW

0x8101_00c0 IRQ Software Interrupt Register (low) IRQ_SOFTL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_SRC1F	INT_SRC1E	INT_SRC1D	INT_SRC1C	INT_SRC1B	INT_SRC1A	INT_SRC19	INT_SRC18	INT_SRC17	INT_SRC16	INT_SRC15	INT_SRC14	INT_SRC13	INT_SRC12	INT_SRC11	INT_SRC10
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_SRCF	INT_SRCE	INT_SRCD	INT_SRCC	INT_SRCB	INT_SRCA	INT_SRC9	INT_SRC8	INT_SRC7	INT_SRC6	INT_SRC5	INT_SRC4	INT_SRC3	INT_SRC2	INT_SRC1	INT_SRC0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8101_00c4 IRQ Software Interrupt Register (high) IRQ_SOFTH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_SRC3F	INT_SRC3E	INT_SRC3D	INT_SRC3C	INT_SRC3B	INT_SRC3A	INT_SRC39	INT_SRC38	INT_SRC37	INT_SRC36	INT_SRC35	INT_SRC34	INT_SRC33	INT_SRC32	INT_SRC31	INT_SRC30
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_SRC2F	INT_SRC2E	INT_SRC2D	INT_SRC2C	INT_SRC2B	INT_SRC2A	INT_SRC29	INT_SRC28	INT_SRC27	INT_SRC26	INT_SRC25	INT_SRC24	INT_SRC23	INT_SRC22	INT_SRC21	INT_SRC20
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Setting “1” to the specific bit position generates a software interrupt for corresponding interrupt line before interrupt input multiplex. This register is used for debug purpose.

INT_SRC0-3F Software Interrupt

0x8101_00d0 FIQ Control Register FIQ_CON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name															**SENS**	**MASK**
Type															R/W	R/W
Reset															0	1

This register provides a means for software program to control the FIQ controller.

MASK Mask control for the FIQ Interrupt Source

- **0** Interrupt is enabled
- **1** Interrupt is disabled

SENS Sensitivity type of the FIQ Interrupt Source

- **0** Edge sensitivity with active LOW
- **1** Level sensitivity with active LOW

0x8101_00d4 FIQ End of Interrupt Register FIQ_EOI

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**EOI**
Type																WO
Reset																0

This register provides a means for software to relinquish and to refresh the FIQ controller. Writing a '1' to the specific bit position results in an End of Interrupt command issued internally to the corresponding interrupt line.

EOI End of Interrupt command

0x8101_00d8 Binary Coded Value of IRQ_STATUS IRQ_STA2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**NOIRQ**			**STA**					
Type								RO			RO					
Reset								0			0					

This Register is a binary coded version of IRQ_STA. It is used by the software program to poll which interrupt line has generated the IRQ interrupt request in a much easier way. Any read to it has the same result as reading IRQ_STA. The IRQ_STA2 is also read-only; write access has no effect on the content. Note that IRQ_STA2 should be coupled with IRQ_EOI2 while using it.

STA Binary coded value of IRQ_STA

NOIRQ Indicating if there is an IRQ or not. If there is no IRQ, this bit is HIGH, and the value of STA is 0_0000b.

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0x8101_00dc Binary Coded Value of IRQ_EOI IRQ_EOI2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name											EOI					
Type											WO					
Reset											0					

This register is a binary coded version of IRQ_EOI. It provides an easier way for software program to relinquish and to refresh the interrupt controller. Writing a specific code results in an End of Interrupt command issued internally to the corresponding interrupt line. Note that IRQ_EOI2 should be coupled with IRQ_STA2 while using it.

EOI Binary coded value of IRQ_EOI

0x8101_0100 EINT Interrupt Status Register EINT_STA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			EINT13	EINT12	EINT11	EINT10	EINT9	EINT8	EINT7	EINT6	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0
Type			RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register keeps up with current status of which EINT Source generated the interrupt request. If EINT sources are set to edge sensitive, EINT_IRQ is de-asserted while the corresponding EINT_INTACK is programmed by 1.

EINT0-EINT13 Interrupt Status

- **0** No interrupt request is generated
- **1** Interrupt request is pending

0x8101_0104 EINT Interrupt Mask Register EINT_MASK

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			EINT13	EINT12	EINT11	EINT10	EINT9	EINT8	EINT7	EINT6	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0
Type			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1

This register controls whether or not EINT Source is allowed to generate an interrupt request. Setting a “1” to the specific bit position prohibits the external interrupt line from becoming active.

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EINT0-EINT13 Interrupt Mask

- **0** Interrupt request is enabled.
- **1** Interrupt request is disabled.

0x8101_0108 EINT Interrupt Mask Clear Register EINT_MASK_CLR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			EINT13	EINT12	EINT11	EINT10	EINT9	EINT8	EINT7	EINT6	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0
Type			W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C

This register is used to clear individual mask bits. Only the bits set to 1 are in effect, and interrupt masks for which the mask bit is set are cleared (set to 0). Otherwise the interrupt mask bit retains its original value.

EINT0-EINT13 Disable mask for the associated external interrupt source

- **0** No effect.
- **1** Disable the corresponding MASK bit.

0x8101_010C EINT Interrupt Mask Set Register EINT_MASK_SET

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			EINT13	EINT12	EINT11	EINT10	EINT9	EINT8	EINT7	EINT6	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0
Type			W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S

This register is used to set individual mask bits. Only the bits set to 1 are in effect, and interrupt masks for which the mask bit is set are set to 1. Otherwise the interrupt mask bit retains its original value.

EINT0-EINT13 Disable mask for the associated external interrupt source.

- **0** No effect.
- **1** Enable corresponding MASK bit.

0x8101_0110 EINT Interrupt Acknowledge Register EINT_INTACK

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			EINT13	EINT12	EINT11	EINT10	EINT9	EINT8	EINT7	EINT6	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0
Type			WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO

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Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Writing "1" to the specific bit position acknowledges the interrupt request correspondingly to the external interrupt line source.

EINT0-EINT13 Interrupt acknowledgement

- **0** No effect.
- **1** Interrupt Request is acknowledged.

0x8101_0114 EINT Sensitive Register EINT_SENS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			EINT13	EINT12	EINT11	EINT10	EINT9	EINT8	EINT7	EINT6	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0
Type			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1

Sensitivity type of external interrupt source.

EINT0-EINT13 Sensitive type of the associated external interrupt source

- **0** Edge sensitivity.
- **1** Level sensitivity.

0x8101_0118 EINT Software Interrupt Register EINT_SOFT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			EINT13	EINT12	EINT11	EINT10	EINT9	EINT8	EINT7	EINT6	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0
Type			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Setting "1" to the specific bit position generates a software interrupt for corresponding interrupt line before mask. This register is used for debug purpose.

EINT0-EINT13 Software Interrupt

0x8101_0120+ n*0x10 EINTn De-bounce Control Register EINTn_CON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	EN	PRESCALER	POL	CNT
Type	R/W	R/W	R/W	R/W
Reset	0	0	0	0

These registers control the de-bounce logic for external interrupt sources in order to minimize the possibility of false activations.

When the external interrupt sources is used to resume the system clock from the sleep mode, the De-bounce control circuit must be enabled.

Note that n is from 0 to 13

CNT De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

POL Activation type of the EINT source

- **0** Negative polarity
- **1** Positive polarity

PRESCALER Determine the clock cycle period for debounce count.

- **000** 32768Hz, max: 0.0625sec
- **001** 16384Hz
- **010** 8192Hz
- **011** 4096Hz
- **100** 2048Hz, max: 1sec
- **101** 1024Hz
- **110** 512Hz
- **111** 256Hz, max: 8secs

EN De-bounce control circuit

- **0** Disable
- **1** Enable

If you have to change the debounce setting of some EINT. Please follow the steps:

1. mask the EINT which you want to change the debounce setting
2. disable debounce (EN=0)
3. delay at least 5 32K cycles
4. Enable the debounce (EN=1) and change the debounce setting
5. unmask the EINT

3.7 MPU

3.7.1 General Description

The purpose of MPU is to provide protection mechanism and cacheable indication of memory. The features of MPU include

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- 16-entry protection settings (MT6251 and MT6253).

  Determine if MCU can read/write a memory region. If the setting doesn't allow MCU's particular access to a memory address, MPU will stop the memory access and issue "ABORT" signal to MCU, making it entering into "abort" mode. The exception handler must then process the situation.

- 16-entry cacheable settings (MT6253 only).

  Determine a memory region is cacheable or not. If cacheable, MCU will keep a small copy in its cache after read accesses. If MCU requires the same data later, it can get it from the high-speed local copy, instead of from low-speed external memory.

Normally the protection and cacheable attributes are combined together for the same address range, as in the example of ARM946E. For greater flexibility, the MPU in MT6253 provides independent protection and cacheable settings. That is to say, the memory regions defined for memory protection and for cacheable are different and independent of each other.

The 4GB memory space is divided to 16 memory blocks of 256MB size, i.e., MB0~MB15. EMI takes MB0~MB3, SYSRAM and SYSROM take MB4, peripherals and other hardware take MB7~MB9, IDMA uses MB10. The characteristics of these memory blocks are listed below:

- Read/write protection setting

  MB7 and above (except MB10) are always readable/writeable.

  MB0~MB4 are determined by MPU.

- Cacheable setting

  MB4 and above are always non-cacheable.

  MB0~MB3 are determined by MPU.

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3.7.2 Protection Settings

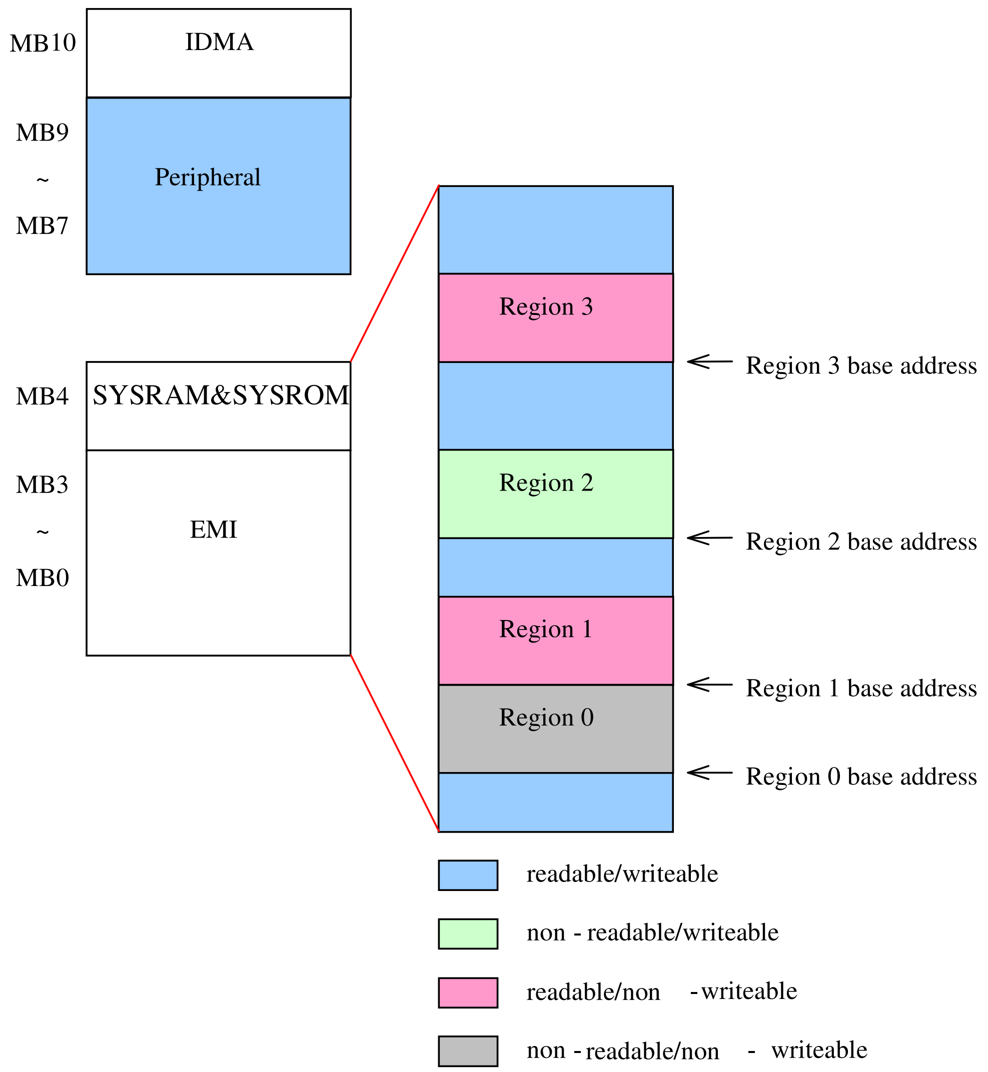

Figure 22 Protection setting

Figure 22 shows the protection setting in each memory block. Five regions are defined in the figure. Note that each region can be continuous or non-continuous to each other, and those address ranges not covered by any region are set to be readable/writeable automatically. One restriction exists: different regions must not overlap.

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The user can define maximum 16 regions in MB0~MB4 and MB10. Each region has its own setting defined in a 32-bit register:

31 … 10	9–8	7–6	5–1	0
base address	00	prot	size	EN

- Region base address (22 bits)
- Region size (5 bits)
- Region protection attribute (2 bits)
- Enable bit (1 bit)

MPU will abort MCU if it accesses MB5, MB6, MB11~MB15 regions (empty regions).

MPU will also abort MCU if it accesses address from 0x4002_4000 to 0x47ff_ffff (empty region).

3.7.2.1 Region base address

Region base address defines the start of the memory region. The user needs only to specify several upper address bits. The number of valid address bits depends on the region size. **The user must align the base address to a region-size boundary.** For example, if a region size is 8KB, its base address must be a multiple of 8KB.

3.7.2.2 Region size

The bit encoding of region size and its relationship with base address are listed as follows.

Region size	Bit encoding	Base address
1KB	00000	Bit [31:10] of region start address
2KB	00001	Bit [31:11] of region start address
4KB	00010	Bit [31:12] of region start address
8KB	00011	Bit [31:13] of region start address
16KB	00100	Bit [31:14] of region start address
32KB	00101	Bit [31:15] of region start address
64KB	00110	Bit [31:16] of region start address
128KB	00111	Bit [31:17] of region start address
256KB	01000	Bit [31:18] of region start address
512KB	01001	Bit [31:19] of region start address

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1MB	01010	Bit [31:20] of region start address
2MB	01011	Bit [31:21] of region start address
4MB	01100	Bit [31:22] of region start address
8MB	01101	Bit [31:23] of region start address
16MB	01110	Bit [31:24] of region start address

Table 13 Region size and bit encoding

3.7.2.3 Region protection attribute

This attribute has two bits. The MSB determines read access permission, and the LSB for write access permission.

Bit encoding	Permission
00	non-readable / non-writeable
10	readable / non-writeable
01	non-readable / writeable
11	readable / writeable

Table 14 Region protection attribute bit encoding

Note that bit encoding “11” allows full read/write permission, which is the case when no region is specified. So it is recommended to only specify regions with protection attribute “00”, “10” or “01”.

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3.7.3 Cacheable Settings

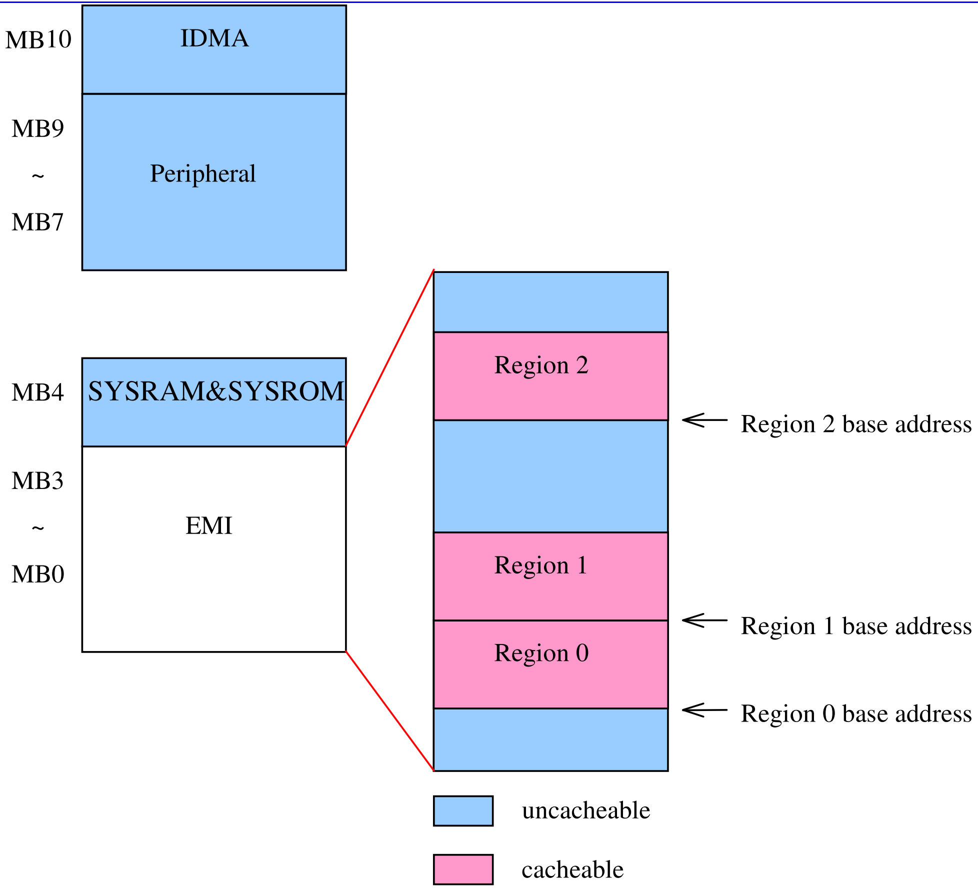

Figure 23 Cacheable setting

Figure 23 shows the cacheable setting in each memory block. Three regions are defined in the figure. Note that each region can be continuous or non-continuous to each other, and those address ranges not covered by any region are set to be uncacheable automatically. One restriction exists: different regions must not overlap.

The user can define maximum 16 regions in MB0~MB3. Each region has its own setting defined in a 32-bit register:

31 ... 10	9 ... 7	6	5 ... 1	0
base address	000	C	size	EN

- Region base address (22 bits)
- Region size (5 bits)

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- Region cacheable attribute (1 bit)
- Enable bit (1 bit)

The region base address and region size bit encoding are the same as those of protection setting. **The user must also align the base address to a region-size boundary.** The cacheable attribute has the following meaning.

Bit encoding	Attribute
0	uncacheable
1	cacheable

Table 15 Region cacheable attribute bit encoding

3.7.4 MPU Register Definition

MPU base address is assumed 0x850f_0000 (subject to change).

0x850f_0000 ~ 0x850f_003C **Protection setting for region 0 to 15** **MPU_PROT0~15**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASEADDR[31:16]															
Type	R W															
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	BASEADDR[15:10]								ATTR[1:0]		SIZE[4:0]					EN
Type	R W								R W		R W					R W
Reset									11		00000					0

This register sets protection attributes for region 0 to 15.

BASEADDR Base address of this region

ATTR Protection attribute

- **00** non-readable / non-writeable
- **01** non-readable / writeable
- **10** readable / non-writeable
- **11** readable / writeable

SIZE size of this region

- **00000** 1KB
- **00001** 2KB
- **00010** 4KB
- **00011** 8KB
- **00100** 16KB
- **00101** 32KB
- **00110** 64KB

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00111 128KB
01000 256KB
01001 512KB
01010 1MB
01011 2MB
01100 4MB
01101 **8MB**
01110 **16MB**

EN enable this region
0 Disable
1 Enable

0x850f_0040 ~ 0x850f_007C Cacheable setting for region 0 to 15 MPU_CACHE0~15

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASEADDR[31:16]															
Type	R W															
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASEADDR[15:10]									C	SIZE[4:0]					EN
Type	R W									R W	R W					R W
Reset										0	00000					0

This register sets cacheable attributes for region 0 to 15.

BASEADDR Base address of this region

C Cacheable attribute
0 uncacheable
1 cacheable

SIZE size of this region
00000 1KB
00001 2KB
00010 4KB
00011 8KB
00100 16KB
00101 32KB
00110 64KB
00111 128KB
01000 256KB
01001 512KB
01010 1MB
01011 2MB
01100 4MB

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01101 8MB
01110 16MB

EN enable this region
0 Disable
1 Enable

The following registers are located inside config module. When any of them is set abort signal will be issued.

0x8001_0604 SYSRAM4_ERR_FLAG SRAM4_ACC__ERR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ERR
Type																R/W
Reset																0

This register indicates that AHB master (MCU is not included) is trying to access sysram bank 4, if there is any, when it is configured as cache way 0.

ERR Error bit to indicate a illegal access
0 legit
1 illegal

0x8001_0608 SYSRAM5_ERR_FLAG SRAM5_ACC_ERR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ERR
Type																R/W
Reset																0

This register indicates that AHB master (MCU is not included) is trying to access sysram bank 5, if there is any, when it is configured as cache way 1.

ERR Error bit to indicate a illegal access
0 legit
1 illegal

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0x8001_060C SYSROM_ERR_FLAG SROM_ACC_ERR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ERR
Type																R/W
Reset																0

This register indicates that AHB master (MCU is not included) is trying to access sysrom.

ERR Error bit to indicate a illegal access

- **0** legit
- **1** illegal

3.8 Internal Memory Interface

3.8.1 System RAM

MT6253 provides one 128K Bytes size of on-chip memory modules acting as System RAM for data access with low latency. Such a module is composed of one high speed synchronous SRAM with AHB Slave Interface connected to the system backbone AHB Bus, as shown in **Figure 24**. The synchronous SRAM operates on the same clock as the AHB Bus and is organized as 32 bits wide with 4 byte-write signals capable for byte operations.

3.8.2 System ROM

The 20K Bytes System ROM is primarily used to store software program for Factory Programming and security-related routines. This module is composed of high-speed ROM with an AHB Slave Interface connected to a system backbone AHB, shown in **Figure 24**. The module operates on the same clock as the AHB and has a 32-bit wide organization.

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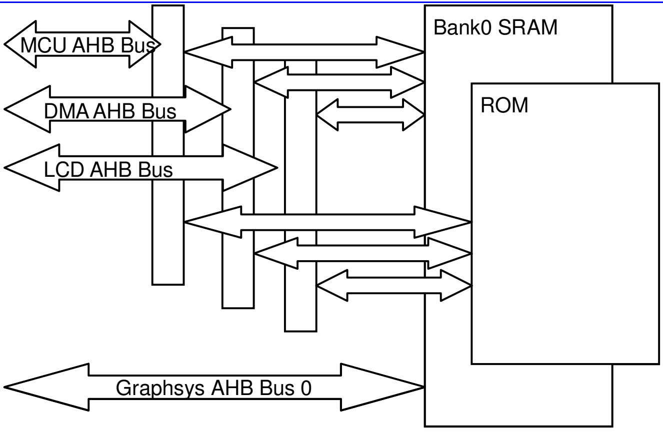

Figure 24 Block Diagram of the Internal Memory Controller

3.9 External Memory Interface

3.9.1 General Description

MT6253 incorporates a powerful and flexible memory controller, External Memory Interface, to connect with a variety of memory components. This controller provides one generic access scheme for FLASH Memory, SRAM and PSRAM. Up to 4 memory banks can be supported simultaneously, BANK0-BANK3, with 64MB maximal size each. MT6253 supports **ADMUX**-type memory only.

Since most of the FLASH Memory, SRAM and PSRAM have similar AC requirements, a generic configuration scheme to interface them is desired. This way, the software program can treat different components by simply specifying certain predefined parameters. All these parameters are based on cycle time of system clock. The external memory need to be set as **16-byte burst length and burst wrap on**.

The interface definition based on such scheme is listed in **Table 16**. Note that, this interface always operates data in Little Endian format for all types of accesses.

Signal Name	Type	Description
EA[24:16]	O	Address Bus
ED[15:0]	I/O	Address/Data Bus
EWR#	O	Write Enable Strobe
ERD#	O	Read Enable Strobe
ELB#	O	Lower Byte Strobe
EUB#	O	Upper Byte Strobe
ECS# [3:0]	O	BANK0~BANK3 Selection Signal
ECLK	O	Burst Mode FLASH Memory Clock Signal

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EADV#	O	Burst Mode FLASH Memory Address Latch Signal
EWAIT	I	Wait Signal Input

Table 16 **External Memory Interface of MT6253 for Asynchronous/Synchronous Type Components**

This controller can also handle parallel type of LCD. By connecting with them, 8080 type of control method is supported. The interface definition is detailed in **Table 17**.

Bus Type	ECS3#	EA25	ERD#	EWR#	ED[15:0]
8080 series	CS#	A0(1:Command 0: Data)	RD#	WR#	D[15:0]

Table 17 Configuration for LCD Parallel Interface

REGISTER ADDRESS	REGISTER NAME	SYNONYM
8100_0000h	EMI Control Register for BANK0	EMI_CONA
8100_0004h	EMI Control Register for BANK1	EMI_CONB
8100_0008h	EMI Control Register for BANK2	EMI_CONC
8100_000Ch	EMI Control Register for BANK3	EMI_COND
8100_0020h	EMI Monitor Control Register	EMI_MONCTRL
8100_0024h	EMI Cycle Count Register	EMI_CYCCNT
8100_0028h	EMI Data Byte Count Register	EMI_DBYTECNT
8100_002Ch	EMI Request Count Register	EMI_RQCNT
8100_0030h	EMI Qualified Byte Request Count Register	EMI_RQBCNT
8100_0034h	EMI Qualified Half Word Request Count Register	EMI_RQHWCNT
8100_0038h	EMI Qualified Word Request Count Register	EMI_RQWCNT
8100_0040h	EMI Remap Control Register	EMI_REMAP
8100_0044h	EMI General Control Register	EMI_GEN
8100_0048h	EMI Clock Delay Register	EMI_CLOCKDEL
8100_0070h	Code Cache and Code Prefetch Control Register	PREFETCH_CON
8100_0074h	EMI A/D Mux Control Register	EMI_ADMUX
8100_0078h	EMI Extension Control Register	EMI_EXTCON
8100_007Ch	EMI Extension Control Register 2	EMI_EXTCON2
8100_0080h	EMI General Control Register 2	EMI_GEN2
8100_0090h	EMI Control Extension Register for BANK 0	EMI_CONA_EXT
8100_0094h	EMI Control Extension Register for BANK 1	EMI_CONB_EXT
8100_0098h	EMI Control Extension Register for BANK 2	EMI_CONC_EXT
8100_009Ch	EMI Control Extension Register for BANK 3	EMI_COND_EXT

Table 18 External Memory Interface Register Map

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3.9.2 Register Definitions

8100_0000h EMI Control Register for BANK0 EMI_CONA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	C2WS				C2WH	C2RS			ADVW	ADVR	LPB	PRLT			BMODE	PMODE
Type	R/W				R/W	R/W			R/W	R/W	R/W	R/W			R/W	R/W
Reset	0				0	0			1	1	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DW	RBLN	HPI	WST					BW	RWAIT_EN	PSIZE	RLT				
Type	R/W	R/W	R/W	R/W					R/W	R/W	R/W	R/W				
Reset	0	1	0	6					0	0	0	7				

8100_0004h EMI Control Register for BANK1 EMI_CONB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	C2WS				C2WH	C2RS			ADVW	ADVR	LPB	PRLT			BMODE	PMODE
Type	R/W				R/W	R/W			R/W	R/W	R/W	R/W			R/W	R/W
Reset	0				0	0			1	1	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DW	RBLN	HPI	WST					BW	RWAIT_EN	PSIZE	RLT				
Type	R/W	R/W	R/W	R/W					R/W	R/W	R/W	R/W				
Reset	0	1	0	6					0	0	0	7				

8100_0008h EMI Control Register for BANK2 EMI_CONC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	C2WS				C2WH	C2RS			ADVW	ADVR	LPB	PRLT			BMODE	PMODE
Type	R/W				R/W	R/W			R/W	R/W	R/W	R/W			R/W	R/W
Reset	0				0	0			1	1	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DW	RBLN	HPI	WST					BW	RWAIT_EN	PSIZE	RLT				
Type	R/W	R/W	R/W	R/W					R/W	R/W	R/W	R/W				
Reset	0	1	0	6					0	0	0	7				

8100_000Ch EMI Control Register for BANK3 EMI_COND

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	C2WS				C2WH	C2RS			ADVW	ADVR	LPB	PRLT			BMODE	PMODE
Type	R/W				R/W	R/W			R/W	R/W	R/W	R/W			R/W	R/W
Reset	0				0	0			1	1	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DW	RBLN	HPI	WST					BW	RWAIT_EN	PSIZE	RLT				

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Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	6	0	0	0	7

For each bank (BANK0-BANK3), a dedicated control register is associated with the bank controller. These registers have the timing parameters that help the controller to convey memory access into proper timing waveform. Note that parameters C2WS, C2WH, C2RS, PRLT, WST and RLT specified explicitly are based on system clock speed in terms of cycle count.

RLT Read Latency Time

Specifying the parameter RLT turns effectively to insert wait-states in bus transfer to requesting agent. Such parameter should be chosen carefully to meet the common parameter tAA (address access time) for device in read operation. Example is shown below.

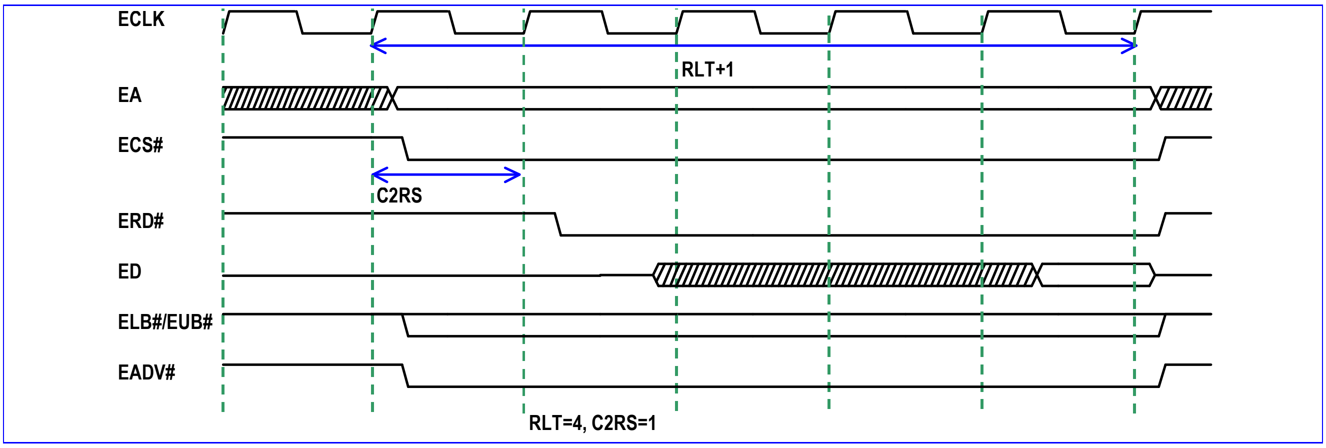

Figure 25 Read Wait State Timing Diagram (ADVR=1)

Address Access Time	Read Latency Time			
	13MHz	26MHz	52MHz	104MHz
60ns	0	1	3	6
90ns	1	2	4	9
120ns	1	3	6	12

Table 19 Reference value of Read Latency Time for variant memory devices

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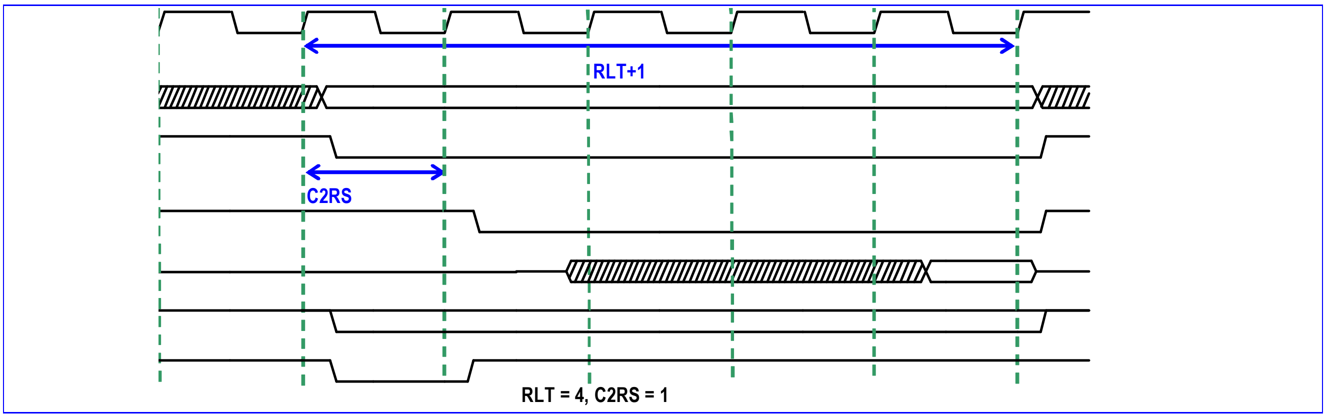

Figure 26 Read Wait State Timing Diagram (ADVR=0)

RLT had better to be not larger than 18. Due to frequency hopping, mpll_clkswprd signal will assert 28T in advance to notify EMI that clock pulse is going to disappear. Considering the longest burst read access time (pre-fetch size = 16 bytes), the on-going transaction need to end within 28T. This restriction is only valid when MPLL_EN setting in register EMI_GEN2 asserts.

PMODE Page Mode Control

If target device supports page mode operations, the Page Mode Control can be enabled. Read in Page Mode is determined by set of parameters: PRLT and PSIZE.

0 disable page mode operation

1 enable page mode operation

BMODE Burst Mode Control

If target device supports burst mode operations, the Burst Mode Control can be enabled. Read in Burst Mode is determined by set of parameters: PRLT and PSIZE.

0 disable burst mode operation

1 enable burst mode operation

PRLT Read Latency within the Same Page or in Burst Mode Operation

Since page/burst mode operation only helps to eliminate read latency in subsequent burst within the same page, it doesn't matter with the initial latency at all. Thus, it should still adopt RLT parameter for initial read or burst read between different pages though PMODE or BMODE is set "1". This parameter should be chosen carefully to meet the common parameter tPAA (page address access time) for device in page mode. PRLT need to be 0 in burst mode, but this field cannot be 0 in page mode.

000 zero wait state

001 one wait state

010 two wait state

011 three wait state

100 four wait state

101 five wait state

110 six wait state

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111 seven wait state

LPB Low Power Burst Mode Operation

LPB is only useful in burst mode. If LPB = 1, ECLK will be gated automatically when external bus is idle.

0 Disable Low Power Burst Mode

1 Enable Low Power Burst Mode

PSIZE Page Size for Page/Burst Mode Operation

These bit positions describe the page size that the Page/Burst Mode enabled device will behave.

0 8 byte, EA[25:3] remains the same

1 16 byte, EA[25:4] remains the same

RWAIT_EN Burst Read Wait Enable Signal Control

0 Once initial latency ends, EMI starts to receive data regardless of EWAIT

1 Once initial latency ends, EMI starts to receive data only when EWAIT de-asserts

BW Burst Write Enable

0 Asynchronous write

1 Synchronous write

WST Write Wait State

Specifying the parameters to extend adequate setup and hold time for target component in write operation. Those parameters also effectively insert wait-states in bus transfer to requesting agent. Example is shown in **Figure 27** and **Table 20**.

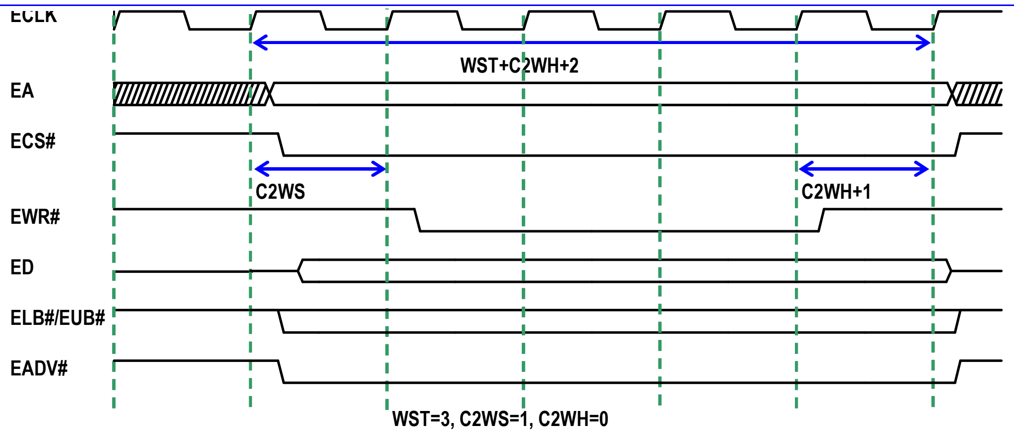

Figure 27 Write Wait State Timing Diagram (ADVW=1)

Write Pulse Width (Write Data Setup Time)	Write Wait State			
	13MHz	26MHz	52MHz	104MHz
30ns	0	0	1	3
60ns	0	1	3	6
90ns	1	2	4	9

Table 20 Reference value of Write Wait State for variant memory devices

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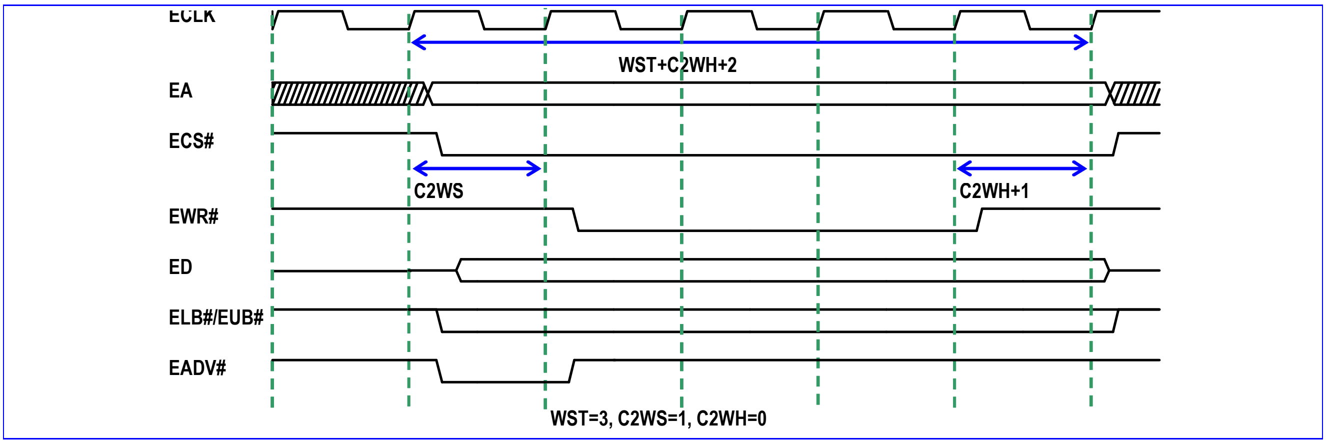

Figure 28 Write Wait State Timing Diagram (ADVW=0)

RBLN Read Byte Lane Enable

- **0** all byte lanes held high during system reads
- **1** all byte lanes held low during system reads

DW Data Width of External Memory Device

- **0** 16-bit device (MT6253 only supports 16-bit memory device)
- **1** 8-bit device

HPI HPI Mode Control

Previous memory device async. mode operation need to consider EWAIT. This is called HPI mode.

- **0** Disable HPI Mode
- **1** Enable HPI Mode

ADVR Read Address Valid

This setting must be 1 in page mode read access and 0 in burst mode read access.

- **0** EADV# will be toggled to latch the valid address in read operation
- **1** EADV# will be held low for entire read operation

ADVW Write Address Valid

This setting must be 0 in burst mode write access.

- **0** EADV# will be toggled to latch the valid address in write operation
- **1** EADV# will be held low for entire write operation

C2RS Chip Select to Read Strobe Setup Time

C2WH Chip Select to Write Strobe Hold Time

C2WS Chip Select to Write Strobe Setup Time

8100_0020h EMI Monitor Control Register EMI_MONCTRL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PORT_EN		TRANS_TYPE				ID_IND		ALIGN_IND		ULTRA_IND		RW_IND		MON_CLR	MON_EN
Type	R/W		R/W				R/W		R/W		R/W		R/W		R/W	R/W
Reset	11		1000				10		10		10		10		0	0

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MON_EN Enable Monitor Function Control
MON_CLR Clear Monitor Counter Control
RW_IND Read/Write Request Indication. Determine to observe read or write or both request number
- **00** Read requests
- **01** Write requests
- **10** Both requests

ULTRA_IND Ultra Request Indication. Determine to observe ultra or non-ultra or both request number
- **00** Non-ultra requests
- **01** Ultra requests
- **10** Both requests

ALIGN_IND Align Request Indication. Determine to observe aligned or non-aligned or both request number
- **00** Non-aligned requests
- **01** Aligned requests
- **10** Don't care

Aligned or non-aligned indications are only useful for incr4, incr8, incr16 type of transaction, and MCU bus also observes wrap4-4 transaction. Aligned or not will affect EMI performance, therefore request number need to be recorded separately. As for don't care, it means record all types of transaction not only incr-4, 8, 16. The alignment criterion also depends on page size setting.

ID_IND MCU Port Instruction / Data Request Indication
- **00** MCU port data requests
- **01** MCU port instruction requests
- **10** Don't care

TRANS_TYPE Burst Type Indication
- **0000** Single requests
- **0010** Wrap-4 requests
- **0011** Incr-4 requests
- **0101** Incr-8 requests
- **0111** Incr-16 requests
- **1000** Don't care

PORT_EN MCU Port / DMA Port Control
- **X1** MCU port
- **1X** DMA port

8100_0024h EMI Cycle Count Register EMI_CYCCNT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CYC_CNT															
Type	RO															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CYC_CNT															
Type	RO															

CYC_CNT Record total cycle count during monitor function enable duration

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8100_0028h EMI Data Byte Count Register EMI_DBYTECNT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBYTE_CNT															
Type	RO															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBYTE_CNT															
Type	RO															

DBYTE_CNT Record total data count during monitor function enable duration

8100_002Ch EMI Request Count Register EMI_RQCNT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RQ_CNT															
Type	RO															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RQ_CNT															
Type	RO															

RQ_CNT Record total request cycle count during monitor function enable duration including MCU & DMA port

8100_0030h EMI Qualified Byte Request Count Register EMI_RQBCNT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RQB_CNT															
Type	RO															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RQB_CNT															
Type	RO															

RQB_CNT Record total qualified byte request count during monitor function enable duration. Qualified means constrained by EMI_MONCTRL register

8100_0034h EMI Qualified Half Word Request Count Register EMI_RQHWCNT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RQHW_CNT															
Type	RO															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RQHW_CNT															
Type	RO															

RQHW_CNT Record total qualified half word request count during monitor function enable duration. Qualified means constrained by EMI_MONCTRL register

8100_0038h EMI Qualified Word Request Count Register EMI_RQWCNT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RQW_CNT															
Type	RO															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RQW_CNT															
Type	RO															

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RQW_CNT Record total qualified word request count during monitor function enable duration. Qualified means constrained by EMI_MONCTRL register

8100_0040h EMI Re-map Control Register EMI_REMAP

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RM1	RM0
Type															R/W	R/W
Reset															BOOT	0

This register accomplishes the Memory Re-mapping Mechanism. Basically, it provides the kernel software program or system designer a capability of changing memory configuration dynamically. Three kinds of configuration are permitted.

RM[1:0] Re-mapping control for Boot Code, BANK0 and BANK1, refer to **Table 21**.

RM[1:0]	Address 0000_0000h – 0x07ff_ffffh	Address 0800_0000h – 0x0fff_ffffh
00	Boot Code	BANK1
01	BANK1	BANK0
10	BANK0	BANK1
11	BANK1	BANK0

Table 21 Memory Map Configuration

8100_0044h EMI General Control Register EMI_GEN

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CKSR	CKE2	CKE4	CKE8	CONSR	CONE2	CONE4	CONE8	EASR	EAE2	EAE4	EAE8	EDSR	EDE2	EDE4	EDE8
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRCEN	PRCCNT				EXTGUARD		EDA	FLUSH	WPOL			CKPH_SEL			
Type	R/W	R/W				R/W		R/W	R/W	R/W			R/W			
Reset	0	0				0		1	1	0			0			

This register is general control that can alter the behavior of all bank controllers according to specific features below.

PRCEN Pseudo SRAM Write Protection Control

- **0** Disable
- **1** Enable

PRCCNT Pseudo SRAM Dummy Cycle Insertion Count

EXTGUARD Extra Guard Cycle Insertion between Contiguous Read/Write Access

EDA ED[15:0] Activity

- **0** Drive ED Bus only on write access
- **1** Always drive ED Bus except for read access

FLUSH Instruction Cache Write Flush Control

WPOL FLASH, SRAM, PSRAM and CellularRAM Wait Signal Inversion Control

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0 Wait if EWAIT = 0.
1 Wait if EWAIT = 1.
In 4T data valid window, this setting needs to be 0.

CKPH_SEL Select External Memory Device Clock Source
0 CK1X_INVL (Centered-aligned emi controller clock, and park at low)
1 CK1X_INVH (Centered-aligned emi controller clock, and park at high)
Option CKPH_SEL = 1 was added to prevent BRAW from being misinterpreted as BRBW in 53T. Because clock enable signal will be sampled once in the path of CKPH_SEL = 0, whereas clock enable directly passes through to CG cell in the path of CKPH_SEL = 1, there will be one more clock pulse for CKPH_SEL = 0. In 53MP, clock enable signal logic has been modified and CKPH_SEL = 0 can be used in all scenarios.

CKSR ECLK Pad Slew Rate Control
CKEx ECLK Pad Driving Control
CONSR EADV#, ECS#, EWR#, ERD#, EUB# and ELB# Pad Slew Rate Control
CONEx EADV#, ECS#, EWR#, ERD#, EUB# and ELB# Pad Driving Control
EASR EA[25:0] Pad Slew Rate Control
EAEx EA[25:0] Pad Driving Control
EDSR ED[15:0] Pad Slew Rate Control
EDEx ED[15:0] Pad Driving Control

8100_0048h EMI Clock Delay Register EMI_CLOCKDEL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CK_SEL	RDSEL	DPU	DPD	DSMT											
Type	R/W	R/W	R/W	R/W	R/W											
Reset	0	0	0	0	0											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CLKDLY														
Type		R/W														
Reset		0														

CK_SEL Select which clock source output to external memory
0 Based on CKPH_SEL bit setting in EMI_GEN register
1 EC_CLK (Original Clock with delay line)

RDSEL Data Macro PMOS Driving Strength Control
This control is used to adjust rising transition time

DPU Data Macro Pull Up Control
This control is used to force data I/O to logic1 without driving.

DPD Data Macro Pull Down Control
This control is used to force data I/O to logic0 without driving.

DSMT Data Macro Schmidt Control
This control is used to improve data signal quality.

CLKDLY EC_CLK delay setting

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EC_CLK delay chain is composed of 3 16-tap delay macros. CLKDLY bit 14 decide clock source is original clock or invert clock. CLKDLY[3:0] are the delay setting of first delay macro, whereas [7:4] is the second and [11:8] is the third. Bit 13, 12 decide which clock source between these delay macros are drawn out. The larger delay setting is, longer delay is applied.

Delay setting sequence:

CLKDLY : 000_0000_0000_0000 → 001_0000_0000_0000 – 001_0000_0000_1111 → 010_0000_0000_1111 – 010_0000_1111_1111 → 011_0000_1111_1111 – 011_1111_1111_1111 → 100_0000_0000_0000 → 101_0000_0000_0000 – 101_0000_0000_1111 → 110_0000_0000_1111 – 110_0000_1111_1111 → 111_0000_1111_1111 – 111_1111_1111_1111

8100_0070h Code Cache and Code Prefetch Control Register PREFETCH_CON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DB3	DB2	DB1	DB0						DWRP8	DPREF	DCACH
Type					R/W	R/W	R/W	R/W						R/W	RW	R/W
Reset					0	0	0	0						0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					IB3	IB2	IB1	IB0						IWRP8	IPREF	ICACH
Type					R/W	R/W	R/W	R/W						R/W	RW	R/W
Reset					0	0	0	0						0	0	0

This register is used to control the functions of Code/Data Cache and Code/Data Prefetch. The Code/Data Cache is a low latency memory that can store up to 16 most recently used instruction codes/data. While an instruction/data fetch hits the one in the code/data cache, not only the access time could be minimized, but also the singling to off chip ROM or FLASH Memory could be relieved. In addition, it can also store up to 16 prefetched instruction codes/data while Code/Data Prefetch function is enabled. The Code/Data Prefetch is a sophisticated controller that can predict and fetch the instruction codes/data in advance based on previous code/data fetching sequence. As the Code/Data Prefetch always performs the fetch staffs during the period that the EMI interface is in IDLE state. The bandwidth to off chip memory could be fully utilized. On the other hand, if the instruction/data fetch hits the one of prefetched codes/data, the access time could be minimized and then enhance the overall system performance.

xWRP8 Prefetch Size

- **0** 8 bytes
- **1** 16 bytes

xBn Prefetchable/Cacheable Area

There bit positions determine the prefetchable and cacheable region in which the instruction/data could be cached or prefetched.

xPREF Prefetch Enable

xCACH Cache Enable

8100_0074h EMI A/D Mux Control Register EMI_ADMUX

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														A2ADVH		MODE
Type														R/W		R/W
Reset														1		XADMUX

MODE A/D Mux memory I/F selection signal. The default value depends on the value of XADMUX pin at reset.

- **0** Non-A/D Mux Mode
- **1** A/D Mux Mode

A2ADVH Address Valid to Address Hold Time

8100_0078h EMI Extension Control Register EMI_EXTCON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									XT_SEL							
Type									R/W							
Reset									0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ADV_CYC							
Type									R/W							
Reset									0							

ADV_CYC ADV signal assert duration in ADV enable mode (2bits/bank). ADV_CYC = k means k+1 cycle assertion. Only useful in A/D demux async mode

XT_SEL Select read data sample times in data macro (2bits/bank)

- **0** For 4T data valid window path (Burst Mode)
- **1** 1 times (Burst Mode)
- **2** 0 time (Async/Page Mode)

8100_007Ch EMI Extension Control Register 2 EMI_EXTCON2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CKE								WWAIT_EN			
Type					R/W								R/W			
Reset					0								0			

WWAIT_EN Burst Write Wait Signal Enable Control. Bit 0 for bank0, and so on

- **0** Once initial latency ends, emi starts to write data out regardless of wait signal
- **1** Once initial latency ends, emi starts to write data out only when wait signal deasserts

CKE Burst Mode FLASH Memory Clock Enable Control. Bit 8 for bank0, and so on

8100_0080h EMI General Control Register 2 EMI_GEN2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											APCC	B2S	EWAIT_SEL_RDCLK	ED_SEL_RDCLK	ULTRA_EN	EWAIT_SEL
Type											R/W	R/W	R/W	R/W	R/W	R/W
Reset											0	0	1	1	1	0

EWAIT_SEL EWAIT Input Selection Control
0: Sampled by positive edge clock
1: Sampled by negative edge clock first then positive edge clock

ULTRA_EN Ultra Enable Control
If layer2 bus issues ultra-high write command, it will get upmost arbitration priority if ultra_en asserts. Otherwise ultra-high write command has normal priority. This enable bit is used to protect MCU command from being blocked too long and result in performance degradation

ED_SEL_RDCLK ED Macro RD_CLK source selection Control
0: Internally generated rd_clk. Need to set external memory device as fixed latency
1: Feedback external memory clock

EWAIT_SEL_RDCLK EWAIT Macro RD_CLK source selection Control
0: Internally generated rd_clk. Need to set external memory device as fixed latency
1: Feedback external memory clock

B2S Burst to Single Control
Split layer2 bus burst transaction to single to prevent MCU from being blocked from too long

APCC Asynchronous & Page Mode Command Continuous Control
If enable this setting, async mode and page mode command could be successive without de-asserting cs_b. Though performance improves, cs_b enable duration may violate timing spec. Default is off.

8100_0090h EMI Control Extension Register for BANK0 EMI_CONA_EXT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								EWAIT_DEL			ED_DEL			FBCLK_DEL		
Type								R/W			R/W			R/W		
Reset								0			0			0		

8100_0094h EMI Control Extension Register for BANK1 EMI_CONB_EXT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name								EWAIT_DEL			ED_DEL			FBCLK_DEL		
Type								R/W			R/W			R/W		
Reset								0			0			0		

8100_0098h EMI Control Extension Register for BANK2 EMI_CONC_EXT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								EWAIT_DEL			ED_DEL			FBCLK_DEL		
Type								R/W			R/W			R/W		
Reset								0			0			0		

8100_009Ch EMI Control Extension Register for BANK3 EMI_COND_EXT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								EWAIT_DEL			ED_DEL			FBCLK_DEL		
Type								R/W			R/W			R/W		
Reset								0			0			0		

FBCLK_DEL Feedback Clock Delay Setting

ED_DEL Data Delay Setting

EWAIT_DEL EWAIT Delay Setting

These three settings are only useful when ED_SEL_RDCLK & EWAIT_SEL_RDCLK are set and are used to compensate trace delay. Normally there is no need to modify these three settings. The larger delay setting is, longer delay is applied.

Special note:

➔The special wire connection among CRE, EA[24] and Addr[25].

16-bits mode (data-pin) ext-MEM :

(A) If max memory size is 32Mbyte(16MX16)

MT6253 can access 16M address location, and support hardware configure by CRE pin (from EA[24] and Addr[25]).

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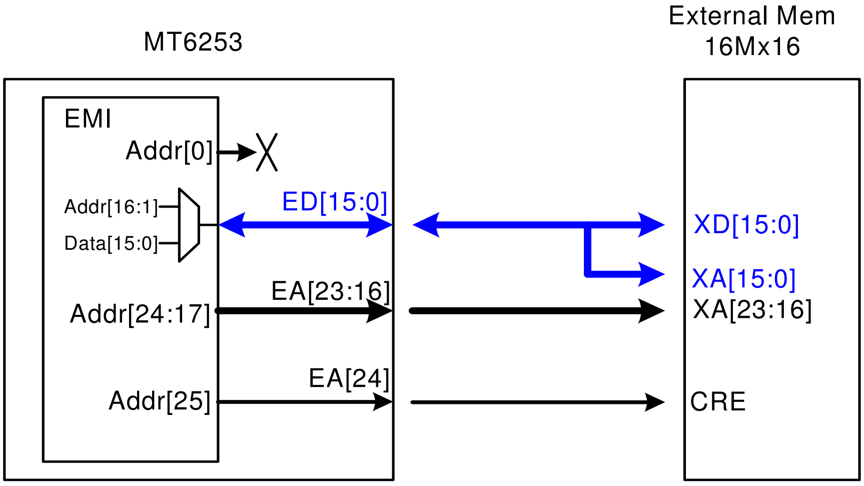
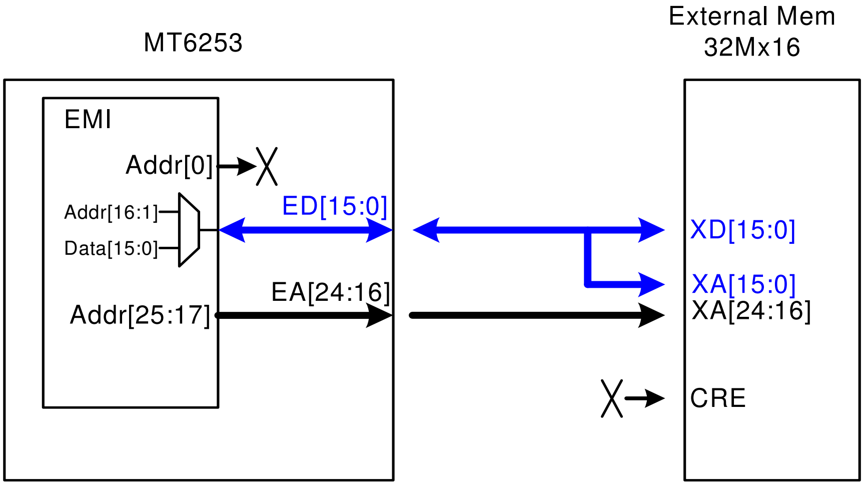


(B) If max memory size is 64Mbyte(32MX16)

MT6253 can access 32M address location, and **only support software configure (without hardware configure, because no extra pin-out for CRE pin)**.



External memory is word (16-bit) addressable (EA[24:0], XA[24:0]).

EMI is byte (8-bit) addressable (Addr[25:0]).

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4 Microcontroller Peripherals

Microcontroller (MCU) Peripherals are devices that are under direct control of the Microcontroller. Most of the devices are attached to the Advanced Peripheral Bus (APB) of the MCU subsystem, and serve as APB slaves. Each MCU peripheral must be accessed as a memory-mapped I/O device; that is, the MCU or the DMA bus master reads from or writes to the specific peripheral by issuing memory-addressed transactions.

4.1 Pulse-Width Modulation Outputs

4.1.1 General Description

Three generic pulse-width modulators are implemented to generate pulse sequences with programmable frequency and duty cycle for LCD backlight or charging purpose. The duration of the PWM output signal is LOW as long as the internal counter value is greater than or equal to the threshold value. The waveform is shown in **Figure 29**.

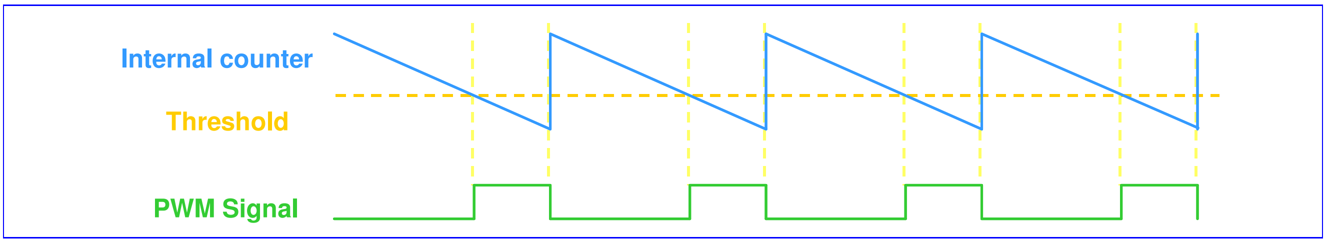

Figure 29 PWM waveform

The frequency and volume of PWM output signal are determined by these registers: PWM_COUNT, PWM_THRES, PWM_CON. The POWERDOWN (pdn_pwm) signal is applied to power-down the PWM module. When PWM is deactivated (POWERDOWN=1), the output is in LOW state.

The output PWM frequency is determined by:

$$\frac{CLK}{CLOCK_DIV \times (PWM_COUNT + 1)} \quad \mathrm{CLK} = 13000000 \text{ when } \mathrm{CLKSEL} = 0, CLK = 32000 \, when CLKSEL = 1$$

CLOCK_DIV = 1, when CLK[1:0] = 00b

CLOCK_DIV = 2, when CLK[1:0] = 01b

CLOCK_DIV = 4, when CLK[1:0] = 10b

CLOCK_DIV = 8, when CLK[1:0] = 11b

The output PWM duty cycle is determined by: $\frac{PWM_THRES}{PWM_COUNT + 1}$

Note that PWM_THRES should be less than the PWM_COUNT: if this condition is not satisfied, the output pulse of the PWM is always HIGH.

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4.1.2 Register Definitions

0x8109_0000h PWM1 Control register PWM1_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CLKSEL	CLK [1:0]	
Type														R/W	R/W	
Reset														0	0	

CLK Select PWM1 clock prescaler scale.

00 CLK Hz

01 CLK/2 Hz

10 CLK/4 Hz

11 CLK/8 Hz

Note: When PWM1 module is disabled, its output should be kept in the LOW state.

CLKSEL Select PWM1 clock

0 CLK=13M Hz

1 CLK=32K Hz

Note: In order to integrate the RF chip into our baseband chip, the clock frequency (CLKSEL=0) is hopping between 13MHz and 14.125MHz, and the clock frequency (CLKSEL=1) is hopping between 32kHz and 34.77kHz. The duty of pwm waveform will be suffered about 3% at most. However, 3% is in the tolerance range, the application of pwm waveform is not sensitive. If the application needs exact duty, the waveform can be generated by PMU. When sleep mode, the clock running at 13MHz is turn-off. Moreover, the clock running at 32kHz is a fixed clock, not a hopping clock.

0x8109_0004h PWM1 max counter value register PWM1_COUNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PWM1_COUNT [12:0]												
Type				R/W												
Reset				1FFFh												

PWM1_COUNT PWM1 max counter value. This value is the initial value for the internal counter. Regardless of the operation mode, if PWM1_COUNT is written while the internal counter is counting backwards, the new initial value does not take effect until the internal counter counts down to zero, i.e. a complete period.

0x8109_0008h PWM1 Threshold Value register PWM1_THRES

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PWM1_THRES [12:0]												
Type				R/W												
Reset				0												

PWM1_THRES Threshold value. When the internal counter value is greater than or equal to PWM1_THRES, the PWM1 output signal is 0; when the internal counter is less than PWM1_THRES, the PWM1 output signal is 1.

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0x8109_000Ch PWM2 Control register PWM2_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CLKSEL	CLK [1:0]	
Type														R/W	R/W	
Reset														0	0	

CLK Select PWM2 clock prescaler scale.

- **00** CLK Hz
- **01** CLK/2 Hz
- **10** CLK/4 Hz
- **11** CLK/8 Hz

Note: When PWM2 module is disabled, its output should be kept in the LOW state.

CLKSEL Select PWM2 clock

- **0** CLK=13M Hz
- **1** CLK=32K Hz

Note: In order to integrate the RF chip into our baseband chip, the clock frequency (CLKSEL=0) is hopping between 13MHz and 14.125MHz, and the clock frequency (CLKSEL=1) is hopping between 32kHz and 34.77kHz. The duty of pwm waveform will be suffered about 3% at most. However, 3% is in the tolerance range, the application of pwm waveform is not sensitive. If the application needs exact duty, the waveform can be generated by PMU. When sleep mode, the clock running at 13MHz is turn-off. Moreover, the clock running at 32kHz is a fixed clock, not a hopping clock.

0x8109_0010h PWM2 max counter value register PWM2_COUNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PWM2_COUNT [12:0]												
Type				R/W												
Reset				1FFFh												

PWM2_COUNT PWM2 max counter value. This value is the initial value for the internal counter. Regardless of the operation mode, if PWM2_COUNT is written while the internal counter is counting backwards, the new initial value does not take effect until the internal counter counts down to zero, i.e. a complete period.

0x8109_0014h PWM2 Threshold Value register PWM2_THRES

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PWM2_THRES [12:0]												
Type				R/W												
Reset				0												

PWM2_THRES Threshold value. When the internal counter value is greater than or equal to PWM2_THRES, the PWM2 output signal is 0; when the internal counter is less than PWM2_THRES, the PWM2 output signal is 1.

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0x8109_0018h PWM3 Control register PWM3_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CLKSEL	CLK [1:0]	
Type														R/W	R/W	
Reset														0	0	

CLK Select PWM3 clock prescaler scale.

- **02** CLK Hz
- **03** CLK/2 Hz
- **10** CLK/4 Hz
- **11** CLK/8 Hz

Note: When PWM3 module is disabled, its output should be kept in the LOW state.

CLKSEL Select PWM3 clock

- **0** CLK=13M Hz
- **1** CLK=32K Hz

Note: In order to integrate the RF chip into our baseband chip, the clock frequency (CLKSEL=0) is hopping between 13MHz and 14.125MHz, and the clock frequency (CLKSEL=1) is hopping between 32kHz and 34.77kHz. The duty of pwm waveform will be suffered about 3% at most. However, 3% is in the tolerance range, the application of pwm waveform is not sensitive. If the application needs exact duty, the waveform can be generated by PMU. When sleep mode, the clock running at 13MHz is turn-off. Moreover, the clock running at 32kHz is a fixed clock, not a hopping clock.

0x8109_001Ch PWM3 max counter value register PWM3_COUNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PWM3_COUNT [12:0]												
Type				R/W												
Reset				1FFFh												

PWM3_COUNT PWM3 max counter value. This value is the initial value for the internal counter. Regardless of the operation mode, if PWM3_COUNT is written while the internal counter is counting backwards, the new initial value does not take effect until the internal counter counts down to zero, i.e. a complete period.

0x8109_0020h PWM3 Threshold Value register PWM3_THRES

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PWM3_THRES [12:0]												
Type				R/W												
Reset				0												

PWM3_THRES Threshold value. When the internal counter value is greater than or equal to PWM3_THRES, the PWM3 output signal is 0; when the internal counter is less than PWM3_THRES, the PWM3 output signal is 1.

Figure 30 shows the PWM waveform with the indicated register values.

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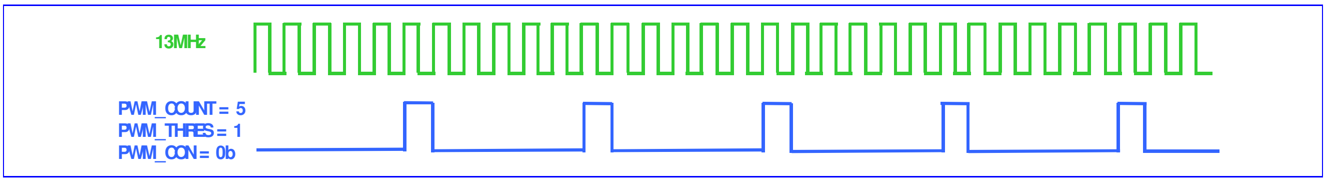

Figure 30 PWM waveform with register values

4.2 Alerter

4.2.1 General Description

The output of Alerter has two sources: one is the enhanced pwm output signal, which is implemented embedded in Alerter module; the other is PDM signal from DSP domain directly. The enhanced pwm with three operation modes is implemented to generate a signal with programmable frequency and tone volume. The frequency and volume are determined by four registers: ALERTER_CNT1, ALERTER_THRES, ALERTER_CNT2 and ALERTER_CON. ALERTER_CNT1 and ALERTER_CNT2 are the initial counting values of internal counter1 and internal counter2 respectively. POWERDOWN signal is applied to power-down the Alerter module. When Alerter is deactivated (POWERDOWN=1), the output will be in low state.

With ALERTER_CON, the output source can be chosen from enhanced pwm or PDM. The waveform of the alerter from enhanced pwm source in different modes can be shown in **Figure 31**. In mode 1, the polarity of alerter output signal according to the relationship between internal counter1 and the programmed threshold will be inverted each time internal counter2 reaches zero. In mode2, each time the internal counter2 count backwards to zero the alerter output signal is normal pwm signal (i.e. signal is low as long as the internal counter1 value is greater than or equals to ALERTER_THRES, and it is high when the internal counter1 is less than ALERTER_THRES) or low state by turns. In mode3, the value of internal counter2 has no effect on output signal, i.e. the alerter output signal is low as long as the internal counter1 value is above the programmed threshold and is high the internal counter1 is less than ALERTER_THRES when no matter what value the internal counter2 is.

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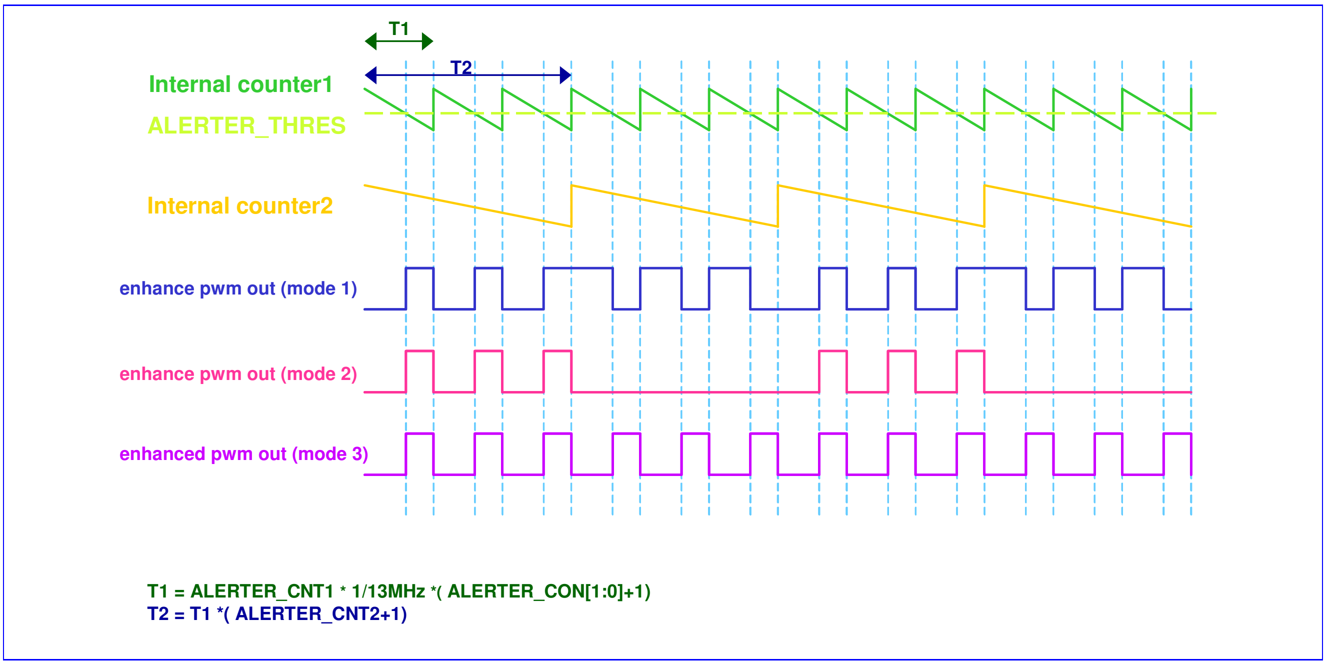

Figure 31 Alerter waveform

The output signal frequency is determined by:

$$\begin{cases} \dfrac{13000000}{2\times(ALERTER_CON[1:0]+1)\times(ALERTER_CNT1+1)\times(ALERTER_CNT2+1)} & \text{for mode 1 and mode 2} \\ \dfrac{13000000}{(ALERTER_CNT1+1)\times(ALERTER_CON[1:0])} & \text{for mode 3} \end{cases}$$

The volume of the output signal is determined by: $\dfrac{ALERTER_THRES}{ALERTER_CNT1+1}$

4.2.2 Register Definitions

0x8107_0000 Alerter counter1 value register ALERTER_CNT1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ALERTER_CNT1 [15:0]															
Type	R/W															
Reset	FFFFh															

ALERTER_CNT1 Alerter max counter's value. ALERTER_CNT1 is the initial value of internal counter1. If ALERTER_CNT1 is written when the internal counter1 is counting backwards, no matter which mode it is, there is no effect until the internal counter1 counts down to zero, i.e. a complete period.

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0x8107_0004 Alerter threshold value register ALERTER_THRES

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ALERTER_THRES [15:0]															
Type	R/W															
Reset	0															

ALERTER_THRES Threshold value. When the internal counter1 value is greater than or equals to ALERTER_THRES, the Alerter output signal will be low state; when the counter1 is less than ALERTER_THRES, the Alerter output signal will be high state.

0x8107_0008 Alerter counter2 value register ALERTER_CNT2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ALERTER_CNT2 [5:0]					
Type											R/W					
Reset											111111b					

AIERTER_CNT2 ALERTER_CNT2 is the initial value for internal counter2. The internal counter2 decreases by one everytime the internal counter1 count down to be zero. The polarity of alerter output signal which depends on the relationship between the internal counter1 and ALERTER_THRES will be inverted anytime when the internal counter2 counts down to zero. E.g. in the beginning, the output signal is low when the internal counter1 isn't less ALERTER_THRES and is high when the internal counter1 is less than ALERTER_THRES. But after the internal counter2 counts down to zero, the output signal will be high when the internal counter1 isn't less than ALERTER_THRES and will be low when the internal counter1 is less than ALERTER_THRES.

0x8107_000C Alerter control register ALERTER_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TYPE				MODE			CLK [1:0]	
Type								R/W				R/W			R/W	
Reset								0				0			0	

CLK Select PWM Waveform clock

00 13M Hz
01 13/2M Hz
10 13/4M Hz
11 13/8M Hz

Note: In order to integrate the RF chip into our baseband chip, the clock frequency is hopping between 13MHz and 14.125MHz. The duty of alerter waveform will be suffered about 3% at most. However, 3% is in the tolerance range, the application of alerter waveform is not sensitive.

MODE Select Alerter mode

00 Mode 1 selected
01 Mode 2 selected

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10 Mode 3 selected

TYPE Select the ALERTER output source from PWM or PDM

0 Output generated from PWM path

1 Output generated from PDM path

Note: When alerter module is power down, its output should be kept in low state.

Figure 32 shows the Alerter waveform with register value present.

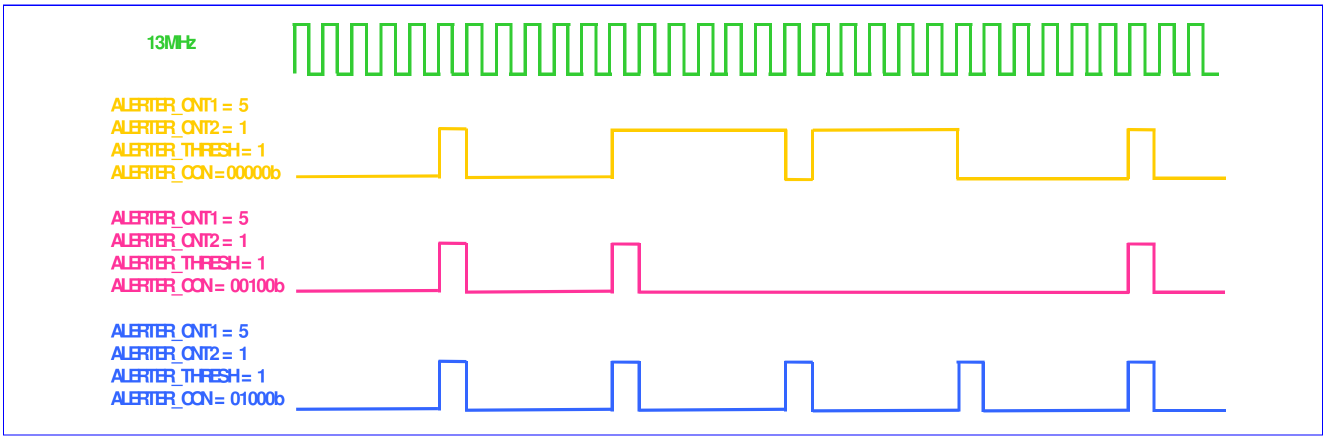

Figure 32 Alerter output signal from enhanced pwm with register value present.

4.3 SIM Interface

The MT6253 contains two dedicated smart card interfaces to allow the MCU to access the two SIM cards. Each interface can operate via 5 terminals. As shown is the **Figure 33**, SIMVCC, SIMSEL, SIMRST, SIMCLK and SIMDATA are for one SIM interface, while SIM2VCC, SIM2SEL, SIM2RST, SIM2CLK and SIM2DATA are for the other one.

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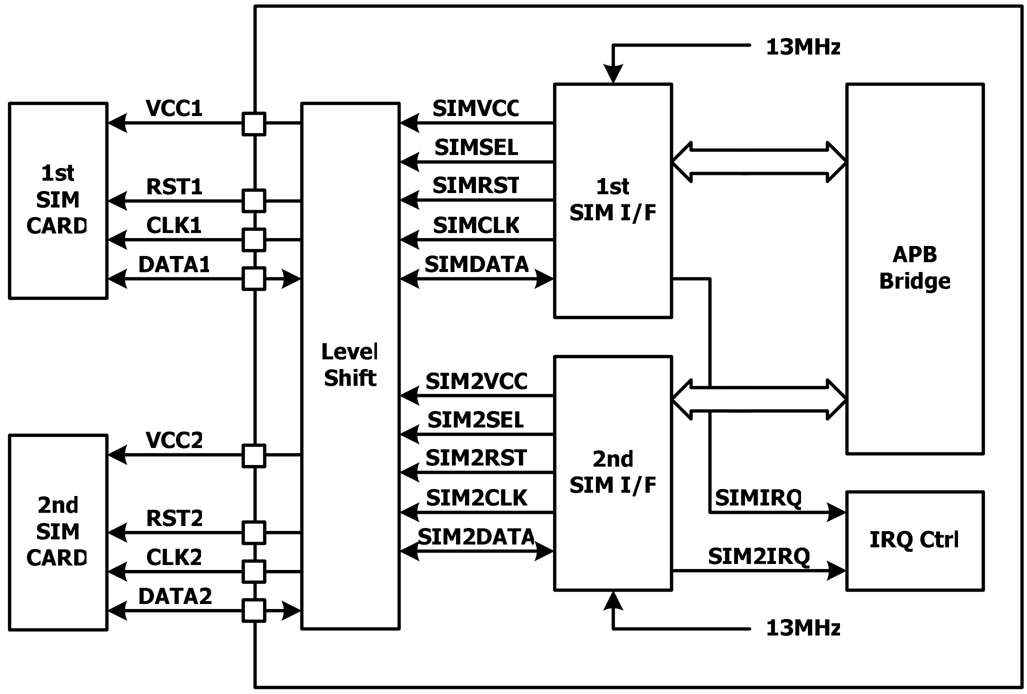

Figure 33 SIM Interface Block Diagram

The functions of the two SIM interfaces are identical; therefore, only first SIM interface will be described in this document. The SIMVCC is used to control the external voltage supply to the SIM card and SIMSEL determines the regulated smart card supply voltage. SIMRST is used as the SIM card reset signal. Besides, SIMDATA and SIMCLK are used for data exchange purpose.

Basically, the SIM interface acts as a half duplex asynchronous communication port and its data format is composed of ten consecutive bits: a start bit in state Low, eight information bits, and a tenth bit used for parity checking. The data format can be divided into two modes as follows:

Direct Convention Mode (ODD=SDIR=SINV=0)

SB D0 D1 D2 D3 D4 D5 D6 D7 PB

SB: Start Bit (in state Low)

Dx: Data Byte (LSB is first and logic level ONE is in state High)

PB: Even Parity Check Bit

Inverse Convention Mode (ODD=SDIR=SINV=1)

SB N7 N6 N5 N4 N3 N2 N1 N0 PB

SB: Start Bit (in state Low)

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***Nx*:** Data Byte (MSB is first and logic level ONE is in state Low)

PB: Odd Parity Check Bit

If the receiver gets a wrong parity bit, it will respond by pulling the SIMDATA Low to inform the transmitter and the transmitter will retransmit the character.

When the receiver is a SIM Card, the error response starts 0.5 bits after the PB and it may last for 1~2 bit periods.

When the receiver is the SIM interface, the error response starts 0.5 bits after the PB and lasts for 1.5 bit period.

When the SIM interface is the transmitter, it will take totally 14 bits guard period whether the error response appears. If the receiver shows the error response, the SIM interface will retransmit the previous character again else it will transmit the next character.

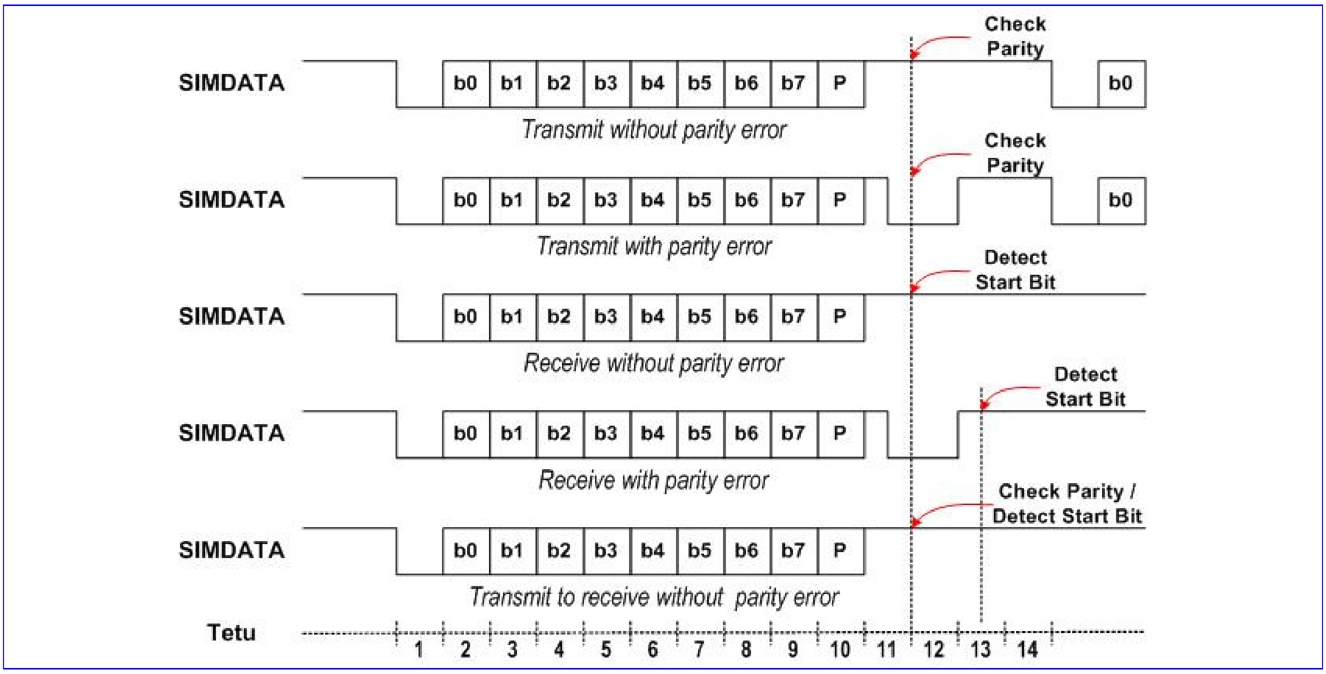

Figure 34 SIM Interface Timing Diagram

4.3.1 Register Definitions

For MCU to control two SIM card interface, all registers are duplicated to two copies but with different base address. In the following, n = “ ” is for 1st SIM card interface, while n=2 is for 2nd SIM card interface. For example, address SIM+0000h is mapped to SIM_SIM_CONT register, while address SIM2+0000h is mapped to SIM2_SIM_CONT register. The base address of 1st SIM card interface is 0x810A0000h, and that of 2nd SIM card interface is 0x81130000h.

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4.3.1.1 Register Overview

MCU Register Address (hex)	Acronym	Discription
1st SIM card Interface		
810A0000h	SIM_SIM_CONT	Control register
810A0004h	SIM_SIM_CONF	Configuration register
810A0008h	SIM_SIM_BRR	Baud rate register
810A0010h	SIM_SIM_IRQEN	Interrupt enable register
810A0014h	SIM_SIM_STS	Status register
810A0020h	SIM_SIM_RETRY	Retry limit register
810A0024h	SIM_SIM_TIDE	FIFO tide mark register
810A0030h	SIM_SIM_DATA	TX/RX data register
810A0034h	SIM_SIM_COUNT	FIFO count register
810A0040h	SIM_SIM_ATIME	Activation time register
810A0044h	SIM_SIM_DTIME	Deactivation time register
810A0048h	SIM_SIM_WTIME	Character to character waiting time register
810A004Ch	SIM_SIM_GTIME	Block to block guard time register
810A0050h	SIM_SIM_ETIME	Block to error signal time register
810A0060h	SIM_SIM_INS	Command header register : INS
810A0064h	SIM_SIM_P3	Command header register : P3
810A0068h	SIM_SIM_SW1	Procedure byte register : SW1
810A006Ch	SIM_SIM_SW2	Procedure byte register : SW2
2nd SIM card Interface		
81130000h	SIM2_SIM_CONT	Control register
81130004h	SIM2_SIM_CONF	Configuration register
81130008h	SIM2_SIM_BRR	Baud rate register
81130010h	SIM2_SIM_IRQEN	Interrupt enable register
81130014h	SIM2_SIM_STS	Status register
81130020h	SIM2_SIM_RETRY	Retry limit register
81130024h	SIM2_SIM_TIDE	FIFO tide mark register
81130030h	SIM2_SIM_DATA	TX/RX data register
81130034h	SIM2_SIM_COUNT	FIFO count register
81130040h	SIM2_SIM_ATIME	Activation time register
81130044h	SIM2_SIM_DTIME	Deactivation time register
81130048h	SIM2_SIM_WTIME	Character to character waiting time register
8113004Ch	SIM2_SIM_GTIME	Block to block guard time register
81130050h	SIM2_SIM_ETIME	Block to error signal time register

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MCU Register Address (hex)	Acronym	Discription
81130060h	SIM2_SIM_INS	Command header register : INS
81130064h	SIM2_SIM_P3	Command header register : P3
81130068h	SIM2_SIM_SW1	Procedure byte register : SW1
8113006Ch	SIM2_SIM_SW2	Procedure byte register : SW2

4.3.1.2 Register Description

SIMn+0000h SIM module control register SIMN_SIM_CONT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														WRST	CSTOP	SIMON
Type														W	R/W	R/W
Reset														0	0	0

SIMON SIM card power-up/power-down control

0 An 1-to-0 change will start the card deactivation sequence

1 A 0-to-1 change will start the card activation sequence

CSTOP Enable clock stop mode. Together with CPOL in SIM_CONF register, it determines the polarity of the SIMCLK in this mode.

0 Enable the SIMCLK output.

1 Disable the SIMCLK output

WRST SIM card warm reset control

SIMn+0004h SIM module configuration register SIMN_SIM_CONF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						HFEN	T0EN	T1EN	TOUT	SIMSEL	ODD	SDIR	SINV	CPOL	TXACK	RXACK
Type						R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset						0	0	0	0	0	0	0	0	0	0	0

RXACK SIM card reception error handshake control

0 Disable character receipt handshaking

1 Enable character receipt handshaking

TXACK SIM card transmission error handshake control

0 Disable character transmission handshaking

1 Enable character transmission handshaking

CPOL SIMCLK polarity control in clock stop mode

0 Make SIMCLK stop in LOW level

1 Make SIMCLK stop in HIGH level

SINV Data invert mode

0 Not invert the transmitted and received data, data logic ONE is in high state

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1 Invert the transmitted and received data, data logic ONE is in low state

SDIR Data Transfer Direction
- **0** LSB is transmitted and received first
- **1** MSB is transmitted and received first

ODD Select odd or even parity
- **0** Even parity
- **1** Odd parity

SIMSEL SIM card supply voltage select
- **0** SIMSEL pin is set to LOW level, 1.8V
- **1** SIMSEL pin is set to HIGH level, 3V

TOUT SIM work waiting time counter control
- **0** Disable Time-Out counter
- **1** Enable Time-Out counter

T1EN T=1 protocol controller control
- **0** Disable T=1 protocol controller
- **1** Enable T=1 protocol controller

T0EN T=0 protocol controller control
- **0** Disable T=0 protocol controller
- **1** Enable T=0 protocol controller

HFEN Hardware flow control
- **0** Disable hardware flow control
- **1** Enable hardware flow control

SIMn +0008h SIM Baud Rate Register SIMN_SIM_BRR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						ETU[8:0]									SIMCLK[1:0]	
Type						R/W									R/W	
Reset						372d									01	

SIMCLK Set SIMCLK frequency
- **00** 13/2 MHz
- **01** 13/4 MHz
- **10** 13/8 MHz
- **11** 13/12 MHz

ETU Determines the duration of elementary time unit in unit of SIMCLK

SIMn +0010h SIM interrupt enable register SIMN_SIM_IRQEN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						EDCERR	T1END	RXERR	T0END	SIMOFF	ATRERR	TXERR	TOUT	OVRUN	RXTIDE	TXTIDE
Type						R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset						0	0	0	0	0	0	0	0	0	0	0

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For all these bits

- **0** Interrupt is disabled
- **1** Interrupt is enabled

SIMn +0014h SIM module status register SIMN_SIM_STS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						EDCERR	T1END	RXERR	T0END	SIMOFF	ATRERR	TXERR	TOUT	OVRUN	RXTIDE	TXTIDE
Type						R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R	R
Reset						—	—	—	—	—	—	—	—	—	—	—

TXTIDE The interrupt occurs when number of transmitted data in the FIFO is less than transmitted tide.
RXTIDE The interrupt occurs when number of received data in the FIFO is less than received tide.
OVRUN Receive FIFO overflow interrupt occurred
TOUT Between characters timeout interrupt occurred
TXERR Character transmission error interrupt occurred
ATRERR ATR start time-out interrupt occurred
SIMOFF Card deactivation complete interrupt occurred
T0END Data Transfer handled by T=0 Controller completed interrupt occurred
RXERR Character reception error interrupt occurred
T1END Data Transfer handled by T=1 Controller completed interrupt occurred
EDCERR T=1 Controller CRC error occurred

SIMn +0020h SIM retry limit register SIMN_SIM_RETRY

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						TXRETRY								RXRETRY		
Type						R/W								R/W		
Reset						3h								3h		

RXRETRY Specify the maximum numbers of receive retries that are allowed when parity error has occurred.
TXRETRY Specify the maximum numbers of transmit retries that are allowed when parity error has occurred.

SIMn +0024h SIM FIFO tide mark register SIMN_SIM_TIDE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TXTIDE[3:0]								RXTIDE[3:0]			
Type					R/W								R/W			
Reset					0h								0h			

RXTIDE Trigger point of RXTIDE interrupt
TXTIDE Trigger point of TXTIDE interrupt

SIMn +0030h Data register used as Tx/Rx Data Register SIMN_SIM_DATA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DATA[7:0]							
Type									R/W							

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Reset									—							

DATA Eight data digits. These correspond to the character being read or written

SIMn +0034h SIM FIFO count register SIMN_SIM_COUNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												COUNT[4:0]				
Type												R/W				
Reset												0h				

COUNT The number of characters in the SIM FIFO when read, and flushes when written.

SIMn +0040h SIM activation time register SIMN_SIM_ATIME

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ATIME[15:0]															
Type	R/W															
Reset	AFC7h															

ATIME The register defines the duration, in SIM clock cycles, of the time taken for each of the three stages of the card activation process, from SIMON transits to high to turn on VCC, from turn on VCC to pull DATA high and then from pull DATA high to turn on CLK.

SIMn +0044h SIM deactivation time register SIMN_SIM_DTIME

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DTIME[11:0]											
Type					R/W											
Reset					3E7h											

DTIME The register defines the duration, in 13MHz clock cycles, of the time taken for each of the three stages of the card deactivation sequence, from pull RST low to turn of CLK, from turn off CLK to pull DATA low, from pull DATA low to turn off to turn off VCC.

SIMn +0048h Character to character waiting time register SIMN_SIM_WTIME

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WTIME[15:0]															
Type	R/W															
Reset	983h															

WTIME Maximum interval between the leading edge of two consecutive characters in 4 ETU unit

SIMn +004Ch Block to block guard time register SIMN_SIM_GTIME

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													GTIME			
Type													R/W			
Reset													10d			

GTIME Minimum interval between the leading edge of two consecutive characters sent in opposite directions in ETU unit

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SIMn +0050h Block to error signal time register SIMN_SIM_ETIME

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ETIME					
Type											R/W					
Reset											15d					

ETIME The register defines the interval, in 1/16 ETU unit, between the end of transmitted parity bit and time to check parity error signal sent from SIM card.

SIMn +0060h SIM command header register: INS SIMN_SIM_INS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								INSD	SIMINS[7:0]							
Type								R/W	R/W							
Reset								0h	0h							

SIMINS This field should be identical to the INS instruction code. When writing to this register, the T=0 controller will be activated and data transfer will be initiated.

INSD [Description for this register field]

0 T=0 controller receives data from the SIM card

1 T=0 controller sends data to the SIM card

SIMn +0064h SIM command header register: P3 SIMN_SIM_P3 (ICC_LEN)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								SIMP3[8:0]								
Type								R/W								
Reset								0h								

SIMP3 This field should be identical to the P3 instruction code. It should be written prior to the SIM_INS register. While the data transfer is going on, this field shows the no. of the remaining data to be sent or to be received

SIMn +0068h SIM procedure byte register: SW1 SIMN_SIM_SW1 (ICC_LEN)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SIMSW1[7:0]							
Type									R							
Reset									0h							

SIMSW1 This field holds the last received procedure byte for debug purpose. When the T0END interrupt occurred, it keeps the SW1 procedure byte.

SIMn +006Ch SIM procedure byte register: SW2 SIMN_SIM_SW2 (ICC_EDC)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SIMSW2[7:0]							
Type									R							
Reset									0h							

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SIMSW2 This field holds the SW2 procedure byte

4.3.2 SIM Card Insertion and Removal

The detection of physical connection to the SIM card and card removal is done by the external interrupt controller or by GPIO.

4.3.3 Card Activation and Deactivation

The card activation and deactivation sequence both are controlled by H/W. The MCU initiates the activation sequence by writing a “1” to bit 0 of the SIM_CON register, and then the interface performs the following activation sequence:

- Assert SIMRST LOW
- Set SIMVCC at HIGH level and SIMDATA in reception mode
- Enable SIMCLK clock
- De-assert SIMRST HIGH (required if it belongs to active low reset SIM card)

The final step in a typical card session is contact deactivation in order that the card is not electrically damaged. The deactivation sequence is initiated by writing a “0” to bit 0 of the SIM_CONT register, and then the interface performs the following deactivation sequence:

- Assert SIMRST LOW
- Set SCIMCLK at LOW level
- Set SIMDATA at LOW level
- Set SIMVCC at LOW level

4.3.4 Answer to Reset Sequence

After card activation, a reset operation results in an answer from the card consisting of the initial character TS, followed by at most 32 characters. The initial character TS provides a bit synchronization sequence and defines the conventions to interpret data bytes in all subsequent characters.

On reception of the first character, TS, MCU should read this character, establish the respective required convention and reprogram the related registers. These processes should be completed prior to the completion of reception of the next character. And then, the remainder of the ATR sequence is received, read via the SIM_DATA in the selected convention and interpreted by the S/W.

The timing requirement and procedures for ATR sequence are handled by H/W and shall meet the requirement of ISO 7816-3 as shown in **Figure 35**.

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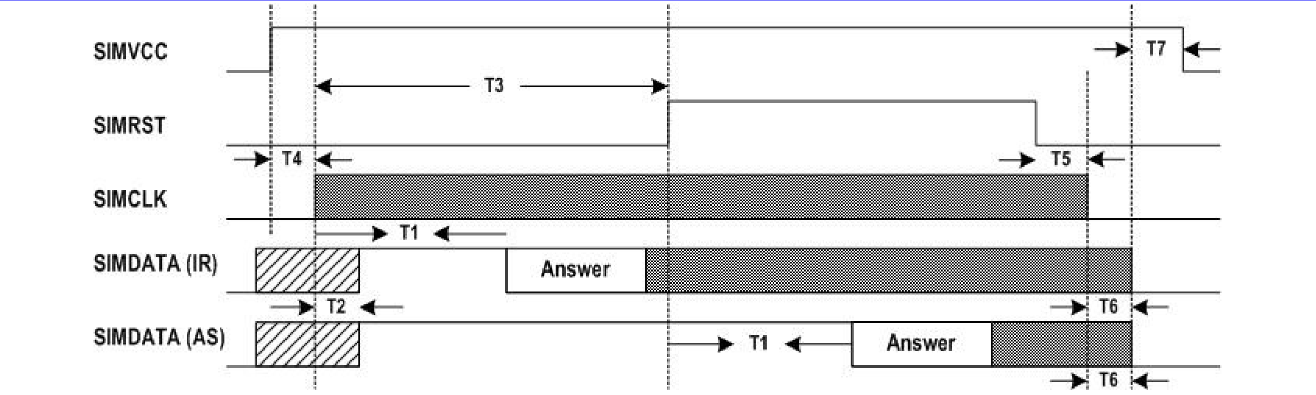

Figure 35 Answer to Reset Sequence

Time	Value	Comment
T1	> 400 SIMCLK	SIMCLK start to ATR appear
T2	< 200 SIMCLK	SIMCLK start to SIMDATA in reception mode
T3	> 40000 SIMCLK	SIMCLK start to SIMRST High
T4	—	SIMVCC High to SIMCLK start
T5	—	SIMRST Low to SIMCLK stop
T6	—	SIMCLK stop to SIMDATA Low
T7	—	SIMDATA Low to SIMVCC Low

Table 22 Answer to Reset Sequence Time-Out Condition

4.3.5 SIM Data Transfer

Two transfer modes are provided, either in software controlled byte by byte fashion or in a block fashion using T=0 controller and DMA controller. In both modes, the time-out counter could be enabled to monitor the elapsed time between two consecutive bytes.

4.3.5.1 Byte Transfer Mode

This mode is used during ATR and PPS procedure. In this mode, the SIM interface only ensures error free character transmission and reception.

Receiving Character

Upon detection of the start-bit sent by SIM card, the interface transforms into reception mode and the following bits are shifted into an internal register. If no parity error is detected or character-receive handshaking is disabled, the received-character is written into the SIM FIFO and the SIM_COUNT register is increased by one. Otherwise, the SIMDATA line is held low at 0.5 etu after detecting the parity error for 1.5 etus, and the character is re-received. If a

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character fails to be received correctly for the RXRETRY times, the receive-handshaking is aborted and the last-received character is written into the SIM FIFO, the SIM_COUNT is increased by one and the RXERR interrupt is generated

When the number of characters held in the receive FIFO exceeds the level defined in the SIM_TIDE register, a RXTIDE interrupt is generated. The number of characters held in the SIM FIFO can be determined by reading the SIM_COUNT register and writing to this register will flush the SIM FIFO.

Sending Character

Characters that are to be sent to the card are first written into the SIM FIFO and then automatically transmitted to the card at timed intervals. If character-transmit handshaking is enabled, the SIMDATA line is sampled at 1 etu after the parity bit. If the card indicates that it did not receive the character correctly, the character is retransmitted a maximum of TXRETRY times before a TXERR interrupt is generated and the transmission is aborted. Otherwise, the succeeding byte in the SIM FIFO is transmitted.

If a character fails to be transmitted and a TXERR interrupt is generated, the interface needs to be reset by flushing the SIM FIFO before any subsequent transmit or receive operation.

When the number of characters held in the SIM FIFO falls below the level defined in the SIM_TIDE register, a TXTIDE interrupt is generated. The number of characters held in the SIM FIFO can be determined by reading the SIM_COUNT register and writing to this register will flush the SIM FIFO.

4.3.5.2 Block Transfer Mode

Basically, the SIM interface is designed to work in conjunction with the T=0 protocol controller and the DMA controller during non-ATR and non-PPS phase, though it is still possible for software to service the data transfer manually like in byte transfer mode if necessary and thus the T=0 protocol should be controlled by software.

The T=0 controller is accessed via four registers representing the instruction header bytes INS and P3, and the procedure bytes SW1 and SW2. These registers are:

SIM_INS, SIM_P3

SIM_SW1, SIM_SW2

During characters transfer, SIM_P3 holds the number of characters to be sent or to be received and SIM_SW1 holds the last received procedure byte including NULL, ACK, NACK and SW1 for debug purpose.

Data Receive Instruction

Data Receive Instructions receive data from the SIM card. It is instantiated as the following procedure.

```
1. Enable the T=0 protocol controller by setting the T0EN bit to 1 in SIM_CONF register
2. Program the SIM_TIDE register to 0x0000 (TXTIDE = 0, RXTIDE = 0)
3. Program the SIM_IRQEN to 0x019C (Enable RXERR, TXERR, T0END, TOUT and OVRUN interrupts)
4. Write CLA, INS, P1, P2 and P3 into SIM FIFO
5. Program the DMA controller :
   DMAn_MSBSRC and DMAn_LSBSRC : address of SIM_DATA register
```


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```
    DMAn_MSBDST and DMAn_LSBDST : memory address reserved to store the received characters
    DMAn_COUNT : identical to P3 or 256 (if P3 == 0)
    DMAn_CON : 0x0078
6.  Write P3 into SIM_P3 register and then INS into SIM_INS register (Data Transfer is initiated
    now)
7.  Enable the Time-out counter by setting the TOUT bit to 1 in SIM_CONF register
8.  Start the DMA controller by writing 0x8000 into the DMAn_START register to
```

Upon completion of the Data Receive Instruction, T0END interrupt will be generated and then the Time-out counter should be disabled by setting the TOUT bit back to 0 in SIM_CONF register.

If error occurs during data transfer (RXERR, TXERR, OVRUN or TOUT interrupt is generated), the SIM card should be deactivated first and then activated prior subsequent operations.

Data Send Instruction

Data Send Instructions send data to the SIM card. It is instantiated as the following procedure.

```
1.  Enable the T=0 protocol controller by setting the T0EN bit to 1 in SIM_CONF register
2.  Program the SIM_TIDE register to 0x0100 (TXTIDE = 1, RXTIDE = 0)
3.  Program the SIM_IRQEN to 0x019C (Enable RXERR, TXERR, T0END, TOUT and OVRUN interrupts)
4.  Write CLA, INS, P1, P2 and P3 into SIM FIFO
5.  Program the DMA controller :
    DMAn_MSBSRC and DMAn_LSBSRC : memory address reserved to store the transmitted characters
    DMAn_MSBDST and DMAn_LSBDST : address of SIM_DATA register
    DMAn_COUNT : identical to P3
    DMAn_CON : 0x0074
6.  Write P3 into SIM_P3 register and then (0x0100 | INS) into SIM_INS register (Data Transfer
    is initiated now)
7.  Enable the Time-out counter by setting the TOUT bit to 1 in SIM_CONF register
8.  Start the DMA controller by writing 0x8000 into the DMAn_START register
```

Upon completion of the Data Send Instruction, T0END interrupt will be generated and then the Time-out counter should be disabled by setting the TOUT bit back to 0 in SIM_CONF register.

If error occurs during data transfer (RXERR, TXERR, OVRUN or TOUT interrupt is generated), the SIM card should be deactivated first and then activated prior subsequent operations.

4.4 Keypad Scanner

4.4.1 General Description

The keypad can be divided into two parts: one is the keypad interface including 7 columns and 6 rows with one dedicated power-key, as shown in **Figure 36**; the other is the key detection block which provides key pressed, key released and de-bounce mechanisms. Each time the key is pressed or released, i.e. something different in the 6 x 7 matrix or power-key, the key detection block senses the change and recognizes if a key has been pressed or released. Whenever the key status changes and is stable, a KEYPAD IRQ is issued. The MCU can then read the key(s) pressed directly in KP_MEM1,

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KP_MEM2, KP_MEM3, and KP_MEM4 registers. To ensure that the key pressed information is not missed, the status register in keypad is not read-cleared by APB read command. The status register can only be changed by the key-pressed detection FSM.

This keypad can detect one or two key-pressed simultaneously with any combination. **Figure 37** shows one key pressed condition. **Figure 38**(a) and **Figure 38**(b) illustrate two keys pressed cases. Since the key press detection depends on the HIGH or LOW level of the external keypad interface, if keys are pressed at the same time and there exists a key that is on the same column and the same row with the other keys, the pressed key cannot be correctly decoded. For example, if there are three key presses: key1 = (x1, y1), key2 = (x2, y2), and key3 = (x1, y2), then both key3 and key4 = (x2, y1) are detected, and therefore they cannot be distinguished correctly. Hence, the keypad can detect only one or two keys pressed simultaneously at any combination. More than two keys pressed simultaneously in a specific pattern retrieve the wrong information.

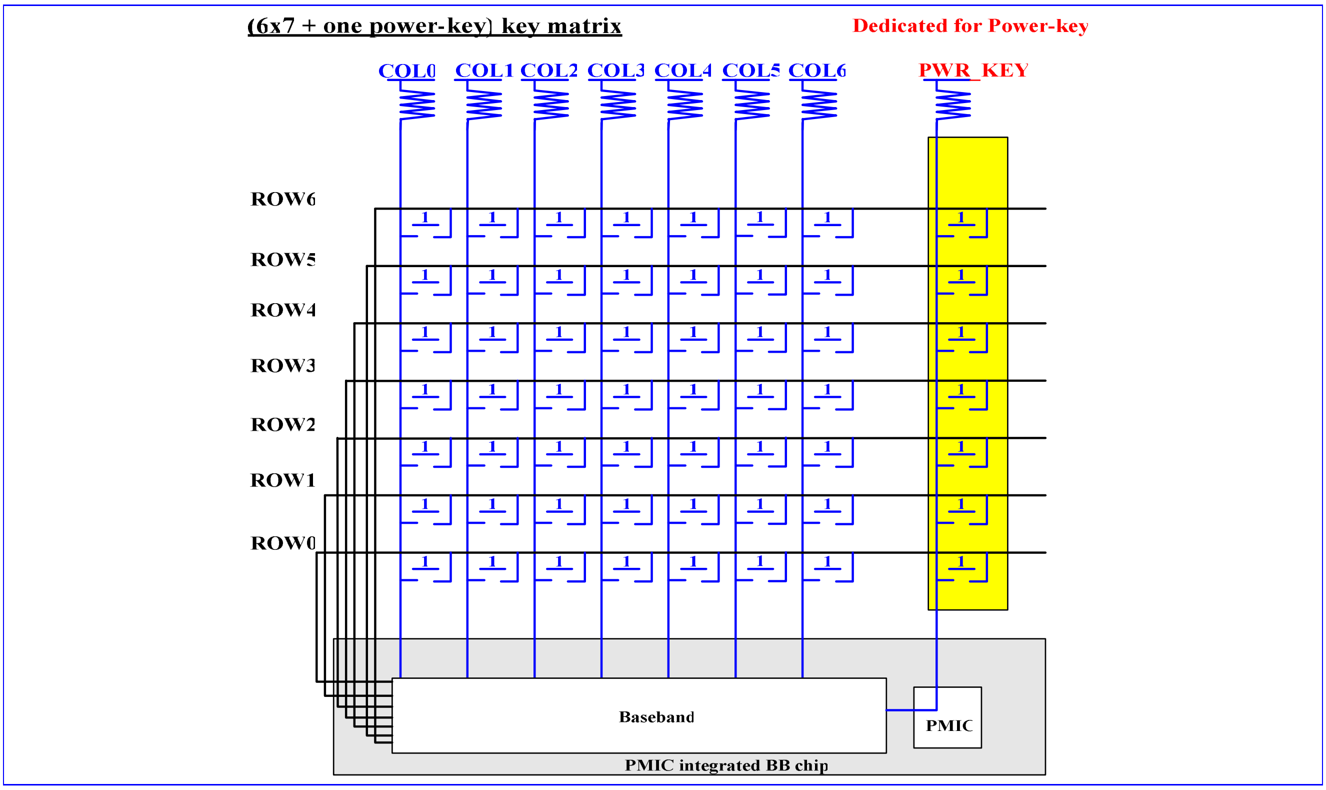

Figure 36 6x7 matrix with one power-key

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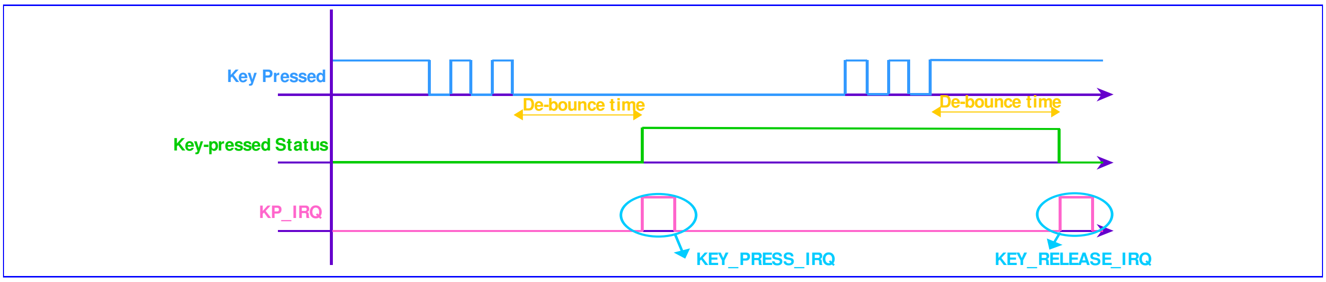

Figure 37 One key pressed with de-bounce mechanism denoted

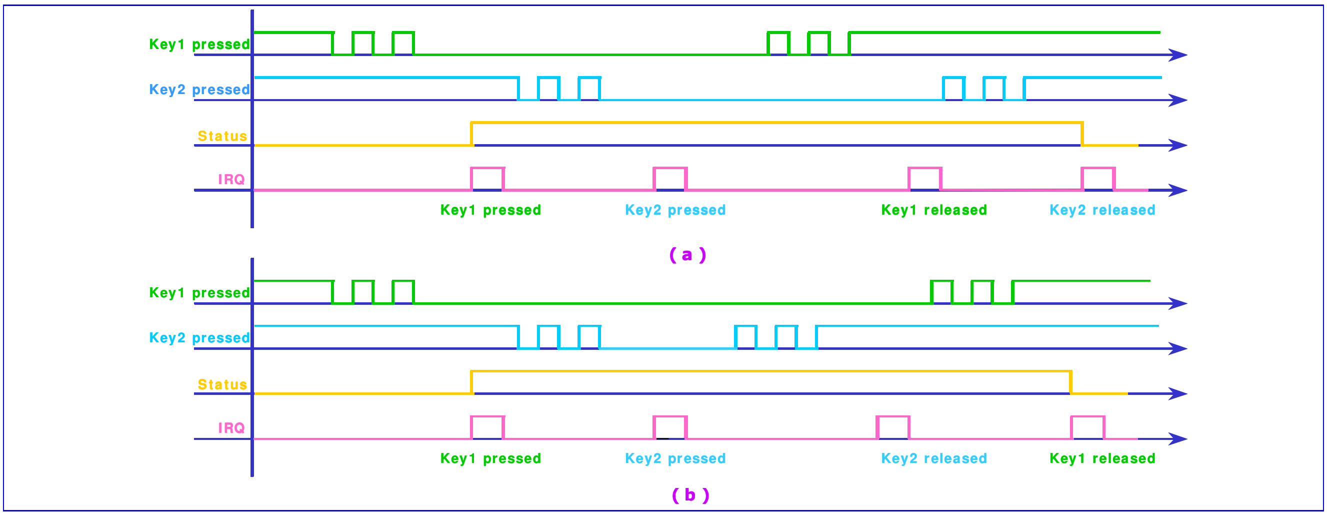

Figure 38 Two keys pressed, case 1 (b) Two keys pressed, case 2

4.4.2 Register Definitions

KP +0000h Keypad status KP_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STA
Type																RO
Reset																0

STA This register indicates the keypad status. The register is not cleared by the read operation.

0 No key pressed

1 Key pressed

KP +0004h Keypad scanning output Register KP_MEM1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY 15	KEY 14	KEY 13	KEY 12	KEY 11	KEY 10	KEY 9	KEY 8	KEY 7	KEY 6	KEY 5	KEY 4	KEY 3	KEY 2	KEY 1	KEY 0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

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Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

KEY0~15 The register shows up the key-press status of key0(LSB)~key15. Please reference **Table 23**
.

KP +0008h Keypad scanning output Register KP_MEM2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY 31	KEY 30	KEY 29	KEY 28	KEY 27	KEY 26	KEY 25	KEY 24	KEY 23	KEY 22	KEY 21	KEY 20	KEY 19	KEY 18	KEY 17	KEY 16
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

KEY16~31 The register shows up the key-press status of key16(LSB)~key31. Please reference **Table 23**

KP +000Ch Keypad scanning output Register KP_MEM3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY 47	KEY 46	KEY 45	KEY 44	KEY 43	KEY 42	KEY 41	KEY 40	KEY 39	KEY 38	KEY 37	KEY 36	KEY 35	KEY 34	KEY 33	KEY 32
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

KEY32~47 The register shows up the key-press status of key32(LSB)~key47. Please reference **Table 23**

KP +0010h Keypad scanning output Register KP_MEM4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											KEY 53	KEY 52	KEY 51	KEY 50	KEY 49	KEY 48
Type											RO	RO	RO	RO	RO	RO
Reset											1	1	1	1	1	1

KEY48~53 The register shows up the key-press status of key48(LSB)~key53. Please reference **Table 23**
These four registers list the status of 54 keys on the keypad but KEY[8], KEY[17], KEY[26], KEY[35], KEY[44] , KEY[53] is dedicated for power key and KEY[7], KEY[16], KEY[25], KEY[34], KEY[52] is not available. When the MCU receives the KEYPAD IRQ, both two registers must be read. If any key is pressed, the relative bit is set to 0.

In order to work normally, the corresponding pull-up/down setting must be programmed correctly. If some keys can be use because their COL or ROW is use as GPIO, these corresponding bit will be tie to high.

KEYS Status list of the 54 keys.

KP +00018h De-bounce period setting KP_DEBOUNCE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEBOUNCE [13:0]													
Type			R/W													
Reset			400h													

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This register defines the waiting period before key press or release events are considered stale. If debounce setting is too small, keypad will be too sensitive and detect too many unexpected key-press. The suitable debounce time setting must be adjust for the user's habit.

DEBOUNCE De-bounce time = KP_DEBOUNCE*(1/32k) sec. 32 kHz is the working clock frequency of keypad module.

	COL0	COL1	COL2	COL3	COL4	COL5	COL6	COL7	PWRKEY
ROW5	45	46	47	48	49	50	51	52	53
ROW4	36	37	38	39	40	41	42	43	44
ROW3	27	28	29	30	31	32	33	34	35
ROW2	18	19	20	21	22	23	24	25	26
ROW1	9	10	11	12	13	14	15	16	17
ROW0	0	1	2	3	4	5	6	7	8

Table 23 KEY's order number in COL/ROW matrix.

4.5 General Purpose Inputs/Outputs

MT6253 offers 83 general-purpose I/O pins. By setting the control registers, MCU software can control the direction, the output value, and read the input values on these pins. These GPIOs and GPOs are multiplexed with other functionalities to reduce the pin count. To further reduce pin count, the GPIO setting is split into two scenarios, auxiliary function mode and debug mode. Depending on the GPIO_BANK(0x8002_0230) bit, overall GPIO setting can alternate between two modes (default is aux. Functional mode). However, leave some GPIO to be in auxiliary function mode while others are in debug mode is prohibited. In addition, all GPO pins are removed. To facilitate application use, software can configure which clock to send outside the chip. There are 6 clock-out ports embedded in 83 GPIO pins, and each clock-out can be programmed to output appropriate clock source.

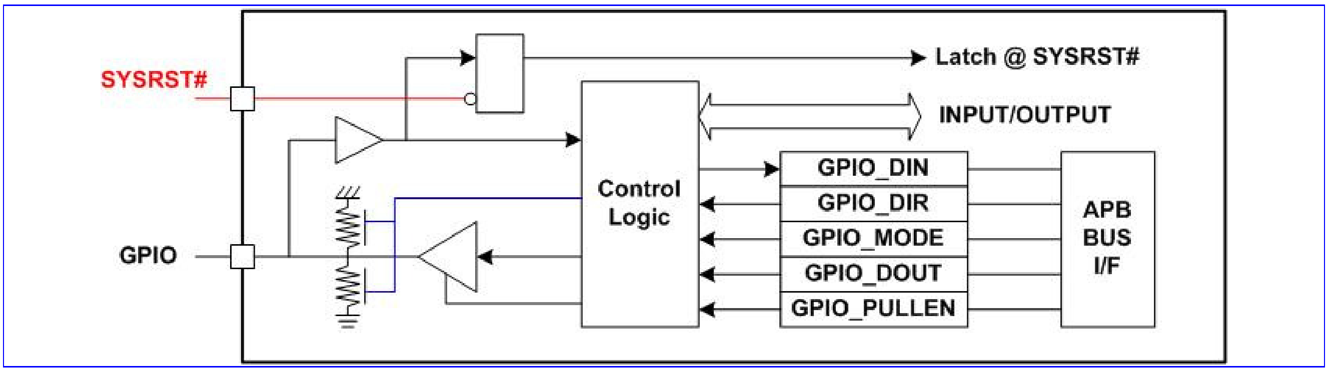

Figure 39 GPIO Block Diagram

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GPIOs at RESET

Upon hardware reset (SYSRST#), GPIOs are all configured as inputs and the following alternative usages of GPIO pins are enabled:

These GPIOs are used to latch the inputs upon reset to memorize the desired configuration to make sure that the system restarts or boots in the right mode.

4.5.1 Register Definitions

0x8002_0000 GPIO direction control register 1 GPIO_DIR1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

0x8002_0010 GPIO direction control register 2 GPIO_DIR2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	PGIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8002_0020 GPIO direction control register 3 GPIO_DIR3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8002_0030 GPIO direction control register 4 GPIO_DIR4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO63	GPIO62	GPIO61	GPIO60	GPIO59	GPIO58	GPIO57	GPIO56	GPIO55	GPIO54	GPIO53	GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8002_0040 GPIO direction control register 5 GPIO_DIR5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO79	GPIO78	GPIO77	GPIO76	GPIO75	GPIO74	GPIO73	GPIO72	GPIO71	GPIO70	GPIO69	GPIO68	GPIO67	GPIO66	GPIO65	GPIO64
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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0x8002_0380 GPIO direction control register 6 GPIO_DIR6

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														GPIO82	GPIO81	GPIO80
Type														R/W	R/W	R/W
Reset														0	0	0

GPIO*n* GPIO direction control

- **0** GPIOs are configured as input
- **1** GPIOs are configured as output

0x8002_0050 GPIO pull-up/pull-down enable register 1 GPIO_PULLEN1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0

0x8002_0060 GPIO pull-up/pull-down enable register 2 GPIO_PULLEN2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	PGIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	1	1	1	1	1	1	0	1	1	1

0x8002_0070 GPIO pull-up/pull-down enable register 3 GPIO_PULLEN3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

0x8002_0080 GPIO pull-up/pull-down enable register 4 GPIO_PULLEN4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO63	GPIO62	GPIO61	GPIO60	GPIO59	GPIO58	GPIO57	GPIO56	GPIO55	GPIO54	GPIO53	GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

0x8002_0090 GPIO pull-up/pull-down enable register 5 GPIO_PULLEN5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO79	GPIO78	GPIO77	GPIO76	GPIO75	GPIO74	GPIO73	GPIO72	GPIO71	GPIO70	GPIO69	GPIO68	GPIO67	GPIO66	GPIO65	GPIO64
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

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0x8002_0390 GPIO pull-up/pull-down enable register 6 GPIO_PULLEN6

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														GPIO82	GPIO81	GPIO80
Type														R/W	R/W	R/W
Reset														1	1	1

GPIO*n* GPIO pull up/down enable

- **0** GPIOs pull up/down is not enabled
- **1** GPIOs pull up/down is enabled

0x8002_00A0 GPIO data inversion control register 1 GPIO_DINV1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INV15	INV14	INV13	INV12	INV11	INV10	INV9	INV8	INV7	INV6	INV5	INV4	INV3	INV2	INV1	INV0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8002_00B0 GPIO data inversion control register 2 GPIO_DINV2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INV31	INV30	INV29	INV28	INV27	INV26	INV25	INV24	INV23	INV22	INV21	INV20	INV19	IVN18	INV17	INV16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8002_00C0 GPIO data inversion control register 3 GPIO_DINV3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INV47	INV46	INV45	INV44	INV43	INV42	INV41	INV40	INV39	INV38	INV37	INV36	INV35	INV34	INV33	INV32
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8002_00D0 GPIO data inversion control register 4 GPIO_DINV4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INV63	INV62	INV61	INV60	INV59	INV58	INV57	INV56	INV55	INV54	INV53	INV52	INV51	INV50	INV49	INV48
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8002_00E0 GPIO data inversion control register 5 GPIO_DINV5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INV79	INV78	INV77	INV76	INV75	INV74	INV73	INV72	INV71	INV70	INV69	INV68	INV67	INV66	INV65	INV64
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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0x8002_03A0 GPIO data inversion control register 6 GPIO_DINV6

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INV82	INV81	INV80
Type														R/W	R/W	R/W
Reset														0	0	0

INVn GPIO inversion control

- **0** GPIOs data inversion disable
- **1** GPIOs data inversion enable

0x8002_00F0 GPIO data output register 1 GPIO_DOUT1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8002_0100 GPIO data output register 2 GPIO_DOUT2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	PGIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8002_0110 GPIO data output register 3 GPIO_DOUT3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8002_0120 GPIO data output register 4 GPIO_DOUT4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO63	GPIO62	GPIO61	GPIO60	GPIO59	GPIO58	GPIO57	GPIO56	GPIO55	GPIO54	GPIO53	GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8002_0130 GPIO data output register 5 GPIO_DOUT5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO79	GPIO78	GPIO77	GPIO76	GPIO75	GPIO74	GPIO73	GPIO72	GPIO71	GPIO70	GPIO69	GPIO68	GPIO67	GPIO66	GPIO65	GPIO64
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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0x8002_03B0 GPIO data output register 6 GPIO_DOUT6

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														GPIO82	GPIO81	GPIO80
Type														R/W	R/W	R/W
Reset														0	0	0

GPIOn GPIO data output control

- **0** GPIOs data output 0
- **1** GPIOs data output 1

0x8002_0140 GPIO data Input register 1 GPIO_DIN1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

0x8002_0150 GPIO data Input register 2 GPIO_DIN2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	PGIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

0x8002_0160 GPIO data Input register 3 GPIO_DIN3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

0x8002_0170 GPIO data input register 4 GPIO_DIN4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO63	GPIO62	GPIO61	GPIO60	GPIO59	GPIO58	GPIO57	GPIO56	GPIO55	GPIO54	GPIO53	GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

0x8002_0180 GPIO data input register 5 GPIO_DIN5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO79	GPIO78	GPIO77	GPIO76	GPIO75	GPIO74	GPIO73	GPIO72	GPIO71	GPIO70	GPIO69	GPIO68	GPIO67	GPIO66	GPIO65	GPIO64
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

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0x8002_03C0 GPIO data input register 6 GPIO_DIN6

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														GPIO82	GPIO81	GPIO80
Type														R/W	R/W	R/W
Reset														0	0	0

GPIOn GPIOs data input

GPIO+0230h GPIO bank GPIO_BANK

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BANK
Type																R/W
Reset																1

BANK Configure the GPIO sets to auxiliary function mode or to debug mode

- **0** debug mode
- **1** auxiliary function mode

GPIO+0300h CLK_OUT0 setting CLKO_MODE1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CLKOUT			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

CLKOUT select the clock output source

- **1** f26m_ck
- **2** f13m_ck
- **3** f65m_ck, 6.5MHz
- **4** f32k_ck
- **5** dsp1_ck
- **6** dsp2_ck
- **7** mcu_hclk_ck
- **8** ahb_hclk_ck
- **9** slow_ck
- **A** fmcu_ck, PLL output, 104MHz
- **B** fdsp_ck, PLL output, 104MHz
- **C** fusb_ck, USB PHY clock output, 30MHz
- **D** fgsm_ck, GPLL output, 104MHz

GPIO+0310h CLK_OUT1 setting CLKO_MODE2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CLKOUT			

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Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIO+0320h CLK_OUT2 setting CLKO_MODE3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CLKOUT			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

GPIO+0330h CLK_OUT3 setting CLKO_MODE4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CLKOUT			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

GPIO+0340h CLK_OUT4 setting CLKO_MODE5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CLKOUT			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

GPIO+0350h CLK_OUT5 setting CLKO_MODE6

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CLKOUT			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

GPIO+0360h CLK_OUT6 setting CLKO_MODE7

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CLKOUT			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

0x8002_0190 GPIO mode control register 1 GPIO_MODE1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO7_M		GPIO6_M		GPIO5_M		GPIO4_M		GPIO3_M		GPIO2_M		GPIO1_M		GPIO0_M	
Type	R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
Reset	01		01		01		01		01		01		01		10	

GPIO0_M GPIO mode selection

- **00** Configured as GPIO function
- **01** PWM1 output
- **10** CLKSQ_SEL if GPIO_BANK is 1, SWDBG data bit 1 if GPIO_BANK is 0

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11 Alerter if GPIO_BANK is 1, slave DSP task ID 6 data bit 1 if GPIO_BANK is 0
GPIO1_M GPIO mode selection
00 Configured as GPIO function
01 Key-pad column 6, KCOL6
10 External interrupt 4, EINT4
11 Reserved
GPIO2_M GPIO mode selection
00 Configured as GPIO function
01 Key-pad column 5, KCOL5
10 Reserved
11 Reserved
GPIO3_M GPIO mode selection
00 Configured as GPIO function
01 Key-pad column 4, KCOL4
10 CLK_OUT1 if GPIO_BANK is 1, SWDBG data bit 2 if GPIO_BANK is 0
11 Reserved
GPIO4_M GPIO mode selection
00 Configured as GPIO function
01 Key-pad column 3, KCOL3
10 Reserved if GPIO_BANK is 1, SWDBG data bit 3 if GPIO_BANK is 0
11 Reserved if GPIO_BANK is 1, TDMA event validate if GPIO_BANK is 0
GPIO5_M GPIO mode selection
00 Configured as GPIO function
01 Key-pad column 2, KCOL2 if GPIO_BANK is 1, host DSP ICE data if GPIO_BANK is 0
10 Reserved if GPIO_BANK is 1, SWDBG data bit 4 if GPIO_BANK is 0
11 Reserved if GPIO_BANK is 1, CTIRQ2 if GPIO_BANK is 0
GPIO6_M GPIO mode selection
00 Configured as GPIO function
01 Key-pad column 1, KCOL1 if GPIO_BANK is 1, host DSP ICE clock if GPIO_BANK is 0
10 Reserved if GPIO_BANK is 1, SWDBG data bit 5 if GPIO_BANK is 0
11 Reserved if GPIO_BANK is 1, CTIRQ1 if GPIO_BANK is 0
GPIO7_M GPIO mode selection
00 Configured as GPIO function
01 Key-pad column 0, KCOL0 if GPIO_BANK is 1, host DSP ICE mode-select if GPIO_BANK is 0
10 Reserved if GPIO_BANK is 1, SWDBG data bit 6 if GPIO_BANK is 0
11 Reserved if GPIO_BANK is 1, DTIRQ if GPIO_BANK is 0

0x8002_01A0 GPIO mode control register 2 GPIO_MODE2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15_M		GPIO14_M		GPIO13_M		GPIO12_M		GPIO11_M		GPIO10_M		GPIO9_M		GPIO8_M	
Type	R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	

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Reset	01	01	01	01	01	01	01	01

GPIO8_M GPIO mode selection
- **00** Configured as GPIO function
- **01** Key-pad row 5, KROW5
- **10** External interrupt 5, EINT5
- **11** Reserved

GPIO9_M GPIO mode selection
- **00** Configured as GPIO function
- **01** Key-pad row 4, KROW4
- **10** Reserved if GPIO_BANK is 1, SWDBG data bit 7 if GPIO_BANK is 0
- **11** SRCLKENA | SRECLKENAI

GPIO10_M GPIO mode selection
- **00** Configured as GPIO function
- **01** Key-pad row 3, KROW3
- **10** Reserved if GPIO_BANK is 1, SWDBG read strobe if GPIO_BANK is 0
- **11** Reserved if GPIO_BANK is 1, TDMA_BTXEN if GPIO_BANK is 0

GPIO11_M GPIO mode selection
- **00** Configured as GPIO function
- **01** Key-pad row 2, KROW2 if GPIO_BANK is 1, slave DSP ICE data if GPIO_BANK is 0
- **10** Reserved if GPIO_BANK is 1, SWDBG read OE if GPIO_BANK is 0
- **11** Reserved if GPIO_BANK is 1, TDMA_BTXFS if GPIO_BANK is 0

GPIO12_M GPIO mode selection
- **00** Configured as GPIO function
- **01** Key-pad row 1, KROW1 if GPIO_BANK is 1, slave DSP ICE clock if GPIO_BANK is 0
- **10** Reserved if GPIO_BANK is 1, SWDBG full flag if GPIO_BANK is 0
- **11** Reserved if GPIO_BANK is 1, TDMA_BRXEN if GPIO_BANK is 0

GPIO13_M GPIO mode selection
- **00** Configured as GPIO function
- **01** Key-pad row 0, KROW0 if GPIO_BANK is 1, slave DSP ICE mode-select if GPIO_BANK is 0
- **10** Reserved if GPIO_BANK is 1, SWDBG empty flag if GPIO_BANK is 0
- **11** Reserved if GPIO_BANK is 1, TDMA_BRXFS if GPIO_BANK is 0

GPIO14_M GPIO mode selection
- **00** Configured as GPIO function
- **01** external memory chip-select 2, ECS2_B
- **10** MFIQ
- **11** Reserved

GPIO15_M GPIO mode selection
- **00** Configured as GPIO function
- **01** DAI clock output

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10 CLK_OUT5 clock if GPIO_BANK is 1, SWDBG clock if GPIO_BANK is 0
11 Reserved if GPIO_BANK is 1, TDMA serial data output bit 0 if GPIO_BANK is 0

0x8002_01B0 GPIO mode control register 3 GPIO_MODE3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO23_M		GPIO22_M		GPIO21_M		GPIO20_M		GPIO19_M		GPIO18_M		GPIO17_M		GPIO16_M	
Type	R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
Reset	01		01		01		01		10		01		01		01	

GPIO16_M GPIO mode selection
00 Configured as GPIO function
01 DAI PCM output
10 Reserved if GPIO_BANK is 1, SWDBG ADDR[1] if GPIO_BANK is 0
11 Reserved if GPIO_BANK is 1, TDMA serial data output bit 1 if GPIO_BANK is 0

GPIO17_M GPIO mode selection
00 Configured as GPIO function
01 Reserved
10 DAI PCM input if GPIO_BANK is 1, SWDBG packet-end if GPIO_BANK is 0
11 IRDA power-down if GPIO_BANK is 1, TDMA serial frame sync.if GPIO_BANK is 0

GPIO18_M GPIO mode selection
00 Configured as GPIO function
01 DAI reset
10 CLK_OUT0 if GPIO_BANK is 1, SWDBG write strobe if GPIO_BANK is 0
11 IRDA TX if GPIO_BANK is 1, TDMA serial clock if GPIO_BANK is 0

GPIO19_M GPIO mode selection
00 Configured as GPIO function
01 DAI sync.
10 ADMUX indication if GPIO_BANK is 1, SWDBG ADDR[0] if GPIO_BANK is 0. The xadmux indicator only used when being boot-up. After system reset, xadmux is of no use, and software can configure the GPIO17_M to any other function
11 IRDA_RX if GPIO_BANK is 1, reserved if GPIO_BANK is 0

GPIO20_M GPIO mode selection
00 Configured as GPIO function
01 URXD3
10 UART2 flow control, UCTS2_B
11 Reserved

GPIO21_M GPIO mode selection
00 Configured as GPIO function
01 UTXD3
10 UART2 flow control, URTS2_B
11 Reserved

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GPIO22_M GPIO mode selection

- **00** Configured as GPIO function
- **01** URXD2
- **10** LCD_TE if GPIO_BANK is 1
- **11** IRDA_RX if GPIO_BANK is 1, slave DSP task ID 2 if GPIO_BANK is 0

GPIO23_M GPIO mode selection

- **00** Configured as GPIO function
- **01** UTXD2
- **10** EDI data
- **11** IRDA_TX if GPIO_BANK is 1, slave DSP task ID 3 if GPIO_BANK is 0

0x8002_01C0 GPIO mode control register 4 GPIO_MODE4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO31_M		GPIO30_M		GPIO29_M		GPIO28_M		GPIO27_M		GPIO26_M		GPIO25_M		GPIO24_M	
Type	R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
Reset	01		01		01		01		01		01		01		01	

GPIO24_M GPIO mode selection

- **00** Configured as GPIO function
- **01** UART1 flow control, UCTS1_B
- **10** I2C SCL

11 Reserved if GPIO_BANK is 1, slave DSP task ID 5 if GPIO_BANK is 0

GPIO25_M GPIO mode selection

- **00** Configured as GPIO function
- **01** UART1 flow control, URTS1_B
- **10** I2C SDA
- **11** Reserved if GPIO_BANK is 1, slave DSP task ID 4 if GPIO_BANK is 0

GPIO26_M GPIO mode selection

- **00** Configured as GPIO function
- **01** NFI chip enable bit 0, NCEB[0]
- **10** Reserved
- **11** Reserved

GPIO27_M GPIO mode selection

- **00** Configured as GPIO function
- **01** NFI read strobe, NREB
- **10** Reserved
- **11** Reserved

GPIO28_M GPIO mode selection

- **00** Configured as GPIO function
- **01** NFI write strobe, NWEB
- **10** Reserved

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11 Reserved
GPIO29_M GPIO mode selection
00 Configured as GPIO function
01 NFI address latch enable, NALE
10 Reserved
11 Reserved
GPIO30_M GPIO mode selection
00 Configured as GPIO function
01 NCLE
10 Reserved
11 Reserved
GPIO31_M GPIO mode selection
00 Configured as GPIO function
01 NFI busy flag, NRNB
10 Reserved
11 Reserved

0x8002_01D0 GPIO mode control register 5 GPIO_MODE5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO39_M		GPIO38_M		GPIO37_M		GPIO36_M		GPIO35_M		GPIO34_M		GPIO33_M		GPIO32_M	
Type	R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
Reset	01		01		01		01		01		01		01		01	

GPIO32_M GPIO mode selection
00 Configured as GPIO function
01 NLD data bit 0. Also act as CMDAT[0] when in MT6252
10 Reserved
11 Reserved
GPIO33_M GPIO mode selection
00 Configured as GPIO function
01 NLD data bit 1. Also act as CMDAT[1] when in MT6252
10 Reserved
11 Reserved
GPIO34_M GPIO mode selection
00 Configured as GPIO function
01 NLD data bit 2. Also act as CMDAT[2] when in MT6252
10 Reserved
11 Reserved
GPIO35_M GPIO mode selection
00 Configured as GPIO function
01 NLD data bit 3. Also act as CMDAT[3] when in MT6252

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10 Reserved
11 Reserved

GPIO36_M GPIO mode selection
00 Configured as GPIO function
01 NLD data bit 4. Also act as CMDAT[4] when in MT6252
10 Reserved
11 Reserved

GPIO37_M GPIO mode selection
00 Configured as GPIO function
01 NLD data bit 5. Also act as CMDAT[5] when in MT6252
10 Reserved
11 Reserved

GPIO38_M GPIO mode selection
00 Configured as GPIO function
01 NLD data bit 6. Also act as CMDAT[6] when in MT6252
10 Reserved
11 Reserved

GPIO39_M GPIO mode selection
00 Configured as GPIO function
01 NLD data bit 7. Also act as CMDAT[7] when in MT6252
10 Reserved
11 Reserved

0x8002_01E0 GPIO mode control register 6 GPIO_MODE6

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47_M		GPIO46_M		GPIO45_M		GPIO44_M		GPIO43_M		GPIO42_M		GPIO41_M		GPIO40_M	
Type	R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
Reset	00		01		01		01		01		01		01		01	

GPIO40_M GPIO mode selection
00 Configured as GPIO function
01 NLD data bit 8
10 EDI clock
11 RF AUXOUT for debug usage

GPIO41_M GPIO mode selection
00 Configured as GPIO function
01 LCD write strobe, LWRB
10 Act as MCINS in MT6252
11 Reserved

GPIO42_M GPIO mode selection
00 Configured as GPIO function

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01 LPA0
10 Act as MCWP in MT6252
11 BSI clock output for debug usage

GPIO43_M GPIO mode selection
00 Configured as GPIO function
01 LCD read strobe, LRDB
10 Act as MCCM0 in MT6252
11 Reserved

GPIO44_M GPIO mode selection
00 Configured as GPIO function
01 LCD reset, LRSTB
10 Reserved
11 BSI chip-select output for debug usage

GPIO45_M GPIO mode selection
00 Configured as GPIO function
01 LCD chip select 0, LPCE0B
10 Reserved
11 BSI data output from baseband to RF for debug usage

GPIO46_M GPIO mode selection
00 Configured as GPIO function
01 LCD chip select 1, LPCE1B
10 Reserved
11 BSI data input from RF to baseband for debug usage

GPIO47_M GPIO mode selection
00 Configured as GPIO function
01 Camera data bit 0, CMDAT0
10 Reserved
11 Reserved

0x8002_01F0 GPIO mode control register 7 GPIO_MODE7

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO55		GPIO54		GPIO53		GPIO52		GPIO51		GPIO50		GPIO49		GPIO48	
Type	R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
Reset	00		00		00		00		0		00		00		00	

GPIO48_M GPIO mode selection
00 Configured as GPIO function
01 Camera data bit 1, CMDAT1
10 Reserved
11 Reserved

GPIO49_M GPIO mode selection

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00 Configured as GPIO function
01 Camera data bit 2, CMDAT2
10 Reserved
11 Reserved

GPIO50_M GPIO mode selection
00 Configured as GPIO function
01 Camera data bit 3, CMDAT3
10 Reserved
11 Reserved

GPIO51_M GPIO mode selection
00 Configured as GPIO function
01 Camera data bit 4, CMDAT4
10 Reserved
11 Reserved

GPIO52_M GPIO mode selection
00 Configured as GPI function
01 Camera data bit 5, CMDAT5
10 Reserved
11 Reserved

GPIO53_M GPIO mode selection
00 Configured as GPI function
01 Camera data bit 6, CMDAT6
10 Reserved
11 Reserved

GPIO54_M GPIO mode selection
00 Configured as GPI function
01 Camera data bit 7, CMDAT7
10 Reserved
11 Reserved

GPIO55_M GPIO mode selection
00 Configured as GPI function
01 CMHREF
10 Reserved
11 Reserved

0x8002_0200 GPIO mode control register 8 GPIO_MODE8

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO63		GPIO62		GPIO61		GPIO60		GPIO59		GPIO58		GPIO57		GPIO56	
Type	R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
Reset	01		01		01		00		00		00		00		00	

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GPIO56_M GPIO mode selection
- **00** Configured as GPIO function
- **01** CMVREF
- **10** Reserved
- **11** Reserved

GPIO57_M GPIO mode selection
- **00** Configured as GPIO function
- **01** CMPDN
- **10** Reserved
- **11** Reserved

GPIO58_M GPIO mode selection
- **00** Configured as GPIO function
- **01** CMMCLK
- **10** Host DSP task ID 0 if GPIO_BANK is 0 if GPIO_BANK is 0
- **11** Reserved

GPIO59_M GPIO mode selection
- **00** Configured as GPIO function
- **01** CMPCLK
- **10** Reserved
- **11** Reserved

GPIO60_M GPIO mode selection
- **00** Configured as GPI function
- **01** CMRST
- **10** Reserved
- **11** Reserved

GPIO61_M GPIO mode selection
- **00** Configured as GPI function
- **01** EINT3
- **10** CLK_OUT4 if GPIO_BANK is 1, SWDBG data bit 0 if GPIO_BANK is 0
- **11** CMVREF when in MT6252

GPIO62_M GPIO mode selection
- **00** Configured as GPI function
- **01** EINT2
- **10** MIRQ
- **11** CLK_OUT3 if GPIO_BANK is 1, host DSP task ID 1if GPIO_BANK is 0

GPIO63_M GPIO mode selection
- **00** Configured as GPI function
- **01** EINT1
- **10** Reserved
- **11** CMHREF when in MT6252 if GPIO_BANK is 1, slave DSP task ID 0 if GPIO_BANK is 0

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0x8002_0210 GPIO mode control register 9 GPIO_MODE9

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO71		GPIO70		GPIO69		GPIO68		GPIO67		GPIO66		GPIO65		GPIO64	
Type	R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
Reset	01		01		01		01		01		01		01		01	

GPIO64_M GPIO mode selection

- **00** Configured as GPIO function
- **01** EINT0
- **10** Reserved
- **11** CMPCLK when in MT6252 if GPIO_BANK is 1, slave DSP task ID 1 if GPIO_BANK is 0

GPIO65_M GPIO mode selection

- **00** Configured as GPIO function
- **01** MCINS
- **10** Reserved
- **11** Reserved

GPIO66_M GPIO mode selection

- **00** Configured as GPIO function
- **01** MCWP
- **10** Reserved
- **11** Reserved

GPIO67_M GPIO mode selection

- **00** Configured as GPIO function
- **01** MCCK
- **10** Reserved
- **11** Reserved

GPIO68_M GPIO mode selection

- **00** Configured as GPI function
- **01** MCDA3
- **10** Reserved
- **11** Reserved

GPIO69_M GPIO mode selection

- **00** Configured as GPI function
- **01** MCDA2
- **10** Reserved
- **11** Reserved

GPIO70_M GPIO mode selection

- **00** Configured as GPI function
- **01** MCDA1
- **10** Reserved

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11 Reserved

GPIO71_M GPIO mode selection

00 Configured as GPI function

01 MCDA0

10 Reserved

11 Reserved

0x8002_0220 GPIO mode control register 10 GPIO_MODE10

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO79		GPIO78		GPIO77		GPIO76		GPIO75		GPIO74		GPIO73		GPIO72	
Type	R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
Reset	00		00		01		00		00		00		00		00	

GPIO72_M GPIO mode selection

00 Configured as GPIO function

01 Reserved

10 Reserved

11 Reserved

GPIO73_M GPIO mode selection

00 Configured as GPIO function

01 Reserved

10 Reserved

11 Reserved

GPIO74_M GPIO mode selection

00 Configured as GPIO function

01 CLK_OUT6

10 Reserved

11 SRCLKENA | SRCLKENAI

GPIO75_M GPIO mode selection

00 Configured as GPIO function

01 Reserved

10 Reserved

11 CLK_OUT2

GPIO76_M GPIO mode selection

00 Configured as GPIO function

01 IRDA power-down, IRDA_PDN

10 EINT6

11 EDI word-select

GPIO77_M GPIO mode selection

00 Configured as GPIO function

01 SRCLKENAI

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10 Reserved
11 Reserved
GPIO78_M GPIO mode selection
00 Configured as GPIO function
01 SIM2 clock
10 Reserved
11 Reserved
GPIO79_M GPIO mode selection
00 Configured as GPIO function
01 SIM2 reset
10 Reserved
11 Reserved

0x8002_03D0 GPIO mode control register 11 GPIO_MODE11

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GPIO82		GPIO81		GPIO80	
Type											R/W		R/W		R/W	
Reset											1		1		0	

GPIO80_M GPIO mode selection
00 Configured as GPIO function
01 SIM2 data
10 Reserved
11 Reserved
GPIO81_M GPIO mode selection
00 Configured as GPIO function
01 BPI_BUS4
10 MCCK in MT6252
11 Reserved
GPIO82_M GPIO mode selection
00 Configured as GPIO function
01 BPI_BUS5
10 MCDAT in MT6252
11 Reserved

0x8002_0240 GPIO Pull Up/Down Select 1 GPIO_PULLSEL1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

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0x8002_0250 GPIO Pull Up/Down Select 2 — GPIO_PULLSEL2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	PGIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	1	1	1	1	1	1	0	1	1	0

0x8002_0260 GPIO Pull Up/Down Select 3 — GPIO_PULLSEL3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8002_0270 GPIO Pull Up/Down Select 4 — GPIO_PULLSEL4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO63	GPIO62	GPIO61	GPIO60	GPIO59	GPIO58	GPIO57	GPIO56	GPIO55	GPIO54	GPIO53	GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8002_0280 GPIO Pull Up/Down Select 5 — GPIO_PULLSEL5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO79	GPIO78	GPIO77	GPIO76	GPIO75	GPIO74	GPIO73	GPIO72	GPIO71	GPIO70	GPIO69	GPIO68	GPIO67	GPIO66	GPIO65	GPIO64
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

0x8002_03E0 GPIO Pull Up/Down Select 6 — GPIO_PULLSEL6

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														GPIO82	GPIO81	GPIO80
Type														R/W	R/W	R/W
Reset														0	0	0

GPIO*n* GPIO pull up/down selection, only valid if corresponding GPIO_PULLEN is high

- **0** GPIOs pull down is selected
- **1** GPIOs pull up is selected

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GPIO +0370h OE read-back selection GPIO_TM

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TM_DIR
Type																R/W
Reset																0

TM_DIR Select to read GPIO_DIRx as the real pad output-enable or the MCU-configured GPIO_DIR

- **0** MCU-configured
- **1** Real pad OE

GPIO+xxx4h GPIO xxx register SET GPIO_XXX_SET

For all registers addresses listed above, writing to the +4h addresse offset will perform a bit-wise **OR** function between the 16bit written value and the 16bit register value already existing in the corresponding GPIO_xxx registers.

Eg.

If GPIO_DIR1 (GPIO+0000h) = 16'h0F0F,

writing GPIO_DIR1_SET (GPIO+0004h) = 16'F0F0 will result in GPIO_DIR1 = 16'hFFFF.

GPIO+xxx8h GPIO xxx register CLR GPIO_XXX_CLR

For all registers addresses listed above, writing to the +8h addresse offset will perform a bit-wise **AND-NOT** function between the 16bit written value and the 16bit register value already existing in the corresponding GPIO_xxx registers.

Eg.

If GPIO_DIR1 (GPIO+0000h) = 16'h0F0F,

writing GPIO_DIR1_CLR (GPIO+0008h) = 16'0F0F will result in GPIO_DIR1 = 16'h0000.

CONFG +0700h Misc usage ACIF_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPIBUS SR	LCD SR	LCD E4	LCD E8	CMPCLK SMT	CMMCLK SR	CMMCLK E4	CMMCLK E8	FM_32K SR	FM_32K E4	BT_POWEN SR	BT_POWEN E4	BT_32K SR	BT_32K E4	ALERTER SR	ALERTER E4
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0

ALERTER E4

- **0** 2 mA
- **1** 6 mA.

ALERTER SR

- **0** Slow slew rate?
- **1** Fast slew rate?

BT_32K E4

- **0** 2 mA
- **1** 6 mA.

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BT_32K SR

- **0** Fast slew rate
- **1** Slow slew rate

BT_POWEN E4

- **0** 2 mA
- **1** 6 mA.

BT_ POWEN SR

- **0** Fast slew rate
- **1** Slow slew rate

FM_32K E4

- **0** 2 mA
- **1** 6 mA.

FM_32K SR

- **0** Fast slew rate
- **1** Slow slew rate

CMMCLK E4

- **0** + 0 mA
- **1** + 4 mA. CMMCLK default is 4 mA.

CMMCLK E8

- **0** + 0 mA
- **1** + 8 mA. CMMCLK default is 4 mA.

CMMCLK SR

- **0** Fast slew rate
- **1** Slow slew rate

CMPCLK SMT

- **0** Disable SMT
- **1** Enable SMT

LCD E4

- **0** + 0 mA
- **1** + 4 mA. LCD related control pins default is 4 mA.

LCD E8

- **0** + 0 mA
- **1** + 8 mA. LCD related control pins default is 4 mA.

LCD SR

- **0** Fast slew rate
- **1** Slow slew rate

BPIBUS SR Note that BPIBUS driving current settings are located at BPI module

- **0** Fast slew rate
- **1** Slow slew rate

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CONFG +0704h **Misc usage** **ACIF_CON1**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		KP_COL SR	KP_COL E2	KP_COL E4		CM SR	CM E4	CM E8		UART SR	UART E4	UART E8	IRDA_PDN SR	NFI SR	NFI E4	NFI E8
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	1	0	0	0	0	0	0	1	1	0	0

NFI E4 NAND flash data and control driving current setting

- **0** + 0 mA
- **1** + 4 mA. NFI related control and data pins default is 4 mA.

NFI E8 NAND flash data and control driving current setting

- **0** + 0 mA
- **1** + 8 mA. NFI related control and data pins default is 4 mA.

NFI SR

- **0** Fast slew rate
- **1** Slow slew rate

IRDA_PSN SR

- **0** Fast slew rate
- **1** Slow slew rate

UART E4 UART data and control driving current setting

- **0** + 0 mA
- **1** + 4 mA. UART related control and data pins default is 4 mA.

UART E8 UART data and control driving current setting

- **0** + 0 mA
- **1** + 8 mA. UART related control and data pins default is 4 mA.

UART SR

- **0** Fast slew rate
- **1** Slow slew rate

CM E4 Camera output signal driving current setting

- **0** + 0 mA
- **1** + 4 mA. Camera related control and data pins default is 4 mA.

CM E8 Camera output signal driving current setting

- **0** + 0 mA
- **1** + 8 mA. Camera related control and data pins default is 4 mA.

CM SR

- **0** Fast slew rate
- **1** Slow slew rate

KP_COL E2 Key pad column driving current setting

- **0** + 0 mA

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1 + 2 mA. Default is 2 mA.

KP_COL E4

0 + 0 mA

1 + 4 mA. Default is 2 mA.

KP_COL SR

0 Fast slew rate

1 Slow slew rate

CONFG +0708h Misc usage ACIF_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			PWM SR	PWM E8		WATCHDOG SR	WATCHDOG E2	WATCHDOG E4	SRCLKENAI SR	SRCLKENAI E4	SD_PWREN SR	SD_PWREN E4	KP_ROW SR	KP_ROW E4	CLK_RDSEL	CMD_RDSEL
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

CMD_RDSEL MDDR IO_CUP RDSEL option for CMD_MACRO

0 Default mode

1 Experiment mode

CLK_RDSEL MDDR IO_CUP RDSEL option for CLK_MACRO

0 Default mode

1 Experiment mode

KP_ROW E4 Key pad row driving current setting

0 + 0 mA

1 + 4 mA. Default is 2 mA.

KP_ROW SR

0 Fast slew rate

1 Slow slew rate

SD_PWREN E4 MSDC power enable driving current setting

0 + 0 mA

1 + 4 mA. Default is 2 mA.

SD_PWREN SR

0 Fast slew rate

1 Slow slew rate

SRCLKENAI E4 Driving current setting

0 + 0 mA

1 + 4 mA. Default is 4 mA.

SRCLKENAI SR

0 Fast slew rate

1 Slow slew rate

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WATCHDOG E2 Driving current setting
- **0** + 0 mA
- **1** + 2 mA. Default is 2 mA.

WATCHDOG E4 Driving current setting
- **0** + 0 mA
- **1** + 4 mA. Default is 2 mA.

WATCHDOG SR
- **0** Fast slew rate
- **1** Slow slew rate

PWM E8 Driving current setting
- **0** + 0 mA
- **1** + 8 mA. Default is 4 mA.

PWM SR
- **0** Fast slew rate
- **1** Slow slew rate

CONFG +070Ch Misc usage ACIF_CON3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		MCD PUPD	MCC PUPD	MCCK PUPD			LCD_MSDCCK_SEL	BSI_EXT_SEL	JTDO SR	JTDO E2	JRTCK SR	JRTCK E2		DAI SR	DAI E2	DAI E4
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	0

DAI E2 Driving current setting
- **0** + 0 mA
- **1** + 2 mA. Default is 2 mA.

DAI E4 Driving current setting
- **0** + 0 mA
- **1** + 4 mA. Default is 2 mA.

DAI SR
- **0** Fast slew rate
- **1** Slow slew rate

JRTCK E2 Driving current setting
- **0** + 0 mA
- **1** + 2 mA. Default is 2 mA.

JRTCK SR
- **0** Fast slew rate
- **1** Slow slew rate

JTDO E2 Driving current setting

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0 + 0 mA
1 + 2 mA. Default is 2 mA.

JTDO SR
0 Fast slew rate
1 Slow slew rate

BSI_EXT_SEL BSI selection
0 Internal BSI
1 External BSI

LCD_MSDC_CK_SEL MCCK pad output clock selection
0 msdc_clk output
1 lcd_mc_clk output

MCCK_PUPD MCCK pad PUPD port connection
0 Pullup
1 Pulldown

MCC_PUPD MSDC command pads PUPD port connection
0 Pullup
1 Pulldown

MCD_PUPD MSDC data pads PUPD port connection
0 Pullup
1 Pulldown

The pull-up pull-down resistance value is determinated by the following tables

PUPD	R0	R1	result
0	0	0	high-Z
0	0	1	pull-up with 47K
0	1	0	pull-up with 47K
0	1	1	pull-up with 23.5K
1	0	0	high-Z
1	0	1	pull-down with 47K
1	1	0	pull-down with 47K
1	1	1	pull-down with 23.5K

Table 24 MSDC Input Ports Definition

PAD	PUPD	Aux. Func. 0	Aux. Func. 1
MCDA0 (GPIO71)	PU 47K	1. 0x8001070c[14] = 0 2. 0x80020090[7] = 1	1. 0x8001070c[14] = 0 2. 0x81110000[27:26]=0x1 or 0x2

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	PU 23.5K	NA	1. 0x8001070c[14] = 0 2. 0x81110000[27:26]=0x3
	High-Z	1. 0x80020090[7] = 0	1. 0x81110000[27:26]=0x0
	PD 47K	1. 0x8001070c[14] = 1 2. 0x80020090[7] = 1	1. 0x8001070c[14] = 1 2. 0x81110000[27:26]=0x1 or 0x2
	PD 23.5K	NA	1. 0x8001070c[14] = 1 2. 0x81110000[27:26]=0x3
MCDA1 (GPIO70)	PU 47K	1. 0x8001070c[14] = 0 2. 0x80020090[6] = 1	1. 0x8001070c[14] = 0 2. 0x81110000[27:26]=0x1 or 0x2
	PU 23.5K	NA	1. 0x8001070c[14] = 0 2. 0x81110000[27:26]=0x3
	High-Z	1. 0x80020090[6] = 0	1. 0x81110000[27:26]=0x0
	PD 47K	1. 0x8001070c[14] = 1 2. 0x80020090[6] = 1	1. 0x8001070c[14] = 1 2. 0x81110000[27:26]=0x1 or 0x2
	PD 23.5K	NA	1. 0x8001070c[14] = 1 2. 0x81110000[27:26]=0x3
MCDA2 (GPIO69)	PU 47K	1. 0x8001070c[14] = 0 2. 0x80020090[5] = 1	53T: NA
			53: 1. 0x8001070c[14] = 0 2. 0x81110000[27:26]=0x1 or 0x2
	PU 23.5K	NA	53T: 1. 0x8001070c[14] = 0 2. 0x81110000[27]=0x1
			53: 1. 0x8001070c[14] = 0 2. 0x81110000[27:26]=0x3
	High-Z	1. 0x80020090[5] = 0	1. 0x81110000[27:26]=0x0
	PD 47K	1. 0x8001070c[14] = 1	53T: NA

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		2. 0x80020090[5] = 1	53: 1. 0x8001070c[14] = 1 2. 0x81110000[27:26]=0x1 or 0x2
	PD 23.5K	NA	53T: 1. 0x8001070c[14] = 1 2. 0x81110000[27]=0x1
			53: 1. 0x8001070c[14] = 1 2. 0x81110000[27:26]=0x3
MCDA3 (GPIO68)	PU 47K	1. 0x8001070c[14] = 0 2. 0x80020090[4] = 1	1. 0x8001070c[14] = 0 2. 0x81110000[27:26]=0x1 or 0x2
	PU 23.5K	NA	1. 0x8001070c[14] = 0 2. 0x81110000[27:26]=0x3
	High-Z	1. 0x80020090[4] = 0	1. 0x81110000[27:26]=0x0
	PD 47K	1. 0x8001070c[14] = 1 2. 0x80020090[4] = 1	1. 0x8001070c[14] = 1 2. 0x81110000[27:26]=0x1 or 0x2
	PD 23.5K	NA	1. 0x8001070c[14] = 1 2. 0x81110000[27:26]=0x3
MCCK (GPIO67)	PU 47K	1. 0x8001070c[12] = 0 2. 0x80020090[3] = 1	1. 0x8001070c[12] = 0 2. 0x80020090[3] = 1
	PU 23.5K	NA	NA
	High-Z	1. 0x80020090[3] = 0	1. 0x80020090[3] = 0
	PD 47K	1. 0x8001070c[12] = 1 2. 0x80020090[3] = 1	1. 0x8001070c[12] = 1 2. 0x80020090[3] = 1
	PD 23.5K	NA	NA
MCCM0 delicated	PU 47K	NA	1. 0x8001070c[13] = 0 2. 0x81110000[25:24]=0x1 or 0x2
	PU 23.5K	NA	1. 0x8001070c[13] = 0 2. 0x81110000[25:24]=0x3

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	High-Z	NA	1. 0x81110000[25:24]=0x0
	PD 47K	NA	1. 0x8001070c[13] = 1 2. 0x81110000[25:24]=0x1 or 0x2
	PD 23.5K	NA	1. 0x8001070c[13] = 1 2. 0x81110000[25:24]=0x3
MCINS (GPIO65)	PU	1. 0x80020090[1] = 1 2. 0x80020280[1] = 1	1. 0x81110014[9:8]=0x2
	High-Z	1. 0x80020090[1] = 0	1. 0x81110014[9:8]=0x0
	PD	1. 0x80020090[1] = 1 2. 0x80020280[1] = 0	1. 0x81110014[9:8]=0x1
MCWP (GPIO66)	PU	1. 0x80020090[2] = 1 2. 0x80020280[2] = 1	1. 0x81110000[23:22]=0x2
	High-Z	1. 0x80020090[2] = 0	1. 0x81110000[23:22]=0x0
	PD	1. 0x80020090[2] = 1 2. 0x80020280[2] = 0	1. 0x81110000[23:22]=0x1

Table 25 MT6253T and MT6253MP MSDC PADs Configurations

4.6 General Purpose Timer

4.6.1 General Description

Three general-purpose timers are provided. The timers are 16 bits long and run independently of each other, although they share the same clock source. Two timers can operate in one of two modes: one-shot mode and auto-repeat mode; the other is a free running timer. In one-shot mode, when the timer counts down and reaches zero, it is halted. In auto-repeat mode, when the timer reaches zero, it simply resets to countdown initial value and repeats the countdown to zero; this loop repeats until the disable signal is set to 1. Regardless of the timer's mode, if the countdown initial value (i.e. GPTIMER1_DAT for GPT1 or GPTIMER_DAT2 for GPT2) is written when the timer is running, the new initial value does not take effect until the next time the timer is restarted. In auto-repeat mode, the new countdown start value is used on the next countdown iteration. Therefore, before enabling the gptimer, the desired values for GPTIMER_DAT and the GPTIMER_PRESCALER registers must first be set.

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4.6.2 Register Definitions

REGISTER ADDRESS	REGISTER NAME	SYNONYM
0x8106_0000	GPT1 Control register	gptIMER1_CON
0x8106_0004	GPT1 Time-Out Interval register	GPTIMER1_DAT
0x8106_0008	GPT2 Control register	GPTIMER2_CON
0x8106_000C	GPT2 Time-Out Interval register	GPTIMER2_DAT
0x8106_0010	GPT Status register	GPTIMER_STA
0x8106_0014	GPT1 Prescaler register	GPTIMER1_PRESCALER
0x8106_0018	GPT2 Prescaler register	GPTIMER2_PRESCALER
0x8106_001C	GPT3 Control register	GPTIMER3_con
0x8106_0020	GPT3 Time-Out Interval register	GPTIMER3_DAT
0x8106_0024	GPT3 Prescaler register	GPTIMER3_PRESCALER

Table 26 General Purpose Timer Register Map

0x8106_0000 GPT1 Control register GPTIMER1_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN	MODE														
Type	R/W	R/W														
Reset	0	0														

MODE This register controls GPT1 to count repeatedly (in a loop) or just one-shot.

0 One-shot mode is selected.

1 Auto-repeat mode is selected.

EN This register controls GPT1 to start counting or to stop.

0 GPT1 is disabled.

1 GPT1 is enabled.

0x8106_0004 GPT1 Time-Out Interval register GPTIMER1_DAT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNT [15:0]															
Type	R/W															
Reset	FFFFh															

CNT [15:0] Initial counting value. GPT1 counts down from GPTIMER1_DAT. When GPT1 counts down to zero, a GPT1 interrupt is generated.

0x8106_0008 GPT2 Control register GPTIMER2_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN	MODE														
Type	R/W	R/W														
Reset	0	0														

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MODE This register controls GPT2 to count repeatedly (in a loop) or just one-shot.

- **0** One-shot mode is selected
- **1** Auto-repeat mode is selected

EN This register controls GPT2 to start counting or to stop.

- **0** GPT2 is disabled.
- **1** GPT2 is enabled.

0x8106_000C GPT2 Time-Out Interval register GPTIMER2_DAT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNT [15:0]															
Type	R/W															
Reset	FFFFh															

CNT [15:0] Initial counting value. GPT2 counts down from GPTIMER2_DAT. When GPT2 counts down to zero, a GPT2 interrupt is generated.

0x8106_0010 GPT Status register GPTIMER_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															GPT2	GPT1
Type															RC	RC
Reset															0	0

This register illustrates the gptimer timeout status. Each flag is set when the corresponding timer countdown completes, and can be cleared when the CPU reads the status register.

0x8106_0014 GPT1 Prescaler register GPTIMER1_PRESCALER

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PRESCALER [2:0]		
Type														R/W		
Reset														100b		

PRESCALER This register controls the counting clock for gptimer1.

- **000** 16384 Hz
- **001** 8192 Hz
- **010** 4096 Hz
- **011** 2048 Hz
- **100** 1024 Hz
- **101** 512 Hz
- **110** 256 Hz
- **111** 128 Hz

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0x8106_0018 GPT2 Prescaler register — GPTIMER2_PRESCALER

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PRESCALER [2:0]		
Type														R/W		
Reset														100b		

PRESCALER This register controls the counting clock for gptimer2.

- **000** 16384 Hz
- **001** 8192 Hz
- **010** 4096 Hz
- **011** 2048 Hz
- **100** 1024 Hz
- **101** 512 Hz
- **110** 256 Hz
- **111** 128 Hz

0x8106_001C GPT3 Control register — GPTIMER3_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																R/W
Reset																0

EN This register controls GPT3 to start counting or to stop.

- **0** GPT3 is disabled.
- **1** GPT3 is enabled.

0x8106_0020 GPT3 Time-Out Interval register — GPTIMER3_DAT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNT[15:0]															
Type	RO															
Reset	0															

CNT [15:0] If EN=1, GPT3 is a free running timer . Software reads this register for the countdown start value for GPT3.

0x8106_0024 GPT3 Prescaler register — GPTIMER3_PRESCALER

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PRESCALER [2:0]		
Type														R/W		
Reset														100b		

PRESCALER This register controls the counting clock for gptimer3.

- **000** 16384 Hz

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001 8192 Hz
010 4096 Hz
011 2048 Hz
100 1024 Hz
101 512 Hz
110 256 Hz
111 128 Hz

4.7 UART

4.7.1 General Description

The baseband chipset houses three UARTs. The UARTs provide full duplex serial communication channels between baseband chipset and external devices.

The UART has M16C450 and M16550A modes of operation, which are compatible with a range of standard software drivers. The extensions have been designed to be broadly software compatible with 16550A variants, but certain areas offer no consensus.

In common with the M16550A, the UART supports word lengths **from five to eight bits**, **an optional parity bit** and one or two stop bits, and is fully programmable by an 8-bit CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided. The UART also includes two DMA handshake lines, used to indicate when the FIFOs are ready to transfer data to the CPU. Interrupts can be generated from any of the 10 sources.

Note: The UART has been designed so that all internal operations are synchronized by the CLK signal. This synchronization results in minor timing differences between the UART and the industry standard 16550A device, which means that the core is not clock for clock identical to the original device.

After a hardware reset, the UART is in M16C450 mode. Its FIFOs can be enabled and the UART can then enter M16550A mode. The UART adds further functionality beyond M16550A mode. Each of the extended functions can be selected individually under software control.

The UART provides more powerful enhancements than the industry-standard 16550:

- Hardware flow control. This feature is very useful when the ISR latency is hard to predict and control in the embedded applications. The MCU is relieved of having to fetch the received data within a fixed amount of time.
- Output of an IR-compatible electrical pulse with a width 3/16 of that of a regular bit period.

Note: In order to enable any of the enhancements, the Enhanced Mode bit, EFR[4], must be set. If EFR[4] is not set, IER[7:5], FCR[5:4], IIR[5:4] and MCR[7:6] cannot be written. The Enhanced Mode bit ensures that the UART is backward compatible with software that has been written for 16C450 and 16550A devices.

Figure 40 shows the block diagram of the UART device.

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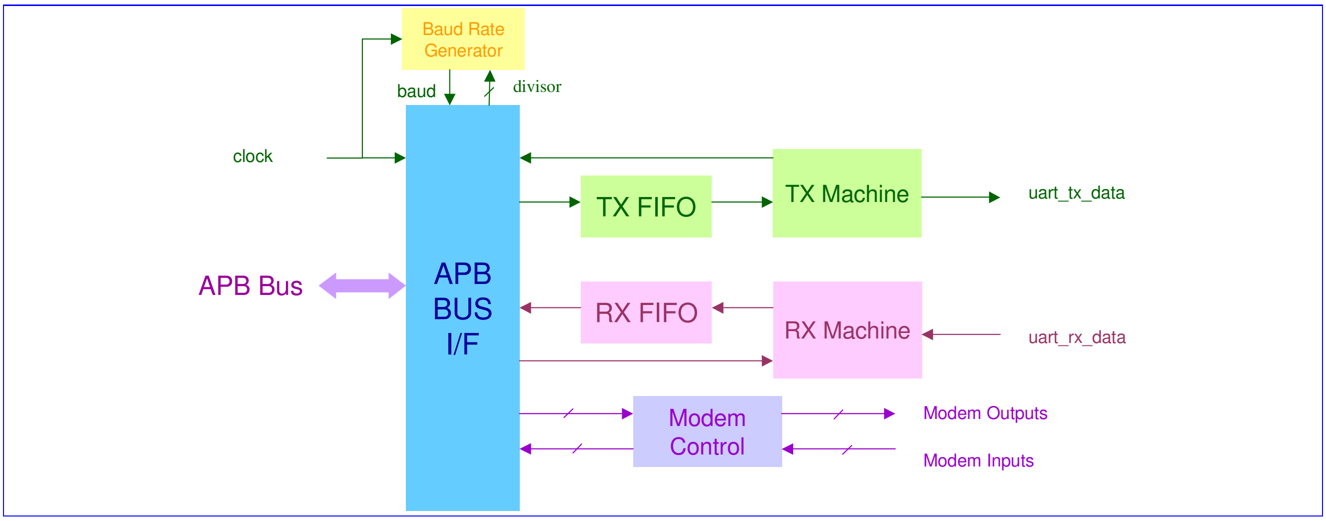

Figure 40 Block Diagram of UART

4.7.2 Register Definitions

UART1 Register Mapping Table:

MCU Register Addr.	Register Function	Acronym
81030000h	RX Buffer Register	UARTn_RBR
81030000h	TX Holding Register	UARTn_THR
81030004h	Interrupt Enable Register	UARTn_IER
81030008h	Interrupt Identification Register	UARTn_IIR
81030008h	FIFO Control Register	UARTn_FCR
8103000Ch	Line Control Register	UARTn_LCR
81030010h	Modem Control Register	UARTn_MCR
81030014h	Line Status Register	UARTn_LSR
81030018h	Modem Status Register	UARTn_MSR
8103001Ch	Scratch Register	UARTn_SCR
81030000h	Divisor Latch (LS)	uartn_dll
81030004h	Divisor Latch (MS)	uartn_dlM

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81030008h	Enhanced Feature Register	UARTn_EFR
81030010h	XON1	UARTn_XON1
81030014h	XON2	UARTn_XON2
81030018h	XOFF1	UARTn_XOFF1
8103001Ch	XOFF2	UARTn_XOFF2
81030020h	AUTOBAUD_EN	UARTn_AUTOBAUD_EN
81030024h	HIGH SPEED UART	UARTn_HIGHSPEED
81030028h	SAMPLE_COUNT	UARTn_SAMPLE_COUNT
8103002Ch	SAMPLE_POINT	UARTn_SAMPLE_POINT
81030030h	AUTOBAUD_REG	UARTn_AUTOBAUD_REG
81030034h	Rate Fix Address	UARTn_RateFix_ad
81030038h	AUTOBAUDSAMPLE	UARTn_AUTOBAUDSAMPLE
8103003Ch	Guard time added register	UARTn_GUARD
81030040h	Escape character register	UARTn_ESCAPE_DAT
81030044h	Escape enable register	UARTn_ESCAPE_EN
81030048h	Sleep enable register	UARTn_SLEEP_EN
8103004Ch	Virtual FIFO enable register	UARTn_VFIFO_EN
81030050h	Rx Trigger Address	UARTn_RXTRI_AD
81030054h	Fractional Divider LSB Address	UARTn_Fracdiv_l
81030058h	Fractional Divider MSB Address	UARTn_FRACDIV_M

UART2 Register Mapping Table:

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MCU Register Addr.	Register Function	Acronym
81040000h	RX Buffer Register	UARTn_RBR
81040000h	TX Holding Register	UARTn_THR
81040004h	Interrupt Enable Register	UARTn_IER
81040008h	Interrupt Identification Register	UARTn_IIR
81040008h	FIFO Control Register	UARTn_FCR
8104000Ch	Line Control Register	UARTn_LCR
81040010h	Modem Control Register	UARTn_MCR
81040014h	Line Status Register	UARTn_LSR
81040018h	Modem Status Register	UARTn_MSR
8104001Ch	Scratch Register	UARTn_SCR
81040000h	Divisor Latch (LS)	uartn_dll
81040004h	Divisor Latch (MS)	uartn_dlM
81040008h	Enhanced Feature Register	UARTn_EFR
81040010h	XON1	UARTn_XON1
81040014h	XON2	UARTn_XON2
81040018h	XOFF1	UARTn_XOFF1
8104001Ch	XOFF2	UARTn_XOFF2
81040020h	AUTOBAUD_EN	UARTn_AUTOBAUD_EN
81040024h	HIGH SPEED UART	UARTn_HIGHSPEED
81040028h	SAMPLE_COUNT	UARTn_SAMPLE_COUNT
8104002Ch	SAMPLE_POINT	UARTn_SAMPLE_POINT
81040030h	AUTOBAUD_REG	UARTn_AUTOBAUD_REG
81040034h	Rate Fix Address	UARTn_RateFix_ad

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81040038h	AUTOBAUDSAMPLE	UARTn_AUTOBAUDSAMPLE
8104003Ch	Guard time added register	UARTn_GUARD
81040040h	Escape character register	UARTn_ESCAPE_DAT
81040044h	Escape enable register	UARTn_ESCAPE_EN
81040048h	Sleep enable register	UARTn_SLEEP_EN
8104004Ch	Virtual FIFO enable register	UARTn_VFIFO_EN
81040050h	Rx Trigger Address	UARTn_RXTRI_AD
81040054h	Fractional Divider LSB Address	UARTn_Fracdiv_l
81040058h	Fractional Divider MSB Address	UARTn_FRACDIV_M

UART3 Register Mapping Table:

MCU Register Addr.	Register Function	Acronym
81050000h	RX Buffer Register	UARTn_RBR
81050000h	TX Holding Register	UARTn_THR
81050004h	Interrupt Enable Register	UARTn_IER
81050008h	Interrupt Identification Register	UARTn_IIR
81050008h	FIFO Control Register	UARTn_FCR
8105000Ch	Line Control Register	UARTn_LCR
81050010h	Modem Control Register	UARTn_MCR
81050014h	Line Status Register	UARTn_LSR
81050018h	Modem Status Register	UARTn_MSR
8105001Ch	Scratch Register	UARTn_SCR

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81050000h	Divisor Latch (LS)	uartn_dll
81050004h	Divisor Latch (MS)	uartn_dlM
81050008h	Enhanced Feature Register	UARTn_EFR
81050010h	XON1	UARTn_XON1
81050014h	XON2	UARTn_XON2
81050018h	XOFF1	UARTn_XOFF1
8105001Ch	XOFF2	UARTn_XOFF2
81050020h	AUTOBAUD_EN	UARTn_AUTOBAUD_EN
81050024h	HIGH SPEED UART	UARTn_HIGHSPEED
81050028h	SAMPLE_COUNT	UARTn_SAMPLE_COUNT
8105002Ch	SAMPLE_POINT	UARTn_SAMPLE_POINT
81050030h	AUTOBAUD_REG	UARTn_AUTOBAUD_REG
81050034h	Rate Fix Address	UARTn_RateFix_ad
81050038h	AUTOBAUDSAMPLE	UARTn_AUTOBAUDSAMPLE
8105003Ch	Guard time added register	UARTn_GUARD
81050040h	Escape character register	UARTn_ESCAPE_DAT
81050044h	Escape enable register	UARTn_ESCAPE_EN
81050048h	Sleep enable register	UARTn_SLEEP_EN
8105004Ch	Virtual FIFO enable register	UARTn_VFIFO_EN
81050050h	Rx Trigger Address	UARTn_RXTRI_AD
81050054h	Fractional Divider LSB Address	UARTn_Fracdiv_l

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81050058h	Fractional Divider MSB Address	UARTn_FRACDIV_M

n = 1, 2, 3; for uart1, uart2 and uart3 respectively.

UARTn+0000h RX Buffer Register UARTn_RBR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RBR[7:0]							
Type									RO							

RBR RX Buffer Register. Read-only register. The received data can be read by accessing this register.
Modified when LCR[7] = 0.

UARTn+0000h TX Holding Register UARTn_THR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									THR[7:0]							
Type									WO							

THR TX Holding Register. Write-only register. The data to be transmitted is written to this register, and then sent to the PC via serial communication.
Modified when LCR[7] = 0.

UARTn+0004h Interrupt Enable Register UARTn_IER

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CTSI	RTSI	XOFFI	VFF_FC_EN	EDSSI	ELSI	ETBEI	ERBFI
Type									R/W							
Reset									0							

IER By storing a '1' to a specific bit position, the interrupt associated with that bit is enabled. Otherwise, the interrupt is disabled.
IER[3:0] are modified when LCR[7] = 0.
IER[7:4] are modified when LCR[7] = 0 & EFR[4] = 1.

CTSI Masks an interrupt that is generated when a rising edge is detected on the CTS modem control line.
Note: This interrupt is only enabled when hardware flow control is enabled.
0 Mask an interrupt that is generated when a rising edge is detected on the CTS modem control line.
1 Unmask an interrupt that is generated when a rising edge is detected on the CTS modem control line.

RTSI Masks an interrupt that is generated when a rising edge is detected on the RTS modem control line.
Note: This interrupt is only enabled when hardware flow control is enabled.
0 Mask an interrupt that is generated when a rising edge is detected on the RTS modem control line.
1 Unmask an interrupt that is generated when a rising edge is detected on the RTS modem control line.

XOFFI Masks an interrupt that is generated when an XOFF character is received.
Note: This interrupt is only enabled when software flow control is enabled.
0 Mask an interrupt that is generated when an XOFF character is received.

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1 Unmask an interrupt that is generated when an XOFF character is received.

VFF_FC_EN Enable flow control triggered by RX FIFO full when VFIFO_EN is set.

EDSSI When set ("1"), an interrupt is generated if DDCD, TERI, DDSR or DCTS (MSR[4:1]) becomes set.

0 No interrupt is generated if DDCD, TERI, DDSR or DCTS (MSR[4:1]) becomes set.

1 An interrupt is generated if DDCD, TERI, DDSR or DCTS (MSR[4:1]) becomes set.

ELSI When set ("1"), an interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.

0 No interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.

1 An interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.

ETBEI When set ("1"), an interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level.

0 No interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level.

1 An interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level

ERBFI When set ("1"), an interrupt is generated if the RX Buffer contains data.

0 No interrupt is generated if the RX Buffer contains data.

1 An interrupt is generated if the RX Buffer contains data.

UARTn+0008h Interrupt Identification Register — UARTn_IIR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFOE		ID4	ID3	ID2	ID1	ID0	NINT
Type									RO							
Reset									0	0	0	0	0	0	0	1

IIR Identify if there are pending interrupts; ID4 and ID3 are presented only when EFR[4] = 1.
The following table gives the IIR[5:0] codes associated with the possible interrupts:

IIR[5:0]	Priority Level	Interrupt	Source
000001	-	No interrupt pending	
000110	1	Line Status Interrupt	BI, FE, PE or OE set in LSR (Under IER[2]=1)
000100	2	RX Data Received	RX Data received or RX Trigger Level reached. (Under IER[0]=1)
001100	2	RX Data Timeout	Timeout on character in RX FIFO. (Under IER[0]=1)
000010	3	TX Holding Register Empty	TX Holding Register empty or TX FIFO Trigger Level reached. (Under IER[1]=1)
000000	4	Modem Status change	DDCD, TERI, DDSR or DCTS set in MSR (Under IER[3]=1)
010000	5	Software Flow Control	XOFF Character received (Under IER[5]=1)
100000	6	Hardware Flow Control	CTS or RTS Rising Edge

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			(Under IER[6]=1, EDR[6]=1)

Table 27 The IIR[5:0] codes associated with the possible interrupts

Line Status Interrupt: A RX Line Status Interrupt (IIR[5:0`] == 000110b) is generated if ELSI (IER[2]) is set and any of BI, FE, PE or OE (LSR[4:1]) becomes set. The interrupt is cleared by reading the Line Status Register.

RX Data Received Interrupt: A RX Received interrupt (IER[5:0] == 000100b) is generated if EFRBI (IER[0]) is set and either RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached. The interrupt is cleared by reading the RX Buffer Register or the RX FIFO (if enabled).

RX Data Timeout Interrupt:

When virtual FIFO mode is disabled, RX Data Timeout Interrupt is generated if all of the following apply:

1. FIFO contains at least one character;
2. The most recent character was received longer than four character periods ago (including all start, parity and stop bits);
3. The most recent CPU read of the FIFO was longer than four character periods ago.

The timeout timer is restarted on receipt of a new byte from the RX Shift Register, or on a CPU read from the RX FIFO.

The RX Data Timeout Interrupt is enabled by setting EFRBI (IER[0]) to 1, and is cleared by reading RX FIFO.

When virtual FIFO mode is enabled, RX Data Timeout Interrupt is generated if all of the following apply:

1. FIFO is empty;
2. The most recent character was received longer than four character periods ago (including all start, parity and stop bits);
3. The most recent CPU read of the FIFO was longer than four character periods ago.

The timeout timer is restarted on receipt of a new byte from the RX Shift Register.

RX Holding Register Empty Interrupt: A TX Holding Register Empty Interrupt (IIR[5:0] = 000010b) is generated if ETRBI (IER[1]) is set and either the TX Holding Register or, if FIFOs are enabled, the TX FIFO becomes empty. The interrupt is cleared by writing to the TX Holding Register or TX FIFO if FIFO enabled.

Modem Status Change Interrupt: A Modem Status Change Interrupt (IIR[5:0] = 000000b) is generated if EDSSI (IER[3]) is set and either DDCD, TERI, DDSR or DCTS (MSR[3:0]) becomes set. The interrupt is cleared by reading the Modem Status Register.

Software Flow Control Interrupt: A Software Flow Control Interrupt (IIR[5:0] = 010000b) is generated if Software Flow Control is enabled and XOFFI (IER[5]) becomes set, indicating that an XOFF character has been received. The interrupt is cleared by reading the Interrupt Identification Register.

Hardware Flow Control Interrupt: A Hardware Flow Control Interrupt (IER[5:0] = 100000b) is generated if Hardware Flow Control is enabled and either RTSI (IER[6]) or CTSI (IER[7]) becomes set indicating that a rising edge has been detected on either the RTS/CTS Modem Control line. The interrupt is cleared by reading the Interrupt Identification Register.

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UARTn+0008h FIFO Control Register UARTn_FCR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RFTL1	RFTL0	TFTL1	TFTL0	DMA1	CLRT	CLRR	FIFOE
Type									WO							

FCR FCR is used to control the trigger levels of the FIFOs, or flush the FIFOs.
FCR[7:6] is modified when LCR != BFh
FCR[5:4] is modified when LCR != BFh & EFR[4] = 1
FCR[4:0] is modified when LCR != BFh

FCR[7:6] RX FIFO trigger threshold. (RX FIFO contains total 24 bytes.)
0 1
1 6
2 12
3 RXTRIG

FCR[5:4] TX FIFO trigger threshold (TX FIFO contains total 16 bytes.)
0 1
1 4
2 8
3 14 (FIFOSIZE - 2)

DMA1 This bit determines the DMA mode, which the TXRDY and RXRDY pins support. TXRDY and RXRDY act to support single-byte transfers between the UART and memory (DMA mode 0) or multiple byte transfers (DMA mode1). Note that this bit has no effect unless the FIFOE bit is set as well
0 The device operates in DMA Mode 0.
1 The device operates in DMA Mode 1.
TXRDY – mode0: Goes active (low) when the TX FIFO or the TX Holding Register is empty. And it becomes inactive when a byte is written to the Transmit channel.
TXRDY – mode1: Goes active (low) when there are no characters in the TX FIFO. And it becomes inactive when the TX FIFO is full.
RXRDY – mode0: Becomes active (low) when at least one character is in the RX FIFO or the RX Buffer Register is full. And it becomes inactive when there are no more characters in the RX FIFO or RX Buffer register.
RXRDY – mode1: Becomes active (low) when the RX FIFO Trigger Level is reached or an RX FIFO Character Timeout occurs. And it goes inactive when the RX FIFO is empty.

CLRT Clear Transmit FIFO. This bit is self-clearing.
0 Leave TX FIFO intact.
1 Clear all the bytes in the TX FIFO.

CLRR Clear Receive FIFO. This bit is self-clearing.
0 Leave RX FIFO intact.
1 Clear all the bytes in the RX FIFO.

FIFOE FIFO Enabled. This bit must be set to 1 for any of the other bits in the registers to have any effect.
0 Disable both the RX and TX FIFOs.

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1 Enable both the RX and TX FIFOs.

UARTn+000Ch Line Control Register — UARTn_LCR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLAB	SB	SP	EPS	PEN	STB	WLS1	WLS0
Type									R/W							
Reset									0	0	0	0	0	0	0	0

LCR Line Control Register. Determines characteristics of serial communication signals.
Modified when LCR[7] = 0.

DLAB Divisor Latch Access Bit.

- **0** The RX and TX Registers are read/written at Address 0 and the IER register is read/written at Address 4.
- **1** The Divisor Latch LS is read/written at Address 0 and the Divisor Latch MS is read/written at Address 4.

SB Set Break

- **0** No effect
- **1** SOUT signal is forced into the “0” state.

SP Stick Parity

- **0** No effect.
- **1** The Parity bit is forced into a defined state, depending on the states of EPS and PEN:
  If EPS=1 & PEN=1, the Parity bit is set and checked = 0.
  If EPS=0 & PEN=1, the Parity bit is set and checked = 1.

EPS Even Parity Select

- **0** When EPS=0, an odd number of ones is sent and checked.
- **1** When EPS=1, an even number of ones is sent and checked.

PEN Parity Enable

- **0** The Parity is neither transmitted nor checked.
- **1** The Parity is transmitted and checked.

STB Number of STOP bits

- **0** One STOP bit is always added.
- **1** Two STOP bits are added after each character is sent; unless the character length is 5 when 1 STOP bit is added.

WLS1, 0 Word Length Select.

- **0** 5 bits
- **1** 6 bits
- **2** 7 bits
- **3** 8 bits

UARTn+0010h Modem Control Register — UARTn_MCR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF STATUS	~~IR ENABLE~~	X	LOOP	OUT2	OUT1	RTS	DTR
Type									R/W							

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Reset									0	0	0	0	0	0	0	0

MCR Modem Control Register. Control interface signals of the UART.
MCR[4:0] are modified when LCR[7] = 0,
MCR[7:6] are modified when LCR[7] = 0 & EFR[4] = 1.

XOFF Status This is a read-only bit.
- **0** When an XON character is received.
- **1** When an XOFF character is received.

LOOP Loop-back control bit.
- **0** No loop-back is enabled.
- **1** Loop-back mode is enabled.

OUT2 Controls the state of the output NOUT2, even in loop mode.
- **0** NOUT2=1.
- **1** NOUT2=0.

OUT1 Controls the state of the output NOUT1, even in loop mode.
- **0** NOUT1=1.
- **1** NOUT1=0.

RTS Controls the state of the output NRTS, even in loop mode.
- **0** NRTS=1.
- **1** NRTS=0.

DTR Control the state of the output NDTR, even in loop mode.
- **0** NDTR=1.
- **1** NDTR=0.

UARTn+0014h Line Status Register UARTn_LSR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFOERR	TEMT	THRE	BI	FE	PE	OE	DR
Type									R/W							
Reset									0	1	1	0	0	0	0	0

LSR Line Status Register.
Modified when LCR[7] = 0.

FIFOERR RX FIFO Error Indicator.
- **0** No PE, FE, BI set in the RX FIFO.
- **1** Set to 1 when there is at least one PE, FE or BI in the RX FIFO.

TEMT TX Holding Register (or TX FIFO) and the TX Shift Register are empty.
- **0** Empty conditions below are not met.
- **1** If FIFOs are enabled, the bit is set whenever the TX FIFO and the TX Shift Register are empty. If FIFOs are disabled, the bit is set whenever TX Holding Register and TX Shift Register are empty.

THRE Indicates if there is room for TX Holding Register or TX FIFO is reduced to its Trigger Level.

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0 **Reset whenever the contents of the TX FIFO are more than its Trigger Level (FIFOs are enabled), or whenever TX Holding Register is not empty(FIFOs are disabled).**

1 Set whenever the contents of the TX FIFO are reduced to its Trigger Level (FIFOs are enabled), or whenever TX Holding Register is empty and ready to accept new data (FIFOs are disabled).

BI Break Interrupt.

0 Reset by the CPU reading this register

1 If the FIFOs are disabled, this bit is set whenever the SIN is held in the 0 state for more than one transmission time (START bit + DATA bits + PARITY + STOP bits).

If the FIFOs are enabled, this error is associated with a corresponding character in the FIFO and is flagged when this byte is at the top of the FIFO. When a break occurs, only one zero character is loaded into the FIFO: the next character transfer is enabled when SIN goes into the marking state and receives the next valid start bit.

FE Framing Error.

0 Reset by the CPU reading this register

1 If the FIFOs are disabled, this bit is set if the received data did not have a valid STOP bit. If the FIFOs are enabled, the state of this bit is revealed when the byte it refers to is the next to be read.

PE Parity Error

0 Reset by the CPU reading this register

1 If the FIFOs are disabled, this bit is set if the received data did not have a valid parity bit. If the FIFOs are enabled, the state of this bit is revealed when the referred byte is the next to be read.

OE Overrun Error.

0 Reset by the CPU reading this register.

1 If the FIFOs are disabled, this bit is set if the RX Buffer was not read by the CPU before new data from the RX Shift Register overwrote the previous contents.

If the FIFOs are enabled, an overrun error occurs when the RX FIFO is full and the RX Shift Register becomes full. OE is set as soon as this happens. The character in the Shift Register is then overwritten, but not transferred to the FIFO.

DR Data Ready.

0 Cleared by the CPU reading the RX Buffer or by reading all the FIFO bytes.

1 Set by the RX Buffer becoming full or by a byte being transferred into the FIFO.

UARTn+0018h Modem Status Register — UARTn_MSR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS
Type									R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset									Input	Input	Input	Input	0	0	0	0

Note: After a reset, D4-D7 are inputs. A modem status interrupt can be cleared by writing ‘0’ or set by writing ‘1’ to this register. D0-D3 can be written to.

Modified when LCR[7] = 0.

MSR Modem Status Register

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DCD Data Carry Detect.

When Loop = "0", this value is the complement of the NDCD input signal.

When Loop = "1", this value is equal to the OUT2 bit in the Modem Control Register.

RI Ring Indicator.

When Loop = "0", this value is the complement of the NRI input signal.

When Loop = "1", this value is equal to the OUT1 bit in the Modem Control Register.

DSR Data Set Ready

When Loop = "0", this value is the complement of the NDSR input signal.

When Loop = "1", this value is equal to the DTR bit in the Modem Control Register.

CTS Clear To Send.

When Loop = "0", this value is the complement of the NCTS input signal.

When Loop = "1", this value is equal to the RTS bit in the Modem Control Register.

DDCD Delta Data Carry Detect.

0 The state of DCD has not changed since the Modem Status Register was last read

1 Set if the state of DCD has changed since the Modem Status Register was last read.

TERI Trailing Edge Ring Indicator

0 The NRI input does not change since this register was last read.

1 Set if the NRI input changes from “0” to “1” since this register was last read.

DDSR Delta Data Set Ready

0 Cleared if the state of DSR has not changed since this register was last read.

1 Set if the state of DSR has changed since this register was last read.

DCTS Delta Clear To Send

0 Cleared if the state of CTS has not changed since this register was last read.

1 Set if the state of CTS has changed since this register was last read.

UARTn+001Ch Scratch Register UARTn_SCR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SCR[7:0]							
Type									R/W							

A general purpose read/write register. After reset, its value is un-defined.

Modified when LCR[7] = 0.

UARTn+0000h Divisor Latch (LS) UARTn_DLL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLL[7:0]							
Type									R/W							
Reset									1							

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UARTn+0004h Divisor Latch (MS) UARTn_DLM

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLM[7:0]							
Type									R/W							
Reset									0							

Note: DLL & DLM can only be updated if DLAB is set (“1”).. Note too that division by 1 generates a BAUD signal that is constantly high.

Modified when LCR[7] = 1.

The table below shows the divisor needed to generate a given baud rate from CLK inputs of 13, 26 MHz and 52 MHz. The effective clock enable generated is 16 x the required baud rate.

BAUD	6.5MHz	13MHz	26MHz	52MHz
110	3693	7386	14773	29545
300	1354	2708	5417	10833
1200	338	677	1354	2708
2400	169	338	677	1354
4800	85	169	339	677
9600	42	85	169	339
19200	21	42	85	169
38400	11	21	42	85
57600	7	14	28	56
115200	*	6	14	28

Table 28 Divisor needed to generate a given baud rate

UARTn+0008h Enhanced Feature Register UARTn_EFR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AUTO CTS	AUTO RTS	D5	ENABLE -E	SW FLOW CONT[3:0]			
Type									R/W	R/W	R/W	R/W	R/W			
Reset									0	0	0	0	0			

*NOTE: Only when LCR=BF’h

Auto CTS Enables hardware transmission flow control

0 Disabled.

1 Enabled.

Auto RTS Enables hardware reception flow control

0 Disabled.

1 Enabled.

Enable-E Enable enhancement features.

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0 Disabled.
1 Enabled.

CONT[3:0] Software flow control bits.

00xx No TX Flow Control
10xx Transmit XON1/XOFF1 as flow control bytes
01xx Transmit XON2/XOFF2 as flow control bytes
11xx Transmit XON1 & XON2 and XOFF1 & XOFF2 as flow control words
xx00 No RX Flow Control
xx10 Receive XON1/XOFF1 as flow control bytes
xx01 Receive XON2/XOFF2 as flow control bytes
xx11 Receive XON1 & XON2 and XOFF1 & XOFF2 as flow control words

UARTn+0010h XON1 — UARTn_XON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON1[7:0]							
Type									R/W							
Reset									0							

UARTn+0014h XON2 — UARTn_XON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON2[7:0]							
Type									R/W							
Reset									0							

UARTn+0018h XOFF1 — UARTn_XOFF1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF1[7:0]							
Type									R/W							
Reset									0							

UARTn+001Ch XOFF2 — UARTn_XOFF2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF2[7:0]							
Type									R/W							
Reset									0							

*Note: XON1, XON2, XOFF1, XOFF2 are valid only when LCR=BFh.

UARTn+0020h AUTOBAUD_EN — UARTn_AUTOBAUD_EN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																AUTO_EN

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Type																R/W
Reset																0

AUTOBAUD_EN Auto-baud enable signal

- **0** Auto-baud function disable
- **1** Auto-baud function enable (UARTn+0024h SPEED should be set 0)

UARTn+0024h HIGH SPEED UART — UARTn_HIGHSPEED

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SPEED [1:0]	
Type															R/W	
Reset															0	

SPEED UART sample counter base

- **0** based on 16*baud_pulse, baud_rate = system clock frequency/16/{DLH, DLL}
- **1** based on 8*baud_pulse, baud_rate = system clock frequency/8/{DLH, DLL}
- **2** based on 4*baud_pulse, baud_rate = system clock frequency/4/{DLH, DLL}
- **3** based on sampe_count * baud_pulse, baud_rate = system clock frequency / sampe_count

The table below shows the divisor needed to generate a given baud rate from CLK inputs of 13M Hz based on different HIGHSPEED value.

BAUD	HIGHSPEED = 0	HIGHSPEED = 1	HIGHSPEED = 2
110	3693	7386	14773
300	1354	2708	7386
1200	338	677	2708
2400	169	338	677
4800	85	169	338
9600	42	85	169
19200	21	42	85
38400	11	21	42
57600	7	14	21
115200	*	7	14
230400	*	*	7
460800	*	*	*
921600	*	*	*

Table 29 Divisor needed to generate a given baud rate from 13MHz based on different HIGHSPEED value

The table below shows the divisor needed to generate a given baud rate from CLK inputs of 6.5 MHz based on different HIGHSPEED value.

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BAUD	HIGHSPEED = 0	HIGHSPEED = 1	HIGHSPEED = 2
110	7386	14773	29545
300	2708	7386	14773
1200	677	2708	7386
2400	338	677	2708
4800	169	338	677
9600	85	169	338
19200	42	85	169
38400	21	42	85
57600	14	21	42
115200	7	14	21
230400	*	7	14
460800	*	*	7
921600	*	*	*

Table 30 Divisor needed to generate a given baud rate from 13MHz based on different HIGHSPEED value

The table below shows the divisor needed to generate a given baud rate from CLK inputs of 13 MHz based on different HIGHSPEED value.

BAUD	HIGHSPEED = 0	HIGHSPEED = 1	HIGHSPEED = 2
110	14773	29545	59091
300	5417	14773	29545
1200	1354	5417	14773
2400	677	1354	5417
4800	339	677	1354
9600	169	339	667
19200	85	169	339
38400	42	85	169
57600	28	42	85
115200	14	28	42
230400	7	14	28
460800	*	7	14
921600	*	*	7

Table 31 Divisor needed to generate a given baud rate from 26 MHz based on different HIGHSPEED value

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The table below shows the divisor needed to generate a given baud rate from CLK inputs of 26MHz based on different HIGHSPEED value.

BAUD	HIGHSPEED = 0	HIGHSPEED = 1	HIGHSPEED = 2
110	29545	59091	118182
300	10833	29545	59091
1200	2708	10833	29545
2400	1354	2708	10833
4800	677	1354	2708
9600	339	677	1354
19200	169	339	677
38400	85	169	339
57600	56	85	169
115200	28	56	85
230400	14	28	56
460800	7	14	28
921600	*	7	14

Table 32 Divisor needed to generate a given baud rate from 52 MHz based on different HIGHSPEED value

UARTn+0028h SAMPLE_COUNT UARTn_SAMPLE_COUNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPLECOUNT [7:0]							
Type									R/W							
Reset									0							

When HIGHSPEED=3, the sample_count is the threshold value for UART sample counter (sample_num).

Count from 0 to sample_count.

UARTn+002Ch SAMPLE_POINT UARTn_SAMPLE_POINT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPLEPOINT [7:0]							
Type									R/W							
Reset									Ffh							

When HIGHSPEED=3, UART gets the input data when sample_count=sample_num.

e.g. system clock = 13MHz, 921600 = 13000000 / 14

sample_count = 14 and sample point = 6 (sample the central point to decrease the inaccuracy)

The SAMPLE_POINT is usually (SAMPLE_COUNT-1)/2 and remove the decimal.

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UARTn+0030h AUTOBAUD_REG — UARTn_AUTOBAUD_REG

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BAUD_STAT[3:0]				BAUDRATE[3:0]			
Type									RO				RO			
Reset									0				0			

BAUD_RATE Autobaud baud rate

- **0** 115200
- **1** 57600
- **2** 38400
- **3** 19200
- **4** 9600
- **5** 4800
- **6** 2400
- **7** 1200
- **8** 300
- **9** 110

BAUDSTAT Autobaud format

- **0** Autobaud is detecting
- **1** AT_7N1
- **2** AT_7O1
- **3** AT_7E1
- **4** AT_8N1
- **5** AT_8O1
- **6** AT_8E1
- **7** at_7N1
- **8** at_7E1
- **9** at_7O1
- **10** at_8N1
- **11** at_8E1
- **12** at_8O1
- **13** Autobaud detection fails

UARTn+0034h Rate Fix Address — UARTn_RATEFIX_AD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RESTRICT	FREQ_SEL	AUTOBAUD_RATE_FIX	RXTE_FIX
Type													R/W	R/W	R/W	R/W
Reset													0	0	0	0

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RATE_FIX When you set "rate_fix"(34H[0]), you can transmit and receive data only if 1) the f13m_en is enable and the freq_sel (34H[2]) is set to 1, or
2) the f26m_en is enable and the freq_sel (34H[2]) is set to 0.

AUTOBAUD_RATE_FIX When you set "autobaud_rate_fix"(34H[1]), you can tx/rx the autobaud packet only if
1) the f13m_en is enable and the freq_sel (34H[2]) is set to 1, or
2) the f26m_en is enable and the freq_sel (34H[2]) is set to 0.

FREQ_SEL
- **0** Select f26m_en for rate_fix and autobaud_rate_fix
- **1** Select f13m_en for rate_fix and autobaud_rate_fix

RESTRICT The "restrict" (34H[3]) is used to set a more condition for the autobaud fsm starting point

UARTn+0038h AUTOBAUDSAMPLE — UARTn_AUTOBAUDSAMPLE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										AUTOBAUDSAMPLE						
Type										R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset										dh						

Since the system clock may change, autobaud sample duration should change as system clock changes.
When system clock = 13MHz, autobaudsample = 6; when system clock = 26MHz, autobaudsample = 13.

UARTn+003Ch Guard time added register — UARTn_GUARD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												GUARD_EN	GUARD_CNT[3:0]			
Type												R/W	R/W	R/W	R/W	R/W
Reset												0	0	0	0	0

GUARD_CNT Guard interval count value. Guard interval = (1/(system clock / div_step / div)) * GUARD_CNT.

GUARD_EN Guard interval add enable signal.
- **0** No guard interval added.
- **1** Add guard interval after stop bit.

UARTn+0040h Escape character register — UARTn_ESCAPE_DAT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ESCAPE_DAT[7:0]							
Type									R/W							
Reset									FFh							

ESCAPE_DAT Escape character added before software flow control data and escape character, i.e. if tx data is xon (31h), with esc_en =1, uart transmits data as esc + CEh (~xon).

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UARTn+0044h Escape enable register — UARTn_ESCAPE_EN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ESC_EN
Type																R/W
Reset																0

ESC_EN Add escape character in transmitter and remove escape character in receiver by UART.

- **0** Do not deal with the escape character.
- **1** Add escape character in transmitter and remove escape character in receiver.

UARTn+0048h Sleep enable register — UARTn_SLEEP_EN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SELLP_EN
Type																R/W
Reset																0

SLEEP_EN For sleep mode issue

- **0** Do not deal with sleep mode indicate signal
- **1** To activate hardware flow control or software control according to software initial setting when chip enters sleep mode. Releasing hardware flow when chip wakes up; but for software control, uart sends xon when awaken and when FIFO does not reach threshold level.

UARTn+004Ch RX Virtual FIFO enable register — UARTn_RXVFF_EN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RXVFF_EN
Type																R/W
Reset																0

RXVFF_EN UART RX Virtual FIFO mechanism enable signal.

- **0** Disable RX VFIFO mode.
- **1** Enable RX VFIFO mode. When UART RX virtual mode is enabled, the flow control is based on the DMA threshold, and generates a timeout interrupt for DMA.

UARTn+0050h Rx Trigger Address — UARTn_RXTRI_AD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RXTRIG[3:0]			
Type													R/W			
Reset													0			

RXTRIG When {rtm,rtl}=2'b11, The Rx FIFO threshold will be Rxtrig.

The value is suggested to be less than half of RX FIFO size, which is 24 Bytes.

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UARTn+0054h Fractional Divider LSB Address UARTn_FRACDIV_L

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FRACDIV_L							
Type									R/W							
Reset									0	0	0	0	0	0	0	0

FRACDIV_L Add sampling count (+1) from state data7 to data0, in order to contribute fractional divisor.

UARTn+0058h Fractional Divider MSB Address UARTn_FRACDIV_M

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FRACDIV_M	
Type															R/W	
Reset															0	0

FRACDIV_M Add sampling count when in state stop to parity, in order to contribute fractional divisor.

UARTn+005Ch FIFO Control Register UARTn_FCR_RD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RFTL1	RFTL0	TFTL1	TFTL0	DMA1	CLRT	CLRR	FIFOE
Type									RO							

Please refer to UARTn_FCR register.

4.8 IrDA Framer

4.8.1 General Description

IrDA framer is implemented to reduce the CPU loading for IrDA transmissions by performing all the physical level protocol framing in hardware. From a software perspective, the framer need only prepare and process the raw data for transmission and reception. Generic DMA is required to move the data between IrDA framer's internal FIFO and software-designated memory. The IrDA framer supports IrDA SIR, MIR, and FIR modes of operation. SIR mode includes operation from 9600bps ~ 115200bps, MIR includes operation at 567000bps or 1152000bps, and FIR mode includes operation at 4Mbps.

4.8.2 Register Definitions

IRDA+0000h TX BUF and RX BUF BUF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BUF[7:0]							
Type									R/W							
Reset									0							

BUF IrDA Framer transmit or receive data.

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A write to this register writes into the internal TX FIFO.
A read from this register reads from the internal RX FIFO.

IRDA+0004h TX BUF and RX BUF clear signal BUF_CLEAR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CLEAR
Type																R/W
Reset																0

CLEAR **SIR mode only**. When CLEAR=1, both the TX and RX FIFO are cleared. This is used primarily for debug purpose. Normal operation does not require this. This control signaled can only be issued under SIR mode.

IRDA+0008h Maximum Turn Around Time MAX_T

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MAX_T [13:0]													
Type			R/W													
Reset			3E80h													

MAX_T The maximum time that a station can hold the P/F bit. This parameter along with the baud rate parameter dictates the maximum number of bytes that a station can transmit before passing the line to another station by transmitting a frame with the P/F bit. This parameter is used by one station to indicate the maximum time the other station can send before it must turn the link around. For baud rates less than 115200 kbps, 500 ms is the only valid value. The default value is 500 ms.

IRDA+000Ch Minimum Turn Around Time MIN_T

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_T [15:0]															
Type	R/W															
Reset	FDE8h															

MIN_T Minimum turn around time, the default value is 10 ms. The minimum turn around time parameter deals with the time needed for a receiver to recover following saturation by transmission from the same device. This parameter corresponds to the required time delay between the last byte of the last frame sent by a station and the point at which it is ready to receive the first byte of a frame from another station, i.e. the latency for a transmit to complete and be ready to receive.

IRDA+0010h Number of additional BOFs prefixed to the beginning of a frame BOFS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TYPE	BOFS [6:0]						
Type									R/W	R/W						
Reset									0	1011b						

BOFs **For SIR mode**: the additional BOFs parameter indicates the number of additional flags needed at the beginning of every frame. The main purpose for the additional BOFs is to provide a delay at the beginning of each frame for devices with a long interrupt latency.

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For MIR mode: This parameter indicates the number of double STA's to transmit in the beginning. This value should be set to 0 (for default 2 STA's) for MIR mode, unless more are required.

For FIR mode: This parameter has no effect.

TYPE **SIR mode only**. Additional BOFs type.

1 BOF = C0h

0 BOF = FFh

IRDA+0014h Baud rate divisor DIV

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIV[15:0]															
Type	R/W															
Reset	55h															

DIV Transmit or receive rate divider. Rate = System clock frequency / DIV/ 16. The default value is 55h when in contention mode. **This divisor is also used to determine the RX FIFO timeout threshold.**

IRDA+0018h Transmit frame size TX_FRAME_SIZE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_FRAME_SIZE[11:0]											
Type					R/W											
Reset					40h											

TX_FRAME_SIZE Transmit frame size; the default value is 64 when in contention mode.

IRDA+001Ch Receiving frame1 size RX_FRAME1_SIZE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_FRAME1_SIZE[11:0]											
Type					RO											
Reset					0											

RX_FRAME1_SIZE Reports the number of byte received. Includes only the A+C+I fields.

IRDA+0020h Transmit abort indication ABORT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ABORT
Type																R/W
Reset																0

ABORT **SIR mode only**. When set 1, the framer transmits an abort sequence and closes the frame without an FCS field or an ending flag.

Note: Tx abort can be achieved in MIR and FIR by simply disabling the tx_en signal.

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IRDA+0024h IrDA framer transmit enable signal TX_EN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TX_ONE	TXINVERT	MODE	TX_EN
Type													R/W	R/W	R/W	R/W
Reset													0	0	0	0

TX_EN Transmit enable.

MODE SIR mode only. Modulation type selection.

- **0** 3/16 modulation
- **1** 1.61us

TXINVERT Invert the transmit signal.

- **0** Transmit signal is not inverted.
- **1** Transmit signal is inverted.

TX_ONE: Controls the transmit enable signal is one or not.

- **0** tx_en is not de-asserted until software programs a so.
- **1** tx_en is de-asserted (i.e. transmit disabled) automatically after one frame has been sent.

IRDA+0028h IrDA framer receive enable signal RX_EN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RX_ONE	RXINVERT	RX_EN
Type														R/W	R/W	R/W
Reset														0	0	0

RX_EN Receive enable.

RXINVERT Invert the receive signal.

- **0** Receive signal is not inverted.
- **1** Receive signal is inverted.

RX_ONE Disable receive when get one frame.

- **0** rx_en is not de-asserted until software programs so.
- **1** rx_en is de-asserted (i.e. transmit disabled) automatically after one frame has been sent.

IRDA+002Ch FIFO trigger level indication TRIGGER

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RX_TRIG[		TX_TRIG	
Type													R/W		R/W	
Reset													0		0	

TX_TRIG TX FIFO interrupt trigger threshold. When the amount of data in the TX FIFO is less than the specified amount, dma req is asserted. (When TX_TRIG = 03, dma req is always asserted as long as FIFO is not full.)

- **00** 0 byte
- **01** 1 byte
- **02** 8 byte

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03 16 byte

RX_TRIG RX FIFO interrupt trigger threshold. When the amount of data in RX FIFO is above the specified amount, dma req is asserted.

00 1 byte

01 2 byte

02 3 byte

IRDA+0030h IRQ enable signal IRQ_ENABLE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				2NDRX_COMP	RXRESTART	THRESHTIMEOUT	FIFOTIMEOUT	TXABORT	RXABORT	MAXTIMEOUT	MINTIMEOUT	RXCOMPLETE	TXCOMPLETE	ERROR	RXTHRES	TXTHRES
Type					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset					0	0	0	0	0	0	0	0	0	0	0	0

TXRES Transmit data reaches the threshold level. (For debug only. Should be set to 0.)

0 No interrupt is generated.

1 Interrupt is generated when transmit FIFO size reaches threshold.

RXRES Receive data reaches the threshold level. (For debug only. Should be set to 0.)

0 No interrupt is generated.

1 Interrupt is generated when receive FIFO size reaches threshold.

ERROR Error status interrupt enable.

0 No interrupt is generated.

1 Interrupt is generated when one of the error statuses occurs.

TXCOMPLETE Transmit one frame completely.

0 No interrupt is generated.

1 Interrupt is generated when transmitting one frame completely.

RXCOMPLETE Receive one frame completely.

0 No interrupt is generated.

1 Interrupt is generated when receiving one frame completely.

MINTIMEOUT Minimum time timeout.

0 No interrupt is generated.

1 Interrupt is generated when minimum timer is timed out.

MAXTIMEOUT Maximum time timeout.

0 No interrupt is generated.

1 Interrupt is generated when maximum timer is timed out.

RXABORT Receiving aborting frame.

0 No interrupt is generated.

1 Interrupt is generated when receiving aborting frame.

TXABORT **SIR mode only**. Transmitting aborting frame.

0 No interrupt is generated.

1 Interrupt is generated when transmitting aborting frame.

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FIFOTIMEOUT FIFO timeout.

- **0** No interrupt is generated.
- **1** Interrupt is generated when FIFO timeout.

THRESHTIMEOUT Threshold time timeout.

- **0** No interrupt is generated.
- **1** Interrupt is generated when threshold timer is timed out.

RXRESTART **SIR mode only**. Receiving a new frame before one frame is received completely.

- **0** No interrupt is generated.
- **1** Interrupt is generated when receiving a new frame before one frame is received completely.

2NDRX_COMP Receiving second frame and get P/F bit.

- **0** No interrupt is generated.
- **1** Interrupt is generated when receiving second frame and get P/F bit completely.

IRDA+0034h Interrupt Status IRQ_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				2NDRX_COMP	RXRESTART	THRESHTIMEOUT	FIFOTIMEOUT	TXABORT	RXABORT	MAXTIMEOUT	MINTIMEOUT	RXCOMPLETE	TXCOMPLETE	ERROR	RXTRES	TXTRES
Type				RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

TXFIFO Transmit FIFO reaches threshold. (For debug only. Not recommended for normal usage.)

RXFIFO Receive FIFO reaches threshold. (For debug only. Not recommended for normal usage.)

ERROR Generated when any of status in Error Status register occurs.
Once the source of an interrupt is determined to be caused by an error (bit 2), the error status register should be read. Once read, both the error status register and the interrupt source are read-cleared. If the error status register indicates either a frame 1 or frame 2 error, the corresponding frame status register should be read.

TXCOMPLETE Transmitting one frame completely.

RXCOMPLETE Receiving one frame completely.

MINTIMEOUT Minimum turn around time timeout.

MAXTIMEOUT Maximum turn around time timeout.

RXABORT Receiving aborting frame.

TXABORT Transmitting aborting frame.

FIFOTIMEOUT FIFO is timeout.

THRESHTIMEOUT Threshold time timeout.

RXRESTART Receiving a new frame before one frame is received completely.

2NDRX_COMP Receiving second frame and get P/F bit completely.

IRDA+0038h ERROR STATUS register ERR_STATUS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										TX FIFO UNDERRUN	FRAME 2 DATA ERR	FRAME 1 DATA ERR	RESERVED2	RESERVED	OVERRUN	RXSIZE

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Type										R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset										0	0	0	0	0	0	0

RXSIZE Receive frame size error.
OVERRUN Frame overrun.
RESERVED Reserved for future use.
RESERVED2 Reserved for future use.
FRAME1 DATA ERR Indicates that an error condition occurred in RX frame1. Must check the RX frame1 status.
FRAME2 DATA ERR Indicates that an error condition occurred in RX frame2. Must check the RX frame2 status.
TX FIFO UNDERRUN **MIR and FIR mode only**.
TX FIFO underrun has occurred. Data transmission is aborted. Software must reset the tx_en signal.

IRDA+003Ch Transceiver power on/off control. Transceiver mode select. TRANSCEIVER_PDN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														TXCVR CONFIG	TX MANUAL	TRANS_ PDN
Type														R/W	R/W	R/W
Reset														0	0	0

TRANSCEIVER_PDN Used for power on/off control for external IrDA transceiver.
TX_MANUAL When txcvr config is set to 1, this bit can be used to select the operation mode of the external IrDA transceiver (some transceivers require selection between high speed and low speed operating modes), by software programming the desired sequence to transmit through the irda_txd pin.
TXCVR CONFIG
0 Irda_txd comes from core logic.
1 Irda_txd depends on tx_manual value.

IRDA+0040h Maximum number of receiving frame size RX_FRAME_MAX

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					MAX_RX_FRAME_SIZE_											
Type					R/W											
Reset					0											

RX_FRAME_MAX Receive frame I field max size, when actual receiving frame size is larger than rx_frame_max, RXSIZE is asserted. The maximum allowed I field size is 2048.

IRDA+0044h Threshold Time THRESH_T

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISCONNECT_TIME[15:0]															
Type	R/W															
Reset	bb8h															

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THRESHOLD TIME Threshold time; used to control the time a station waits without receiving a valid frame before disconnecting the link. Associated with this is the time a station waits without receiving a valid frame before sending a status indication to the service user layer.

IRDA+0048h Counter enable signal COUNT_ENABLE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														THRESH_EN	MIN_EN	MAX_EN
Type														R/W	R/W	R/W
Reset														0	0	0

COUNT_ENABLE Counter enable signals.

IRDA+004Ch Indication of system clock rate CLOCK_RATE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CLOCK_RATE	
Type															R/W	
Reset															0	

CLOCK_RATE **SIR mode only** Indication of the system clock rate.

- **0** 26 MHz
- **1** 52 MHz
- **2** 13 MHz

IRDA+0050h System Clock Rate Fix RATE_FIX

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												MIR TIMING TUNE		CRC REPORT	SIR FRAMING SET	RATE_FIX
Type												R/W		R/W	R/W	R/W
Reset												0		0	0	0

RATE_FIX **SIR mode only** Fix the IrDA framer sample base clock rate as 13 MHz.

- **0** Clock rate based on clock_rate selection.
- **1** Clock rate fixed at 13 MHz.

SIR FRAMING SET **SIR mode only**. Framing error check condition.

- **0** Ignore the STOP bit of the last byte of a frame.
- **1** Check the STOP bit of the last byte of a frame.

CRC REPORT When set to 1, CRC error is reported via error status register and error interrupt.

MIR TIMING TUNE[1:0] **MIR mode only**. For some transceivers, in MIR 0.576mbps mode, the RX output pulse does not conform to IRDA specification. Therefore, this option is used to detect the RX output from those transceivers correctly.

- **0** For transceivers that conform to spec.

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1 For transceivers that do not conform to spec, and the RX output pulse is half of that specified.
2 For transceivers that do not conform to spec, and the RX output pulse is quarter of that specified.

IRDA+0054h RX Frame1 Status FRAME1_STATUS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										FIR STO ERR	FIR 4PPM ERR	MIR HDLC ERR	UNKNOW _ERROR	PF_DETECT	CRC_FAIL	FRAME_ERROR
Type										R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset										0	0	0	0	0	0	0

FRAME_ERROR **SIR mode only**. Framing error, i.e. STOP bit = 0.
- **0** No framing error
- **1** Framing error occurred

CRC_FAIL CRC check fail
- **2** CRC check successfully
- **3** CRC check fail

PF_DETECT P/F bit detect
- **0** Not a P/F bit frame
- **1** Detected P/F bit in this frame

UNKNOWN_ERROR **SIR mode only**. Receiving error data, i.e. escape character is followed by a character that is not an ESC, BOF, or EOF character.
- **0** Data received correctly.
- **1** Unknown error occurred.

MIR HDLC ERR **MIR mode only**. MIR HDLC encoding error
- **0** No error
- **1** Error

FIR 4PPM ERR **FIR mode only**. FIR 4ppm encoding error
- **0** No error
- **1** Error

FIR STO ERR **FIR mode only**. FIR STO sequence error
- **0** No error
- **1** Error

IRDA+0058h RX Frame2 Status FRAME2_STATUS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										FIR STO ERR	FIR 4PPM ERR	MIR HDLC ERR	UNKNOW _ERROR	PF_DETECT	CRC_FAIL	FRAME_ERROR
Type										R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset										0	0	0	0	0	0	0

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FRAME_ERROR **SIR mode only.** Framing error, i.e. STOP bit = 0

- **0** No framing error.
- **1** Framing error occurred.

CRC_FAIL CRC check fail.

- **0** CRC check successfully.
- **1** CRC check fail.

PF_DETECT P/F bit detect.

- **0** Not a P/F bit frame.
- **1** Detected P/F bit in this frame.

UNKNOWN_ERROR **SIR mode only**. Receiving error data, i.e. escape character is followed by a character that is not an ESC, BOF, or EOF character.

- **0** Data receiving correctly.
- **1** Unknown error occurred.

MIR HDLC ERR **MIR mode only**. MIR HDLC encoding error.

- **0** No error
- **1** Error

FIR 4PPM ERR **FIR mode only**.FIR 4ppm encoding error

- **0** No error
- **1** Error

FIR STO ERR **FIR mode only**.FIR STO sequence error

- **0** No error
- **1** Error

IRDA+005Ch Receiving frame2 size RX_FRAME2_SIZE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_FRAME2_SIZE[11:0]											
Type					RO											
Reset					0											

RX_FRAME2_SIZE Reports the number of byte received. Includes only the A+C+I fields.

IRDA+0060h Irda Mode Select IRDA_MODE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														MIR SPEED	IRDA MODE	
Type														R/W	R/W	
Reset														0	00	

IRDA MODE Selects the IrDA operating mode. NOTE: this mode selection cannot be issued while transmitting or receiving.

- **00** IR mode
- **01** MIR mode

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10 FIR mode

MIR SPEED Select the MIR speed.

0 0.576 Mbps

1 1.152 Mbps

IRDA+0064h Fifo Status FIFO_STAT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX FIFO HOLD	TX FIFO WR FULL	TX FIFO RD EMPTY	RX FIFO WR FULL	RX FIFO RD EMPTY
Type												RO	RO	RO	RO	RO
Reset												0	0	1	0	1

This register indicates the real time FIFO status, for monitoring purposes.

4.9 Real Time Clock

4.9.1 General Description

The Real Time Clock (RTC) module provides time and data information. The clock is based on a 32.768KHz oscillator with an independent power supply. When the mobile handset is powered off, a dedicated regulator supplies the RTC block. If the main battery is not present, a backup supply such as a small mercury cell battery or a large capacitor is used. In addition to providing timing data, an alarm interrupt is generated and can be used to power up the baseband core via the BBWAKEUP pin. Regulator interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value reaches a maximum value (e.g., 59 for seconds and minutes, 23 for hours, etc.). The year span is supported up to 2127. The maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

4.9.2 Register Definitions

REGISTER ADDRESS	REGISTER NAME	SYNONYM
0x810c_0000	Baseband power up	RTC_BBPU
0x810c_0004	RTC IRQ status	RTC_IRQ_STA
0x810c_0008	RTC IRQ enable	RTC_IRQ_EN
0x810c_000C	Counter increment IRQ enable	RTC_CII_EN
0x810c_0010	RTC alarm mask	RTC_AL_MASK
0x810c_0014	RTC seconds time counter register	RTC_TC_SEC
0x810c_0018	RTC minutes time counter register	RTC_TC_MIN
0x810c_001C	RTC hours time counter register	RTC_TC_HOU
0x810c_0020	RTC day-of-month time counter register	RTC_TC_DOM
0x810c_0024	RTC day-of-week time counter register	RTC_TC_DOW

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0x810c_0028	RTC month time counter register	RTC_TC_MTH
0x810c_002C	RTC year time counter register	RTC_TC_YEA
0x810c_0030	RTC second alarm setting register	RTC_AL_SEC
0x810c_0034	RTC minute alarm setting register	RTC_AL_MIN
0x810c_0038	RTC hour alarm setting register	RTC_AL_HOU
0x810c_003C	RTC day-of-month alarm setting register	RTC_AL_DOM
0x810c_0040	RTC day-of-week alarm setting register	RTC_AL_DOW
0x810c_0044	RTC month alarm setting register	RTC_AL_MTH
0x810c_0048	RTC year alarm setting register	RTC_AL_YEA
0x810c_004C	XOSC bias current control register	RTC_XOSCCALI
0x810c_0050	RTC_POWERKEY1 register	RTC_POWERKEY1
0x810c_0054	RTC_POWERKEY2 register	RTC_POWERKEY2
0x810c_0058	PDN1	RTC_PDN1
0x810c_005C	PDN2	RTC_PDN2
0x810c_0064	Spare register for specific purpose	RTC_SPAR1
0x810c_0068	Lock / unlock scheme to prevent RTC miswriting	RTC_PROT
0x810c_006c	One-time calibration offset	RTC_DIFF
0x810c_0070	Repeat calibration offset	RTC_CALI
0x810c_0074	Enable the transfers from core to RTC in the queue	RTC_WRTGR

Table 33 RTC Register Map

0x810c_0000 Baseband power up RTC_BBPU

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY_BBPU								DBING	CBUSY	RELOAD	CLRPKY	AUTO	BBPU	WRITE_EN	PWREN
Type	WO								RO	RO	WO	WO	R/W	R/W	R/W	R/W

KEY_BBPU A bus write is acceptable only when KEY_BBPU=0x43.

DBING This bit indicates RTC is still de-bouncing.

CBUSY The read/write channels between RTC / Core is busy. This bit indicates high after software program sequence to anyone of RTC data registers and enable the transfer by RTC_WRTGR=1. By the way, it is high after the reset from low to high because RTC reload process.

RELOAD Reload the values from RTC domain to Core domain. Generally speaking, RTC will reload synchronize the data from RTC to core when reset from 0 to 1. This bit can be treated as debug bit.

CLRPKY Clear powerkey1 and powerkey2 at the same time. In some cases, software may clear powerkey1 & powerkey2. The BBWAKEUP depends on the matching specific patterns of powerkey1 and powerkey2. If any one of powerkey1 or powerkey2 or BBPU is cleared, BBWAKEUP goes low immediately. Software can’t program the

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other control bits without power. By program RTC_BBPU with CLRPKY=1 and BBPU=0 condition, RTC can clear powerkey1, powerkey2 and BBPU at the same moment.

AUTO Controls if BBWAKEUP is automatically in the low state when SYSRST# transitions from high to low.

- **0** BBWAKEUP is not automatically in the low state when SYSRST# transitions from high to low.
- **1** BBWAKEUP is automatically in the low state when SYSRST# transitions from high to low.

BBPU Controls the power of PMIC. If powerkey1=A357h and powerkey2=67D2h, PMIC takes on the value programmed by software; otherwise PMIC is low.

- **0** Power down
- **1** Power on

WRITE_EN When WRITE_EN is write 0 by the MCU, the RTC programing interface is disabled immediately (MCU can't program RTC). After the debounce counter is time-out, the interface enabled again (MCU can program RTC). The debounce counter time-out period is decided by RTC_PDN1. Note that the WRITE_EN value read out is meaningless. The hardware only care about the "write-0 action" to WRITE_EN control bit.

When WRITE_EN==0, avoid to "read out RTC_BBPU, AND/OR something and write back", like this -> *RTC_BBPU=*RTC_BBPU|RTC_BBPU_KEY|0x1. This would disable RTC write interface for a while and hard to debug.

PWREN

- **0** RTC alarm has no action on power switch.
- **1** When an RTC alarm occurs, BBPU is set to 1 and the system powers on by RTC alarm wakeup.

0x810c_0004 RTC IRQ status RTC_IRQ_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															TCSTA	ALSTA
Type															R/C	R/C

ALSTA This register indicates the IRQ status and whether or not the alarm condition has been met.

- **0** No IRQ occurred; the alarm condition has not been met.
- **1** IRQ occurred; the alarm condition has been met.

TCSTA This register indicates the IRQ status and whether or not the tick condition has been met.

- **0** No IRQ occurred; the tick condition has not been met.
- **1** IRQ occurred; the tick condition has been met.

0x810c_0008 RTC IRQ enable RTC_IRQ_EN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														ONESHOT	TC_EN	AL_EN
Type														R/W	R/W	R/W

The function is only active when RTC_POWERKEY1 & RTC_POWERKEY2 match the correct values.

ONESHOT Controls automatic reset of AL_EN and TC_EN.

AL_EN This register enables the control bit for IRQ generation if the alarm condition has been met.

- **0** Disable IRQ generations.

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1 Enable the alarm time match interrupt. Clear the interrupt when ONESHOT is high upon generation of the corresponding IRQ.

TC_EN This register enables the control bit for IRQ generation if the tick condition has been met.

0 Disable IRQ generations.

1 Enable the tick time match interrupt. Clear the interrupt when ONESHOT is high upon generation of the corresponding IRQ.

0x810c_000C Counter increment IRQ enable RTC_CII_EN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							1/8SECCII	1/4SECCII	1/2SECCII	YEACII	MTHCII	DOWCII	DOMCII	HOUCII	MINCII	SECCII
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This register activates or de-activates the IRQ generation when the TC counter reaches its maximum value.

SECCII Set this bit to 1 to activate the IRQ at each second update.
MINCII Set the bit to 1 to activate the IRQ at each minute update.
HOUCII Set the bit to 1 to activate the IRQ at each hour update.
DOMCII Set the bit to 1 to activate the IRQ at each day-of-month update.
DOWCII Set the bit to 1 to activate the IRQ at each day-of-week update.
MTHCII Set the bit to 1 to activate the IRQ at each month update.
YEACII Set the bit to 1 to activate the IRQ at each year update.
1/2SECCII Set the bit to 1 to activate the IRQ at each one-half of a second update.
1/4SECCII Set the bit to 1 to activate the IRQ at each one-fourth of a second update.
1/8SECCII Set the bit to 1 to activate the IRQ at each one-eighth of a second update.

0x810c_0010 RTC alarm mask RTC_AL_MASK

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										YEA_MSK	MTH_MSK	DOW_MSK	DOM_MSK	HOU_MSK	MIN_MSK	SEC_MSK
Type										R/W	R/W	R/W	R/W	R/W	R/W	R/W

The alarm condition for alarm IRQ generation depends on whether or not the corresponding bit in this register is masked. Warning: If you set all bits 1 in RTC_AL_MASK (i.e. RTC_AL_MASK=0x7f) and PWREN=1 in RTC_BBPU, it means alarm comes EVERY SECOND, not disabled.

SEC_MSK

0 Condition (RTC_TC_SEC = RTC_AL_SEC) is checked to generate the alarm signal.

1 Condition (RTC_TC_SEC = RTC_AL_SEC) is masked, i.e. the value of RTC_TC_SEC does not affect the alarm IRQ generation.

MIN_MSK

0 Condition (RTC_TC_MIN = RTC_AL_MIN) is checked to generate the alarm signal.

1 Condition (RTC_TC_MIN = RTC_AL_MIN) is masked, i.e. the value of RTC_TC_MIN does not affect the alarm IRQ generation.

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HOU_MSK

- **0** Condition (RTC_TC_HOU = RTC_AL_HOU) is checked to generate the alarm signal.
- **1** Condition (RTC_TC_HOU = RTC_AL_HOU) is masked, i.e. the value of RTC_TC_HOU does not affect the alarm IRQ generation.

DOM_MSK

- **0** Condition (RTC_TC_DOM = RTC_AL_DOM) is checked to generate the alarm signal.
- **1** Condition (RTC_TC_DOM = RTC_AL_DOM) is masked, i.e. the value of RTC_TC_DOM does not affect the alarm IRQ generation.

DOW_MSK

- **0** Condition (RTC_TC_DOW = RTC_AL_DOW) is checked to generate the alarm signal.
- **1** Condition (RTC_TC_DOW = RTC_AL_DOW) is masked, i.e. the value of RTC_TC_DOW does not affect the alarm IRQ generation.

MTH_MSK

- **0** Condition (RTC_TC_MTH = RTC_AL_MTH) is checked to generate the alarm signal.
- **1** Condition (RTC_TC_MTH = RTC_AL_MTH) is masked, i.e. the value of RTC_TC_MTH does not affect the alarm IRQ generation.

YEA_MSK

- **0** Condition (RTC_TC_YEA = RTC_AL_YEA) is checked to generate the alarm signal.
- **1** Condition (RTC_TC_YEA = RTC_AL_YEA) is masked, i.e. the value of RTC_TC_YEA does not affect the alarm IRQ generation.

0x810c_0014 RTC seconds time counter register RTC_TC_SEC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TC_SECOND					
Type											R/W					

TC_SECOND The second initial value for the time counter. The range of its value is: 0-59.

0x810c_0018 RTC minutes time counter register RTC_TC_MIN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TC_MINUTE					
Type											R/W					

TC_MINUTE The minute initial value for the time counter. The range of its value is: 0-59.

0x810c_001C RTC hours time counter register RTC_TC_HOU

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TC_HOUR				
Type												R/W				

TC_HOUR The hour initial value for the time counter. The range of its value is: 0-23.

0x810c_0020 RTC day-of-month time counter register RTC_TC_DOM

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name												TC_DOM				
Type												R/W				

TC_DOM The day-of-month initial value for the time counter. The day-of-month maximum value depends on the leap year condition, i.e. 2 LSB of year time counter are zeros.

0x810c_0024 RTC day-of-week time counter register RTC_TC_DOW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														TC_DOW		
Type														R/W		

TC_DOW The day-of-week initial value for the time counter. The range of its value is: 1-7.

0x810c_0028 RTC month time counter register RTC_TC_MTH

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TC_MONTH			
Type													R/W			

TC_MONTH The month initial value for the time counter. The range of its value is: 1-12.

0x810c_002C RTC year time counter register RTC_TC_YEA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										AL_SECOND						
Type										R/W						

TC_YEAR The year initial value for the time counter. The range of its value is: 0-127. (2000-2127)

0x810c_0030 RTC second alarm setting register RTC_AL_SEC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											AL_SECOND					
Type											R/W					

AL_SECOND The second value of the alarm counter setting. The range of its value is: 0-59.

0x810c_0034 RTC minute alarm setting register RTC_AL_MIN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											AL_MINUTE					
Type											R/W					

AL_MINUTE The minute value of the alarm counter setting. The range of its value is: 0-59.

0x810c_0038 RTC hour alarm setting register RTC_AL_HOU

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												AL_HOUR				
Type												R/W				

AL_HOUR The hour value of the alarm counter setting. The range of its value is: 0-23.

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0x810c_003C RTC day-of-month alarm setting register RTC_AL_DOM

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												AL_DOM				
Type												R/W				

AL_DOM The day-of-month value of the alarm counter setting. The day-of-month maximum value depends on the leap year condition, i.e. 2 LSB of year time counter are zeros.

0x810c_0040 RTC day-of-week alarm setting register RTC_AL_DOW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														AL_DOW		
Type														R/W		

AL_DOW The day-of-week value of the alarm counter setting. The range of its value is: 1-7.

0x810c_0044 RTC month alarm setting register RTC_AL_MTH

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													AL_MONTH			
Type													R/W			

AL_MONTH The month value of the alarm counter setting. The range of its value is: 1-12.

0x810c_0048 RTC year alarm setting register RTC_AL_YEA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										AL_YEAR						
Type										R/W						

AL_YEAR The year value of the alarm counter setting. The range of its value is: 0-127. (2000-2127)

0x810c_004C XOSC bias current control register RTC_XOSCCALI

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												XOSCCALI				
Type												WO				

The function is only active when RTC_POWERKEY1 & RTC_POWERKEY2 match the correct values.

XOSCCALI This register controls the XOSC32 bias current.

0x810c_0050 RTC_POWERKEY1 register RTC_POWERKEY1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_POWERKEY1															
Type	R/W															

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0x810c_0054 RTC_POWERKEY2 register RTC_POWERKEY2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_POWERKEY2															
Type	R/W															

These register sets are used to determine if the real time clock has been programmed by software; i.e. the time value in real time clock is correct. When the real time clock is first powered on, the register contents are all undefined, therefore the time values shown are incorrect. Software needs to know if the real time clock has been programmed. Hence, these two registers are defined to solve this power-on issue. After software programs the correct value, these two register sets do not need to be updated. In addition to programming the correct time value, when the contents of these register sets are wrong, the interrupt is not generated. Therefore, the real time clock does not generate the interrupts before the software programs the registers; unwanted interrupt due to wrong time value do not occur. The correct values of these two register sets are:

RTC_POWERKEY1 A357h
RTC_POWERKEY2 67D2h

0x810c_0058 PDN1 RTC_PDN1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_PDN1[7:0]							
Type									R/W							

RTC_PDN1[3:1] is for reset de-bounce mechanism. When RTC_POWERKEY1 & RTC_POWERKEY2 do not match the correct values, RTC_PDN1[3:1] is set to 3 (011 in binary).

- **0** 2ms
- **1** 8ms
- **2** 32ms
- **3** 128ms
- **4** 256ms
- **5** 512ms
- **6** 1024ms
- **7** 2048ms

RTC_PDN1[7:4] & RTC_PDN1[0] is the spare register for software to keep power on and power off state information.

0x810c_005C PDN2 RTC_PDN2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_PDN2[7:0]							
Type									R/W							

RTC_PDN2 The spare register for software to keep power on and power off state information.

0x810c_0064 Spare register for specific purpose RTC_SPAR1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	RTC_SPAR1
Type	R/W

RTC_SPAR1 This register is reserved for specific purpose.

0x810c_0068 Lock / unlock scheme to prevent RTC miswriting RTC_PROT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_PROT															
Type	R/W															

RTC_PROT The RTC write interface is protected by RTC_PROT. Whether the RTC writing interface is enabled or not is decided by RTC_PROT contents. When RTC_POWERKEY1 & RTC_POWERKEY2 are not equal to the correct values, the RTC writing interface is always enabled. But when they match, users have to perform Unlock flow to enable the writing interface.

Unlock flow:
Step1: *RTC_PROT=0x586a;
Step2: *RTC_WRTRG=1;
Step3: while(*RTC_BBPU & 0x40) {}; // Timeout period: 120usec
Step4: *RTC_PROT=0x9136;
Step5: *RTC_WRTRG=1;
Step6: while(*RTC_BBPU & 0x40) {}; // Timeout period: 120usec

Lock flow:
Step1: *RTC_PROT=0x0;
Step2: *RTC_WRTRG=1;
Step3: while(*RTC_BBPU & 0x40) {}; // Timeout period: 120usec

Once the normal RTC content writing is complete, it is suggested to perform Lock flow to turn off the interface to avoid accident writing.

The RTC_PROT contents will be corrupt when reset.

0x810c_006c One-time calibration offset RTC_DIFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RTC_DIFF											
Type					R/W											

The function is only active when RTC_POWERKEY1 & RTC_POWERKEY2 match the correct values.

RTC_DIFF These registers are used to adjust the internal counter of RTC. It effects once and returns to zero in done.

In some cases, you observe the RTC is faster or slower than the standard. To change RTC_TC_SEC is coarse and may cause alarm problem. RTC_DIFF provides a finer time unit. An internal 15-bit counter accumulates in each 32768-HZ clock. Entering a non-zero value into the RTC_DIFF causes the internal RTC counter increases or decreases RTC_DIFF when RTC_DIFF changes to zero again. RTC_DIFF represents as 2's completement form.

For example, if you fill in 0xfff into RTC_DIFF, the internal counter decreases 1 when RTC_DIFF returns to zero. In other words, you can only use RTC_DIFF continuously if RTC_DIFF is equal to zero now.

Note: RTC_DIFF ranges from 0x800 (-2048) to 0x7fd (2045). 0x7ff & 0x7fe are forbid to use.

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0x810c_0070 Repeat calibration offset RTC_CALI

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RTC_CALI						
Type										R/W						

The function is only active when RTC_POWERKEY1 & RTC_POWERKEY2 match the correct values.

RTC_CALI These registers provide a repeat calibration scheme. RTC_CALI provides 7-bit calibration capability in 8-second duration; in other words, 5-bit calibration capability in each second. RTC_CALI represents in 2's complement form, such that you can adjust RTC increasing or decreasing.

Due to RTC_CALI is revealed in 8 seconds, the resolution is less than a 1/32768 clock.
Avg. resolution: 1/32768/8=3.81us
Avg. adjust range: -0.244~0.240ms/sec in 2's complement: -0x40~0x3f (-64~63)

0x810c_0074 Enable the transfers from core to RTC in the queue RTC_WRTGR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WRTGR
Type																WO

WRTGR This register enables the transfers from core to RTC. After you modify all the RTC registers you'd like to change, you must write RTC_WRTGR to 1 to trigger the transfer. The prior writing operations are queued at core power domain. The pending data will not be transferred to RTC domain until WRTGR=1.
After WRTGR=1, the pending data is transferred to RTC domain sequentially in order of register address, from low to high. For example: RTC_BBPU -> RTC_IRQ_EN -> RTC_CII_EN -> RTC_AL_MASK -> RTC_TC_SEC -> etc. The CBUSY in RTC_BBPU is equal to 1 in writing process. You can observe CBUSY to determine when the transmission completes.

4.10 Auxiliary ADC Unit

The auxiliary ADC unit is used to monitor the status of the battery and charger, to identify the plugged peripheral, and to perform temperature measurement. 6 input channels allow diverse applications in this unit.

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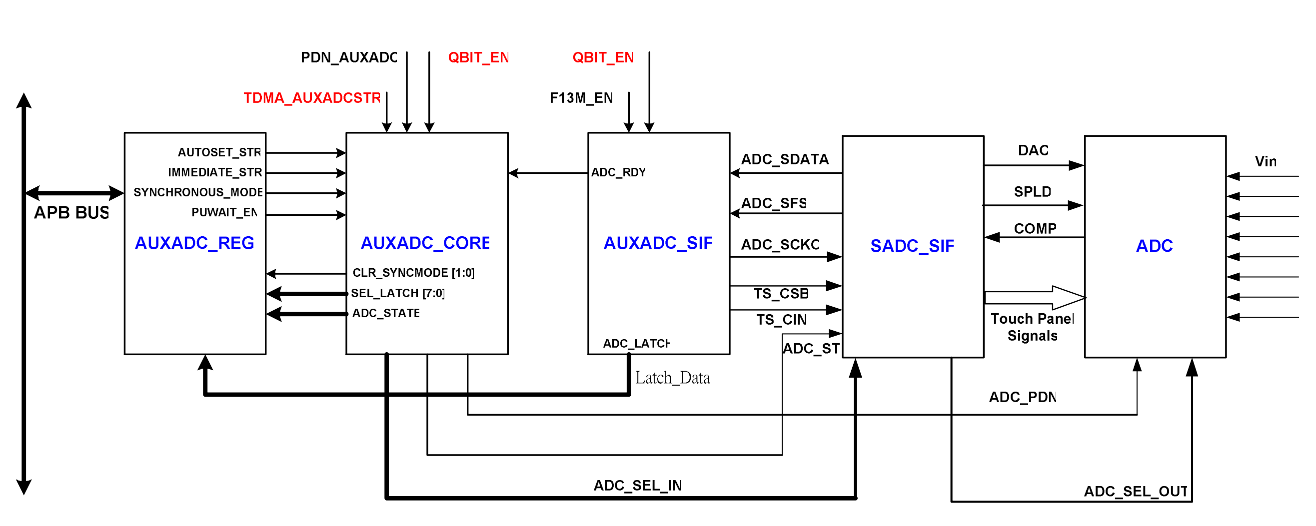

Figure 41 Auxadc Architecture

Each channel can operate in one of two modes: immediate mode and timer-triggered mode. The mode of each channel can be individually selected through register AUXADC_CON0. For example, if the flag SYN0 in the register AUXADC_CON0 is set, the channel 0 is set in timer-triggered mode. Otherwise, the channel operates in immediate mode.

In immediate mode, the A/D converter samples the value once only when the flag in the AUXADC_CON1 register has been set. For example, if the flag IMM0 in AUXADC_CON1 is set, the A/D converter samples the data for channel 0. The IMM flags must be cleared and set again to initialize another sampling.

The value sampled for channel 0 is stored in register AUXADC_DAT0, the value for channel 1 is stored in register AUXADC_DAT1, etc.

If the AUTOSET flag in the register AUXADC_CON3 is set, the auto-sample function is enabled. The A/D converter samples the data for the channel in which the corresponding data register has been read. For example, in the case where the SYN1 flag is not set, the AUTOSET flag is set, when the data register AUXADC_DAT0 has been read, the A/D converter samples the next value for channel 1 immediately.

If multiple channels are selected at the same time, the task is performed sequentially on every selected channel. For example, if AUXADC_CON1 is set to 0x3f, that is, all 6 channels are selected, the state machine in the unit starts sampling from channel 6 to channel 0, and saves the values of each input channel in the respective registers. The same process also applies in timer-triggered mode.

In timer-triggered mode, the A/D converter samples the value for the channels in which the corresponding SYN flags are set when the TDMA timer counts to the value specified in the register TDMA_AUXEV1, which is placed in the TDMA timer. For example, if AUXADC_CON0 is set to 0x3f, all 6 channels are selected to be in timer-triggered mode. The state machine samples all 6 channels sequentially and save the values in registers from AUXADC_DAT0 to AUXADC_DAT5, as it does in immediate mode.

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There is a dedicated timer-triggered scheme for channel 0. This scheme is enabled by setting the SYN11 flag in the register AUXADC_CON2. The timing offset for this event is stored in the register TDMA_AUXEV0 in the TDMA timer. The sampled data triggered by this specific event is stored in the register AUXADC_DAT11. It is used to separate the results of two individual software routines that perform actions on the auxiliary ADC unit.

The AUTOCLR*n* in the register AUXADC_CON3 is set when it is intended to sample only once after setting timer-triggered mode. If AUTOCLR1 flag has been set, after the data for the channels in timer-triggered mode has been stored, the SYN*n* flags in the register AUXADC_CON0 are cleared. If AUTOCLR0 flag has been set, after the data for the channel 0 has been stored in the register AUXADC_DAT11, the SYN11 flag in the register AUXADC_CON2 is cleared.

The usage of the immediate mode and timer-triggered mode are mutually exclusive in terms of individual channels.

The PUWAIT_EN bit in the registers AUXADC_CON3 is used to power up the analog port in advance. This ensures that the power has ramped up to the stable state before A/D converter starts the conversion. The analog part is automatically powered down after the conversion is completed.

There are only four external pins (channel 3~5) for voltage detection. The other channels (0~2) are for battery voltage, battery current, and charger, respectively.

Touch Panel:

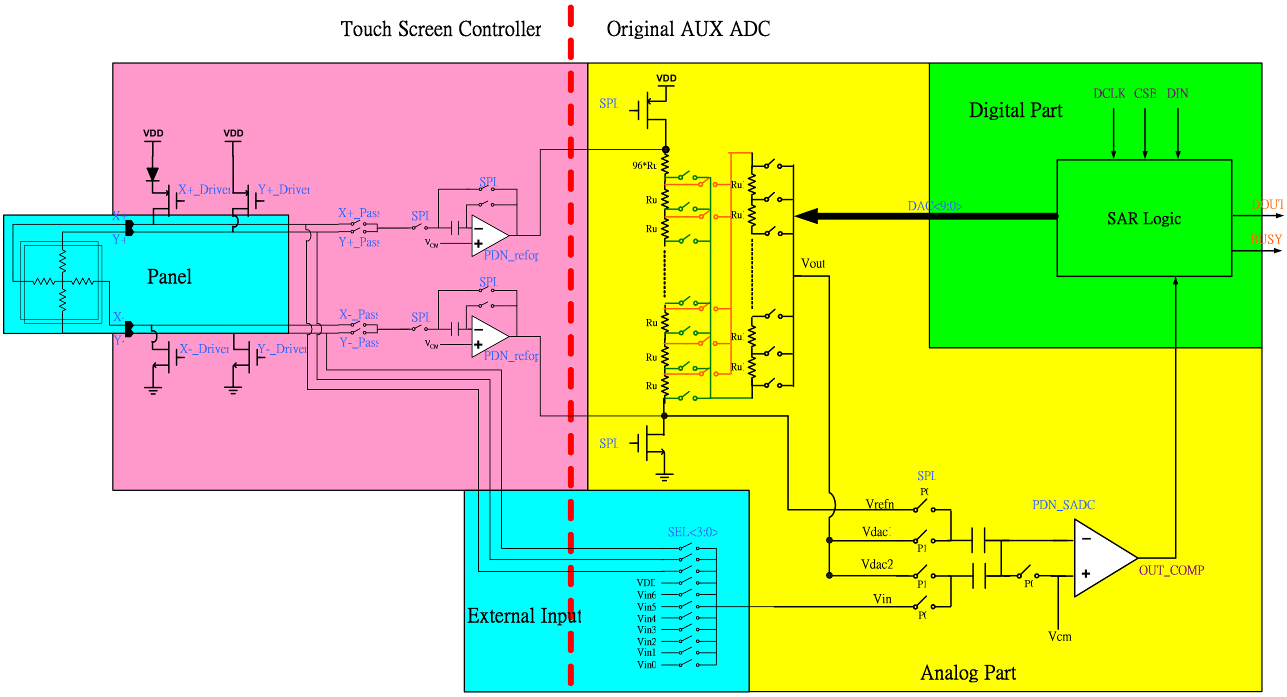

Figure 42 Touch Panel Circuit Structure

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Besides the normal sampling of external input voltage, auxadc includes the sampling of the touch panel function. For the specified axis, SW should program **AUX_TS_CMD** first, and then trigger touch panel's sample in the register **AUX_TS_CON**. The touch panel sampling waveform is shown as follows. After SW polls status bit in the register **AUXADC_CON3** to know that the touch panel sample is finished. SW can read back the specified axis value from the register **AUX_TS_DAT0**.

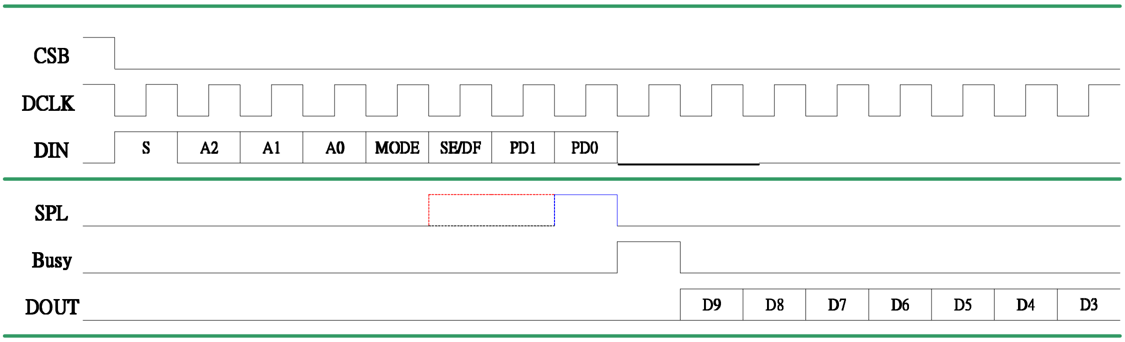

Figure 43 Touch Panel Sampling Waveform

S: Start bit

A2~A0: Addressing bits

Mode: 10bit or 8bit

SE/DF: Single End or Differential mode

PD1~0: Power Down Command

These values are defined in the register **AUX_TS_CMD**. In the following table, it shows the relationship between AUX_TS_CMD and touch panel control signals.

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SE/DFB	A2	A1	A0	X/Y Driver	X/Y Pass	SEL< 3:0 >	NOTE
0	0	0	0	ALL OFF	ALL OFF		TBD
0	0	0	1	X+ / X- off Y+ / Y- on	X+ / X- off Y+ / Y- on	1000	Y Position
0	0	1	0	ALL OFF	ALL OFF	0011	IN3
0	0	1	1	X+ / Y- off Y+ / X- on	X+ / Y- off Y+ / X- on	1000	Z_1 Position
0	1	0	0	X+ / Y- off Y+ / X- on	X+ / Y- off Y+ / X- on	1010	Z_2 Position
0	1	0	1	X+ / X- on Y+ / Y- off	X+ / X- on Y+ / Y- off	1001	X Position
0	1	1	0	ALL OFF	ALL OFF	0100	IN4
0	1	1	1	ALL OFF	ALL OFF		TBD
1	0	0	0	ALL OFF	ALL OFF		TBD
1	0	0	1	X+ / X- off Y+ / Y- on	ALL OFF	1000	Y Position
1	0	1	0	ALL OFF	ALL OFF	0011	IN3
1	0	1	1	X+ / Y- off Y+ / X- on	ALL OFF	1000	Z_1 Position
1	1	0	0	X+ / Y- off Y+ / X- on	ALL OFF	1010	Z_2 Position
1	1	0	1	X+ / X- on Y+ / Y- off	ALL OFF	1001	X Position
1	1	1	0	ALL OFF	ALL OFF	0100	IN4
1	1	1	1	ALL OFF	ALL OFF		TBD

Table 34 Relationship between commands and touch panel control signals

4.10.1 Register Definitions

Register Address	Register Function	Acronym
0x8205_0000	Auxiliary ADC control register 0	AUXADC_CON0
0x8205_0004	Auxiliary ADC control register 1	AUXADC_CON1
0x8205_0008	Auxiliary ADC control register 2	AUXADC_CON2
0x8205_0010	Auxiliary ADC channel 0 data register (VBAT)	AUXADC_DAT0
0x8205_0014	Auxiliary ADC channel 1 data register (ISENSE)	AUXADC_DAT1
0x8205_0018	Auxiliary ADC channel 2 data register (CHRIN)	AUXADC_DAT2
0x8205_001C	Auxiliary ADC channel 3 data register (External)	AUXADC_DAT3
0x8205_0020	Auxiliary ADC channel 4 data register (External)	AUXADC_DAT4
0x8205_0024	Auxiliary ADC channel 5 data register (External)	AUXADC_DAT5
0x8205_003C	Auxiliary ADC channel 0 data register for TDMA event 0	AUXADC_DAT11
0x8205_0050	Touch Screen Debounce Time	AUX_TS_DEBT
0x8205_0054	Touch Screen Sample Command	AUX_TS_CMD
0x8205_0058	Touch Screen Control	AUX_TS_CON

Table 35 Auxadc Registers

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0x8205_0000 Auxiliary ADC control register 0 AUXADC_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											SYN5	SYN4	SYN3	SYN2	SYN1	SYN0
Type											R/W	R/W	R/W	R/W	R/W	R/W
Reset											0	0	0	0	0	0

SYN*n* These 7 bits define whether the corresponding channel is sampled or not in timer-triggered mode. It is associated with timing offset register TDMA_AUXEV1. It supports multiple flags. The flags can be automatically cleared after those channel have been sampled if AUTOCLR1 in the register AUXADC_CON3 is set.

0 The channel is not selected.

1 The channel is selected.

0x8205_0004 Auxiliary ADC control register 1 AUXADC_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											IMM5	IMM4	IMM3	IMM2	IMM1	IMM0
Type											R/W	R/W	R/W	R/W	R/W	R/W
Reset											0	0	0	0	0	0

IMM*n* These 7 bits are set individually to sample the data for the corresponding channel. It supports multiple flags.

0 The channel is not selected.

1 The channel is selected.

0x8205_0008 Auxiliary ADC control register 2 AUXADC_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SYN11
Type																R/W
Reset																0

SYN11 This bit is used only for channel 0 and is to be associated with timing offset register TDMA_AUXEV0 in the TDMA timer in timer-triggered mode. The flag can be automatically cleared after channel 0 has been sampled if AUTOCLR0 in the register AUXADC_CON3 is set.

0 The channel is not selected.

1 The channel is selected.

0x8205_000C Auxiliary ADC control register 3 AUXADC_CON3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOSET				PUWAIT_EN		AUTOCLR1	AUTOCLR0	SOFT_RST							STA
Type	R/W				R/W		R/W	R/W	R/W							RO
Reset	0				0		0	0	0							0

AUTOSET This field defines the auto-sample mode of the module. In auto-sample mode, each channel with its sample register being read can start sampling immediately without configuring the control register AUXADC_CON1 again.

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PUWAIT_EN Thus field enables the power warm-up period to ensure power stability before the SAR process takes place. It is recommended to activate this field.

- **0** The mode is not enabled.
- **1** The mode is enabled.

SOFT_RST Software Reset AUXADC state machine

- **0** Normal function
- **1** Reset AUXADC state machine

AUTOCLR1 The field defines the auto-clear mode of the module for event 1. In auto-clear mode, each timer-triggered channel gets samples of the specified channels once the SYN*n* bit in the register AUXADC_CON0 has been set. The SYN*n* bits are automatically cleared and the channel is not enabled again by the timer event except when the SYN*n* flags are set again.

- **0** The automatic clear mode is not enabled.
- **1** The automatic clear mode is enabled.

AUTOCLR0 The field defines the auto-clear mode of the module for event 0. In auto-clear mode, the timer-triggered channel 0 gets the sample once the SYN11 bit in the register AUXADC_CON2 has been set. The SYN11 bit is automatically cleared and the channel is not enabled again by the timer event 0 except when the SYN11 flag is set again.

- **0** The automatic clear mode is not enabled.
- **1** The automatic clear mode is enabled.

STA The field defines the state of the module.

- **0** This module is idle.
- **1** This module is busy.

0x8205_0010 Auxiliary ADC channel 0 register AUXADC_DAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							DAT									
Type							RO									
Reset							0									

The register stores the sampled data for the channel 0. There are 8 registers of the same type for the corresponding channel . The overall register definition is listed in **Table 36**.

Register Address	Register Function	Acronym
0x8205_0010	Auxiliary ADC channel 0 data register	AUXADC_DAT0
0x8205_0014	Auxiliary ADC channel 1 data register	AUXADC_DAT1
0x8205_0018	Auxiliary ADC channel 2 data register	AUXADC_DAT2
0x8205_001C	Auxiliary ADC channel 3 data register	AUXADC_DAT3
0x8205_0020	Auxiliary ADC channel 4 data register	AUXADC_DAT4
0x8205_0024	Auxiliary ADC channel 5 data register	AUXADC_DAT5
0x8205_003C	Auxiliary ADC channel 0 data register for TDMA event 0	AUXADC_DAT11

Table 36 Auxiliary ADC data register list

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0x8205_0050 Touch Screen Debounce Time AUX_TS_DEBT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEBOUNCE TIME													
Type			R/W													
Reset			0													

DEBOUNCE TIME While the analog touch screen irq signal is from high to low level, auxadc will issue an interrupt after the debounce time.

0x8205_0054 Touch Screen Sample Command AUX_TS_CMD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										ADDRESS			MODE	SE/DF	PD	
Type										R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset										0	0	0	0	0	0	0

ADDRESS Define which x or y or z data will be sampled.

- **001** Y Position
- **011** Z1 Position
- **100** Z2 Position
- **101** X Position
- **Others** Reserved

MODE Select the sample resolution

- **0** 10-bit resolution
- **1** 8-bit resolution

SE/DF Mode selection

- **0** Differential mode
- **1** Single-end mode

PD Power down control for analog IRQ signal and touch screen sample control signal

- **00** Turn on Y-_drive signal and PDN_sh_ref
- **01** Turn on PDN_IRQ and PDN_sh_ref
- **10** Reserved
- **11** Turn on PDN_IRQ

0x8205_0058 Touch Screen Control AUX_TS_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															ST	SPL
Type															R	R/W
Reset															0	0

SPL Touch Screen Sample Trigger

- **0** No Action
- **1** While SW writes 1'b1, auxadc will trigger the touch screen process. After the sample process of touch screen finishes, this bit will be disserted.

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ST Touch Screen Status

- **0** Touch Screen is idle.
- **1** Touch Screen is touched.

0x8205_005C Touch Screen Sample DATA AUX_TS_DAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							DAT									
Type							RO									
Reset							0									

This register stores the touch screen sample data.

4.11 I2C / SCCB Controller

4.11.1 General Description

I2C (Inter-IC) /SCCB (Serial Camera Control Bus) is a two-wire serial interface. The two signals are SCL and SDA. SCL is a clock signal that is driven by the master. SDA is a bi-directional data signal that can be driven by either the master or the slave. This generic controller supports the master role and conforms to the I2C specification.

4.11.1.1 Feature Support

I2C compliant master mode operation

Adjustable clock speed for LS/FS mode operation.

7bit/10 bit addressing support.

High Speed mode support.

Slave Clock Extension support.

START/STOP/REPEATED START condition

Manual/DMA Transfer Mode

Multi write per transfer (up to 8 data bytes for non dma mode and 255 data bytes for dma mode)

Multi read per transfer (up to 8 data bytes for non dma mode and 255 data bytes for dma mode)

Multi transfer per transaction (up to 256 write transfers or 256 read transfers with dma mode)

DMA mode with Fifo Flow Control and bus signal holding

Combined format transfer with length change capability.

Active drive / wired-and I/O configuration

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4.11.1.2 Manual/DMA Transfer Mode

The controller offers 2 types of transfer mode, Manual and DMA.

When Manual mode is selected, in addition to the slave address register, the controller has a built-in 8byte deep FIFO which allows mcu to prepare up to 8 bytes of data for a write transfer, or read up to 8 bytes of data for a read transfer.

When DMA mode is enabled, the data to and from the FIFO is controlled via DMA transfer and can therefore support up to 255 bytes of consecutive read or write, with the data read from or write to another memory space. When DMA mode is enabled, flow control mechanism is also implemented to hold the bus clk when FIFO underflow or overflow condition is encountered.

4.11.1.3 Transfer format support

This controller has been designed to be as generic as possible in order to support a wide range of devices that may utilize different combinations of transfer formats. Here are the transfer format types that can be supported through different software configuration:

(Wording convention note:

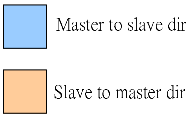
transfer = anything encapsulated within a Start and Stop or Repeated Start.

transfer length = the number of bytes within the transfer.

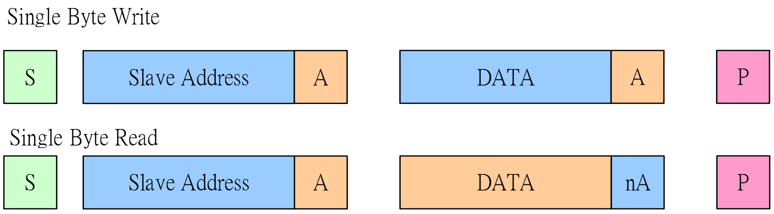
transaction = this is the top unit. Everything combined equals 1 transaction.

Transaction length = the number of transfers to be conducted.

)



Single Byte Access



Multi Byte Access

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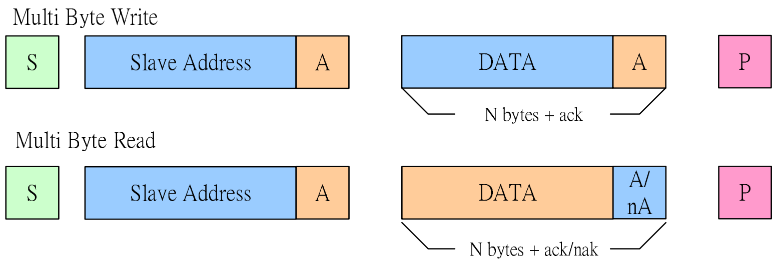
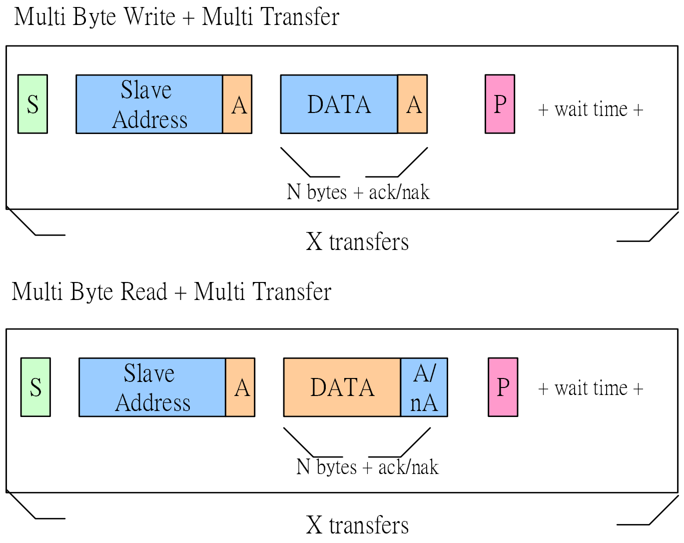
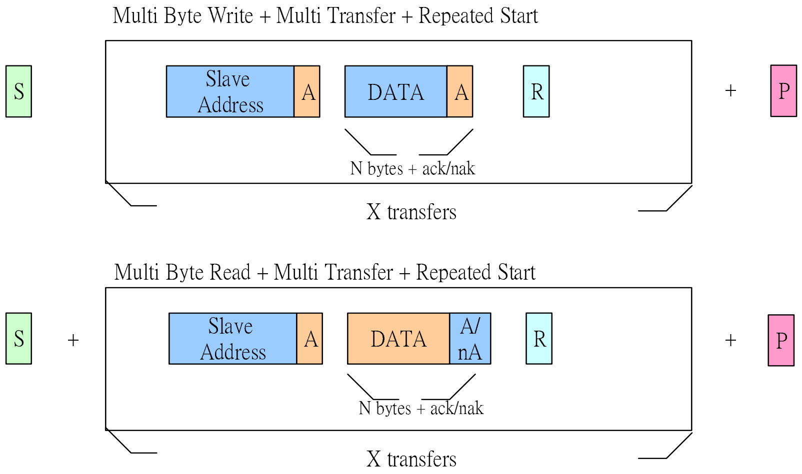


Multi Byte Transfer + Multi Transfer (same direction)



Multi Byte Transfer + Multi Transfer w RS (same direction)



Combined Write/Read with Repeated Start (direction change)

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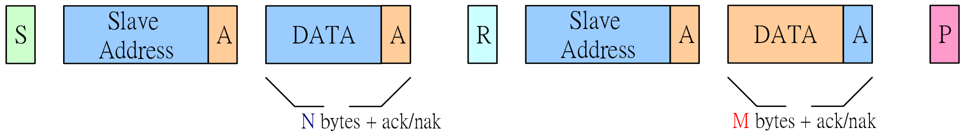
(Note: Only supports Write and then Read sequence. Read and then Write is not supported)

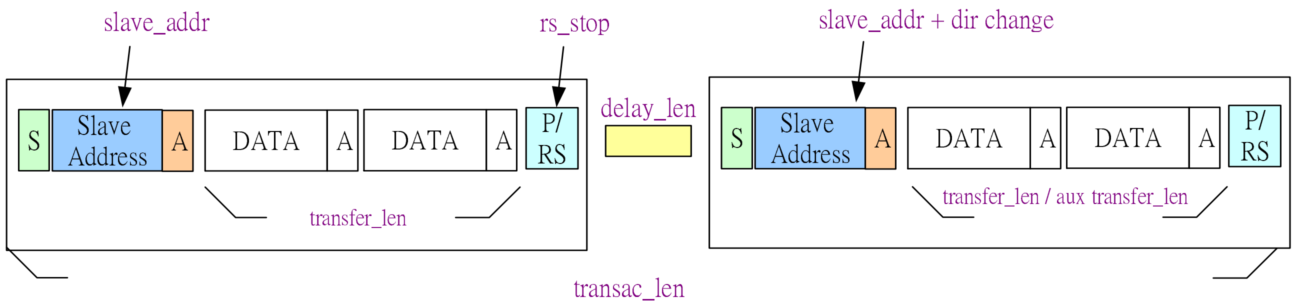
Combined Multi Byte Write + Multi Byte Read



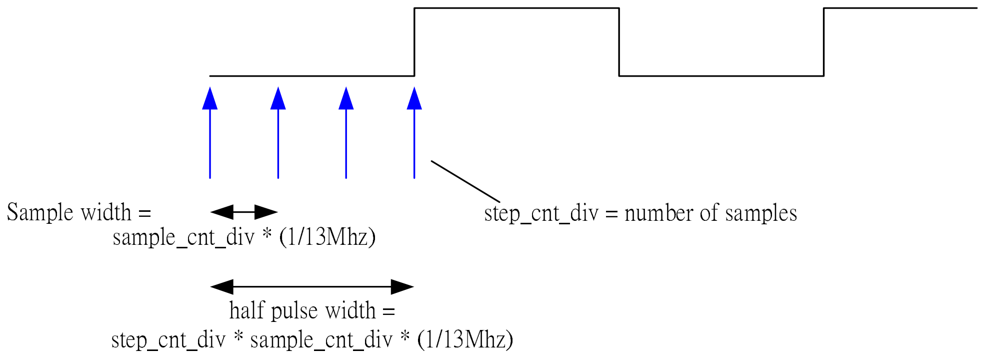
4.11.2 Programming Examples

Common Transfer Programmable Parameters

Programmable Parameters



Output Waveform Timing Programmable Parameters



4.11.3 Register Definitions

0x8110_0000 Data Port Register DATA_PORT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFO DATA							
Type									R/W							
Reset									0							

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DATA_PORT[7:0] This is the FIFO access port. During master write sequences (slave_addr[0] = 0), this port can be written by APB, and during master read sequences (slave_addr[0] = 1), this port can be read by APB.

(NOTE) Slave_addr must be set correctly before accessing the fifo.

(DEBUG ONLY) If the fifo_apb_debug bit is set, then the FIFO can be read and write by the APB

0x8110_0004 Slave Address Register SLAVE_ADDR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SLAVE_ADDR							
Type									R/W							
Reset									0							

SLAVE_ADDR [7:0] This specifies the slave address of the device to be accessed. Bit 0 is defined by the I2C protocol as a bit that indicates the direction of transfer. 1 = master read, 0 = master write.

0x8110_0008 Interrupt Mask Register INTR_MASK

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DEBUG	HS_NACKER	ACKERR	TRANSAC_COMP
Type													R.W	R/W	R/W	R/W
Reset													1	1	1	1

This register provides masks for the corresponding interrupt sources as indicated in intr_stat register.

1 = allow interrupt

0 = disable interrupt

Note: while disabled, the corresponding interrupt will not be asserted, however the intr_stat will still be updated with the status. Ie. mask does not affect intr_stat register values.

0x8110_000C Interrupt Status Register INTR_STAT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														HS_NACKERR	ACKERR	TRANSAC_COMP
Type														W1C	W1C	W1C
Reset														0	0	0

When an interrupt is issued by i2c controller, this register will need to be read by mcu to determine the cause for the interrupt. After this status has been read and appropriate actions are taken, the corresponding interrupt source will need to be write 1 cleared.

HS_NACKERR This status is asserted if hs master code nack error detection is enabled. If enabled, hs master code nack err will cause transaction to end and stop will be issued.

ACKERR This status is asserted if ACK error detection is enabled. If enabled, ackerr will cause transaction to end and stop will be issued.

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TRANSAC_COMP This status is asserted when a transaction has completed successfully.

0x8110_0010 Control Register CONTROL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										TRANSFER_LEN_CHANGE	ACKERR_DET_EN	DIR_CHANGE	CLK_EXT_EN	DMA_EN	RS_STOP	
Type										R/W	R/W	RW	RW	RW	RW	R/W
Reset										0	0	0	0	0	0	0

TRANSFER_LEN_CHANGE This options specifies whether or not to change the transfer length after the fist transfer completes. If enabled, the transfers after the first transfer will use the transfer_len_aux parameter.

ACKERR_DET_EN This option enables slave ack error detection. When enabled, if slave ack error is detected, the master shall terminate the transaction by issuing a STOP condition and then asserts ackerr interrupt. Mcu shall handle this case appropriately and then resets the fifo address before reissuing transaction again. If this option is disabled, the controller will ignore slave ack error and keep on scheduled transaction.

0 disable
1 enable

DIR_CHANGE This option is used for combined transfer format, where the direction of transfer is to be changed from write to read after the FIRST RS condition. Note: when set to 1, the transfers after the direction change will be based on the transfer_len_aux parameter.

0 disable
1 enable

CLK_EXT_EN I2C spec allows slaves to hold the SCL line low if it is not yet ready for further processing. Therefore, if this bit is set to 1, master controller will enter a high wait state until the slave releases the SCL line.

DMA_EN By default, this is disabled, and fifo data shall be manually prepared by mcu. This default setting should be used for transfer sizes of less than 8 data bytes and no multiple transfer is configured. When enabled, dma requests are turned on, and the fifo data should be prepared in memory.

RS_STOP In LS/FS mode, this bit affects multi-transfer transaction only. It controls whether or not REPEATED-START condition is used between transfers. The last ending transfer always ends with a STOP.

In HS mode, this bit must be set to 1.

0 use STOP

1 use REPEATED-START

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0x8110_0014 Transfer Length Register (Number of Bytesper Transfer) TRANSFER_LEN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**TRANSFER_LEN_AUX**					**TRANSFER_LEN**							
Type				R/W												R/W
Reset				'h1												'h1

TRANSFER_LEN_AUX[4:0] This field is valid only when dir_change is set to 1. This indicates the number of DATA BYTES to be transferred in 1 transfer unit (excluding slave address byte) for the transfers following the direction change. I.e., if dir_change =1, then the first write transfer length depends on transfer_len, while the second read transfer length depend on transfer_len_aux. Dir change is always after the first transfer.

(NOTE) The value must be set greater than 1, otherwise no transfer will take place.

TRANSFER_LEN[7:0] This indicates the number of DATA BYTES to be transferred in 1 transfer unit (excluding slave address byte)

(NOTE) The value must be set greater than 1, otherwise no transfer will take place.

0x8110_0018 Transaction Length Register (Number of Transfers per Transaction) TRANSAC_LEN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**TRANSAC_LEN**							
Type																R/W
Reset																'h1

TRANSAC_LEN[7:0] This indicates the number of TRANSFERS to be transferred in 1 transaction

(NOTE) The value must be set greater than 1, otherwise no transfer will take place.

0x8110_001C Inter Delay Length Register DELAY_LEN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**DELAY_LEN**							
Type									R/W							
Reset									'h2							

DELAY_LEN[3:0] This sets the wait delay between consecutive transfers when RS_STOP bit is set to 0. (the unit is same as the half pulse width)

0x8110_0020 Timing Control Register TIMING

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DATA READ ADJ**	**DATA_READ_TIME**				**SAMPLE_CNT_DIV**					**STEP_CNT_DIV**					
Type	R/W	R/W				R/W					R/W					
Reset	'h0	'h1				'h3					'h3					

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LS/FS only. This register is used to control the output waveform timing. Each half pulse width (ie. each high or low pulse) is equal to = step_cnt_div * (sample_cnt_div * 1/13Mhz)

SAMPLE_CNT_DIV[2:0] Used for LS/FS only. This adjusts the width of each sample. (sample width = sample_cnt_div * 1/13Mhz)

STEP_CNT_DIV[5:0] This specifies the number of samples per half pulse width (ie. each high or low pulse)

DATA_READ_ADJ When set to 1, data latch in sampling time during master reads are adjusted according to DATA_READ_TIME value. Otherwise, by default, data is latched in at half of the high pulse width point. This value must be set to less or equal to half the high pulse width.

DATA_READ_TIME[2:0] This value is valid only when DATA_READ_ADJ is set to 1. This can be used to adjust so that data is latched in at earlier sampling points (assuming data is settled by then)

0x8110_0024 Start Register START

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																START
Type																R/W
Reset																0

START This register starts the transaction on the bus. It is auto deasserted at the end of the transaction.

0x8110_0030 Fifo Status Register FIFO_STAT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RD_ADDR				WR_ADDR				FIFO_OFFSET						WR_FULL	RD_EMPTY
Type	RO				RO				RO						RO	RO
Reset	0				0				0				0	0	0	0

RD_ADDR[3:0] The current rd address pointer. (only bit [2:0] has physical meaning)

WR_ADDR[3:0] The current wr address pointer. (only bit [2:0] has physical meaning)

FIFO_OFFSET[3:0] wr_addr[3:0] – rd_addr[3:0]

WR_FULL This indicates that the fifo is full.

RD_EMPTY This indicates that the fifo is empty.

0x8110_0034 Fifo Thresh Register FIFO_THRESH

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						TX_TRIG_THRESH								RX_TRIG_THRESH		
Type						RW								R/W		
Reset						‘h7								‘h0		

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DEBUG ONLY. By default, these values do not need to be adjusted. Note! for RX, no timeout mechanism is implemented. Therefore, RX_trig_thresh must be left at 0, or there would be data left in the fifo that is not fetched by DMA controller.

TX_TRIG_THRESH[2:0] When tx fifo level is below this value, tx dma request is asserted.

RX_TRIG_THRESH[2:0] When rx fifo level is above this value, rx dma request is asserted.

0x8110_0038 Fifo Address Clear Register FIFO_ADDR_CLR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FIFO_ADDR_CR
Type																WO
Reset																0

FIFO_ADDR_CLR When written with a 1'b1, a 1 pulse fifo_addr_clr is generated to clear the fifo address to back to 0.

0x8110_0040 IO Config Register IO_CONFIG

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														IO SYNC EN	SDA_IO_CONFIG	SCL_IO_CONFIG
Type														R/W	R/W	R/W
Reset														0	0	0

This register is used to configure the I/O for the sda and scl lines to select between normal i/o mode, or open-drain mode to support wired-and bus.

IO_SYNC_EN DEBUG ONLY: When set to 1, scl and sda inputs will be first dual synced by bclk_ck. This should not be needed. Only reserved for debugging.

SDA_IO_CONFIG
- 0 normal tristate io mode
- 1 open-drain mode

SCL_IO_CONFIG
- 0 normal tristate io mode
- 1 open-drain mode

0x8110_0044 RESERVED DEBUG Register DEBUG

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type														R/W	R/W	R/W
Reset														0	0	0

NOTE: This register is for DEBUG ONLY. The bits are R/W, do not change the values from the default value.

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0x8110_0048 High Speed Mode Register HS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		HS_SAMPLE_CNT DIV				HS_STEP_CNT_DIV				MASTER_CODE					HS_NACKERR_DET_EN	HS_EN
Type		R/W				R/W				R/W					R/W	R/W
Reset		0				1				0					1	0

This register contains options for supporting high speed operation features

Each HS half pulse width (ie. each high or low pulse) is equal to = step_cnt_div * (sample_cnt_div * 1/13Mhz)

HS_SAMPLE_CNT_DIV[2:0] When high speed mode is entered after the master code transfer has been completed, the sample width becomes dependent on this parameter.

HS_STEP_CNT_DIV[2:0] When high speed mode is entered after the master code transfer has been completed, the number of samples per half pulse width becomes dependent on this value.

MASTER_CODE[2:0] This is the 3 bit programmable value for the master code to be transmitted.

HS_NACKERR_DET_EN This enables NACKERR detection during the master code transmission. When enabled, if NACK is not received after master code has been transmitted, the transaction will terminated with a STOP condition.

HS_EN This enables the high speed transaction. (note: rs_stop must be set to 1 as well)

0x8110_0050 Soft Reset Register SOFTRESET

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SOFT_RESET
Type																WO
Reset																0

SOFT_RESET When written with a 1'b1, a 1 pulse soft reset is used as synchronous reset to reset the I2C internal hardware circuits.

0x8110_0064 Debug Status Register DEBUGSTAT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUS_BUSY	MASTER_WRITE	MASTER_READ	MASTER_STATE			
Type										RO	RO	RO	RO			
Reset										0	1	0	0			

BUS_BUSY DEBUG ONLY: valid when bus_detect_en is 1. bus_busy = 1 indicates a start transaction has been detected and no stop condition has been detected yet.

MASTER_WRITE DEBUG ONLY: 1 = current transfer is in the master write dir

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MASTER_READ DEBUG ONLY: 1 = current transfer is in the master read dir

MASTER_STATE[3:0] DEBUG ONLY: reads back the current master_state.

0x8110_0068 Debug Control Register DEBUGCTRL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															APB_DEBUG_RD	FIFO_APB_DEBUG
Type															WO	R/W
Reset															0	0

APB_DEBUG_RD This bit is only valid when fifo_apb_debug is set to 1. Writing to this register will generate a 1 pulsed fifo apb rd signal for reading the fifo data.

FIFO_APB_DEBUG This is used for trace32 debug purposes. When using trace32, and the memory map is shown, turning this bit on will block the normal apb read access. Apb read access to the fifo is then enabled by writing to apb_debug_rd.

0 disable
1 enable

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5 Microcontroller Coprocessors

Microcontroller Coprocessors are designed to run computing-intensive processes in place of the Microcontroller (MCU). These coprocessors especially target timing critical GSM/GPRS Modem processes that require fast response and large data movement. Controls to the coprocessors are all through memory access via the APB.

5.1 Divider

To ease the processing load of MCU, a divider is employed here. The divider can operate signed and unsigned 32bit/32bit division, as well as modulus. The processing time of the divider is from 1 clock cycle to 33 clock cycles, which depends upon the magnitude of the value of the dividend. The detailed processing time is listed below in **Table 37**. From the table we can see that there are two kind of processing time (except for when the dividend is zero) in an item. Which kind depends on whether there is the need for restoration at the last step of the division operation.

After the divider is started by setting START to "1" in Divider Control Register, DIV_RDY will go low, and it will be asserted after the division process is finished. MCU could detect this status bit by polling it to know the correct access timing. In order to simplify polling, only the value of register DIV_RDY will appear while Divider Control Register is read. Hence, MCU does not need to mask other bits to extract the value of DIV_RDY.

In GSM/GPRS system, many divisions are executed with some constant divisors. Therefore, some often-used constants are stored in the divider to speed up the process. By controlling control bits IS_CNST and CNST_IDX in Divider Control register, one can start a division without giving a divisor. This could save the time for writing divisor in and the instruction fetch time, and thus make the process more efficient.

Signed Division		Unsigned Division	
Dividend	**Clock Cycles**	**Dividend**	**Clock Cycles**
0000_0000h	1	0000_0000h	1
0000_00ffh – (-0000_0100h), excluding 0x0000_0000	8 or 9	0000_0001h – 0000_00ffh	8 or 9
0000_ffffh – (-0001_0000h)	16 or 17	0000_0100h – 0000_ffffh	16 or 17
00ff_ffffh – (-0100_0000h)	24 or 25	0001_0000h – 00ff_ffffh	24 or 25
7fff_ffffh – (-8000_0000h)	32 or 33	0100_0000h – ffff_ffffh	32 or 33

Table 37 Processing time in different value of dividend.

5.1.1 Register Definitions

Register Address	Register Function	Acronym
0x8206_0000	Divider Control Register	DIV_CON
0x8206_0004	Divider Dividend register	DIV_DIVIDEND

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0x8206_0008	Divider Divisor register	DIV_DIVISOR
0x8206_000C	Divider Quotient register	DIV_QUOTIENT
0x8206_0010	Divider Remainder register	DIV_REMAINDER

Table 38 All Registers Table

0x8206_0000 Divider Control Register DIV_CON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														CNST_IDX		
Type														WO		
Reset														0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											IN_CNST	SIGN			DIV_RDY	START
Type											WO	WO			RO	WO
Reset											0	1			1	0

START To start division. It will return to 0 after division has started.

- **0** Reserved
- **1** Start division

DIV_RDY Current status of divider. Note that when DIV_CON register is read, only the value of DIV_RDY will appear. That means program does not need to mask other part of the register to extract the information of DIV_RDY.

- **0** division is in progress.
- **1** division is finished.

SIGN To indicate signed or unsigned division.

- **0** Unsigned division.
- **1** Signed division.

IS_CNST To indicate if internal constant value should be used as a divisor. If IS_CNST is enabled, User does not need to write the value of the divisor, and divider will automatically use the internal constant value instead. What value divider will use depends on the value of CNST_IDX.

- **0** Normal division. Divisor is written in via APB
- **1** Using internal constant divisor instead.

CNST_IDX Index of constant divisor.

- **0** divisor = 13
- **1** divisor = 26
- **2** divisor = 51
- **3** divisor = 52
- **4** divisor = 102
- **5** divisor = 104

0x8206_0004 Divider Dividend register DIV_DIVIDEND

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	DIVIDEND[31:16]															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIVIDEND[15:0]															
Type	WO															
Reset	0															

DIVIDEND Dividend

0x8206_0008 Divider Divisor register DIV_DIVISOR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIVISOR[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIVISOR[15:0]															
Type	R/W															
Reset	0															

Divisor Divisor

0x8206_000C Divider Quotient register DIV_QUOTIENT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QUOTIENT[31:16]															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QUOTIENT[15:0]															
Type	RO															
Reset	0															

QUOTIENT Quotient

0x8206_0010 Divider Remainder register DIV_REMAINDER

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REMAINDER[31:16]															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REMAINDER[15:0]															
Type	RO															
Reset	0															

REMAINDER Remainder

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5.2 CSD Accelerator

5.2.1 General Description

This unit performs the data format conversion of RA0, RA1, and FAX in CSD service. CSD service consists of two major functions: data flow throttling and data format conversion. The data format conversion is a bit-wise operation and takes a number of instructions to complete a conversion. Therefore, it is not efficient to do by MCU itself. A coprocessor, CSD accelerator, is designed here to reduce the computing power needed to perform this function.

CSD accelerator only helps in converting data format; the data flow throttling function is still implemented by the MCU. CSD accelerator performs three types of data format conversion, RA0, RA1, and FAX.

For RA0 conversion, only uplink RA0 data format conversion is provided here. This is because there are too many judgments on the downlink path conversion, which will greatly increase area cost. Uplink RA0 conversion is to insert one start bit and one stop bit before and after a byte, respectively, during 16 bytes. **Figure 44** illustrates the detailed conversion table.

RA0 converter can only process RA0 data state by state. Before filling in new data, software must make sure the converted data of certain state is withdrawn, or the converted data will be replaced by the new data. For example, if 32-bit data is written, and the state pointer goes from state 0 to state 1, and word ready of state 0 is asserted; then, before writing the next 32-bit data, the word of state 0 should be withdrawn first, or the data will be lost.

RA0 records the number of written bytes, state pointer, and ready state word. The information can help software to perform flow control. See Register Definition for more detail.

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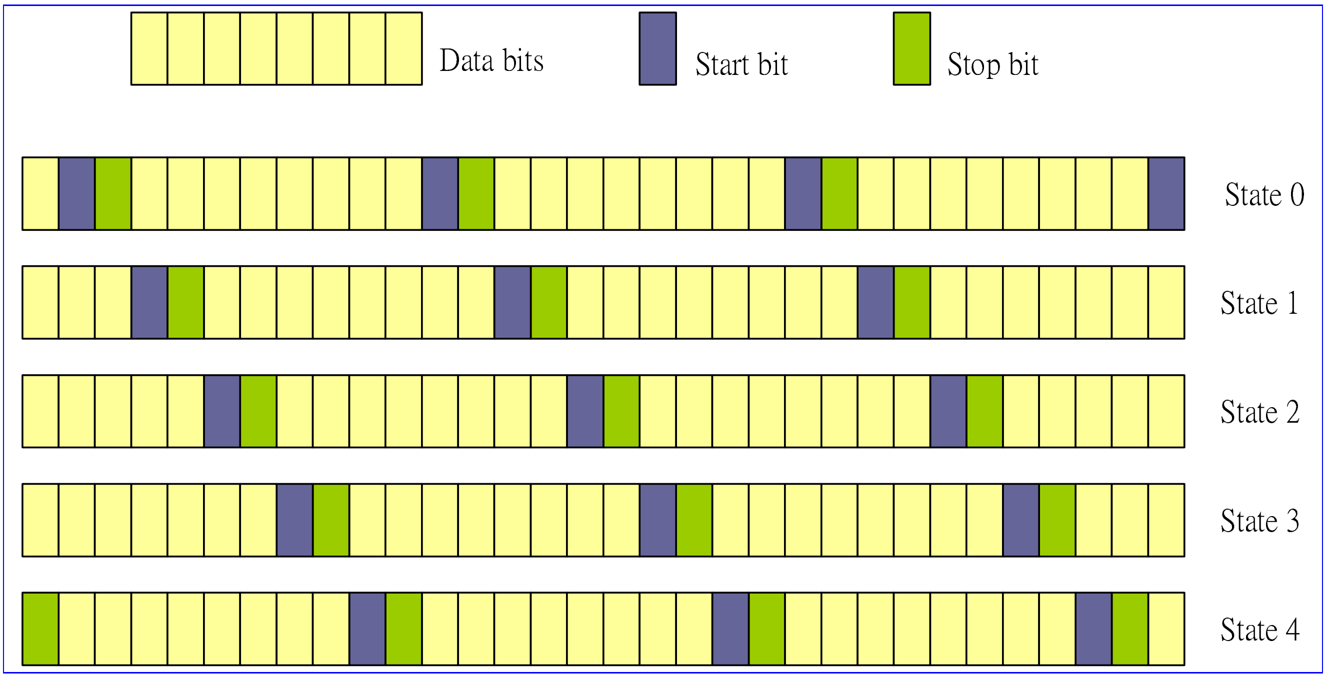

Figure 44 data format conversion of RA0

For RA1 conversion, both directions, downlink and uplink, are supported. The data formats vary in different data rate. The detailed conversion table is shown in **Figure 45** and **Figure 46**. The yellow part is the payload data, and the blue part is the status bit.

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Bit 0 → Bit 6

D1	D2	D3	D4	D5	D6	S1
D7	D8	D9	D10	D11	D12	X
D13	D14	D15	D16	D17	D18	S3
D19	D20	D21	D22	D23	D24	S4
E4	E5	E6	E7	D25	D26	D27
D28	D29	D30	S6	D31	D32	D33
D34	D35	D36	X	D37	D38	D39
D40	D41	D42	S8	D43	D44	D45
D46	D47	D48	S9			

Bit 59

Figure 45 data format conversion for 6k/12k RA1

Bit 0 → Bit 7

D1	D2	D3	S1	D4	D5	D6	X
D7	D8	D9	S3	D10	D11	D12	S4
E4	E5	E6	E7	D13	D14	D15	S6
D16	D17	D18	X	D19	D20	D21	S8
D22	D23	D24	S9				

Bit 35

Figure 46 data format conversion for 3.6k RA1

For FAX, two types of bit-reversal functions are provided. One is bit-wise reversal, and the other is byte-wise reversal, which are illustrated in **Figure 47** and **Figure 48**, respectively.

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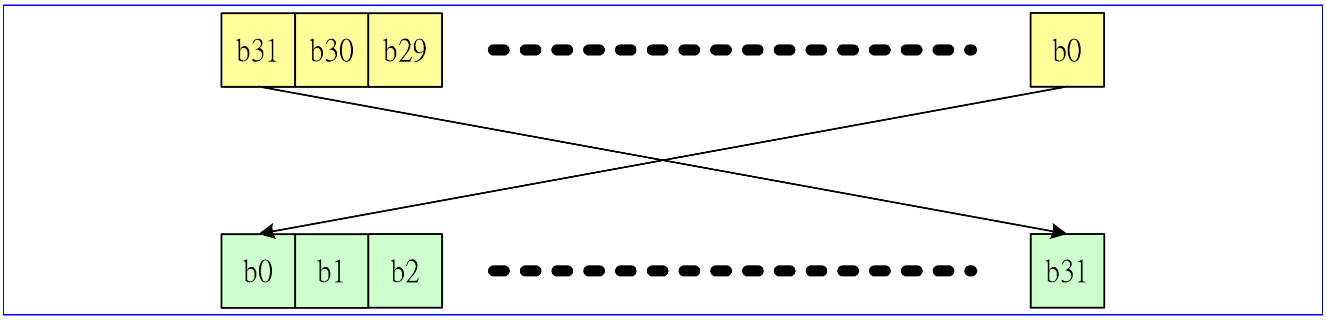

Figure 47 Type 1 bit reverse

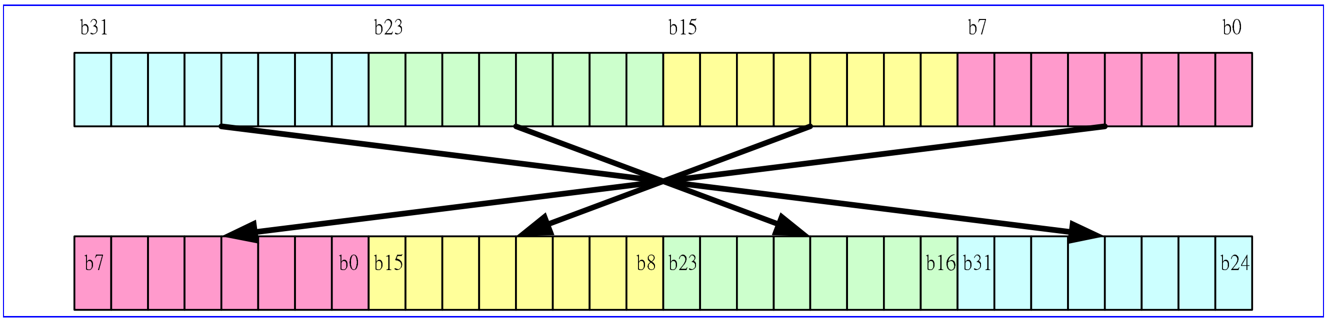

Figure 48 Type 2 bit reverse

Register Address	Register Function	Acronym
0x8209_0000	CSD RA0 Control Register	**CSD_RA0_CON**
0x8209_0004	CSD RA0 Status Register	**CSD_RA0_STA**
0x8209_0008	CSD RA0 Input Data Register	**CSD_RA0_DI**
0x8209_000C	CSD RA0 Output Data Register	**CSD_RA0_DO**
0x8209_0100	CSD RA1 6K/12K Uplink Input Data Register 0	**CSD_RA1_6K_12K_ULDI0**
0x8209_0104	CSD RA1 6K/12K Uplink Input Data Register 1	**CSD_RA1_6K_12K_ULDI1**
0x8209_0108	CSD RA1 6K/12K Uplink Status Data Register	**CSD_RA1_6K_12K_ULSTUS**
0x8209_010C	CSD RA1 6K/12K Uplink Output Data Register 0	**CSD_RA1_6K_12K_ULDO0**
0x8209_0110	CSD RA1 6K/12K Uplink Output Data Register 1	**CSD_RA1_6K_12K_ULDO1**
0x8209_0200	CSD RA1 6K/12K Downlink Input Data Register 0	**CSD_RA1_6K_12K_DLDI0**
0x8209_0204	CSD RA1 6K/12K Downlink Input Data Register 1	**CSD_RA1_6K_12K_DLDI1**
0x8209_0208	CSD RA1 6K/12K Downlink Output Data Register 0	**CSD_RA1_6K_12K_DLDO0**
0x8209_020C	CSD RA1 6K/12K Downlink Output Data Register 1	**CSD_RA1_6K_12K_DLDO1**
0x8209_0210	CSD RA1 6K/12K Downlink Status Data Register	**CSD_RA1_6K_12K_DLSTUS**
0x8209_0300	CSD RA13.6K Uplink Input Data Register 0	**CSD_RA1_3P6K_ULDI0**
0x8209_0304	CSD RA13.6K Uplink Status Data Register	**CSD_RA1_3P6K_ULSTUS**

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0x8209_0308	CSD RA13.6K Uplink Output Data Register 0	**CSD_RA1_3P6K_ULDO0**
0x8209_030C	CSD RA13.6K Uplink Output Data Register 1	**CSD_RA1_3P6K_ULDO1**
0x8209_0400	CSD RA1 3.6K Downlink Input Data Register 0	**CSD_RA1_3P6K_DLDI0**
0x8209_0404	CSD RA1 3.6K Downlink Input Data Register 1	**CSD_RA1_3P6K_DLDI1**
0x8209_0408	CSD RA1 3.6K Downlink Output Data Register 0	**CSD_RA1_3P6K_DLDO0**
0x8209_040C	CSD RA1 3.6K Downlink Status Data Register	**CSD_RA1_3P6K_DLSTUS**
0x8209_0500	CSD FAX Bit Reverse Type 1 Input Data Register	**CSD_FAX_BR1_DI**
0x8209_0504	CSD FAX Bit Reverse Type 1 Output Data Register	**CSD_FAX_BR1_DO**
0x8209_0510	CSD FAX Bit Reverse Type 2 Input Data Register	**CSD_FAX_BR2_DI**
0x8209_0514	CSD FAX Bit Reverse Type 2 Output Data Register	**CSD_FAX_BR2_DO**

Table 39 CSD Accelerater Registers

5.2.2 Register Definitions

0x8209_0000 CSD RA0 Control Register CSD_RA0_CON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name											RST	BTS0		VLD_BYTE		
Type											WO	WO		WO		
Reset											0	0		100		

VLD_BYTE Specify how many valid bytes in the current input data. It must be specified before filling data in.

BTS0 Back to state 0. Force RA0 converter go back to state 0. Incomplete word will be padded by STOP bit. For instance, back-to-state0 command is issued after 8 byte data are filled in. Then these bit after the 8th byte will be padded with stop bits, and RDYWD2 is asserted. After removing state word 2, the state pointer goes back to state 0. Note that new data filling should take place after removing state word 2, or the state pointer may be out of order.

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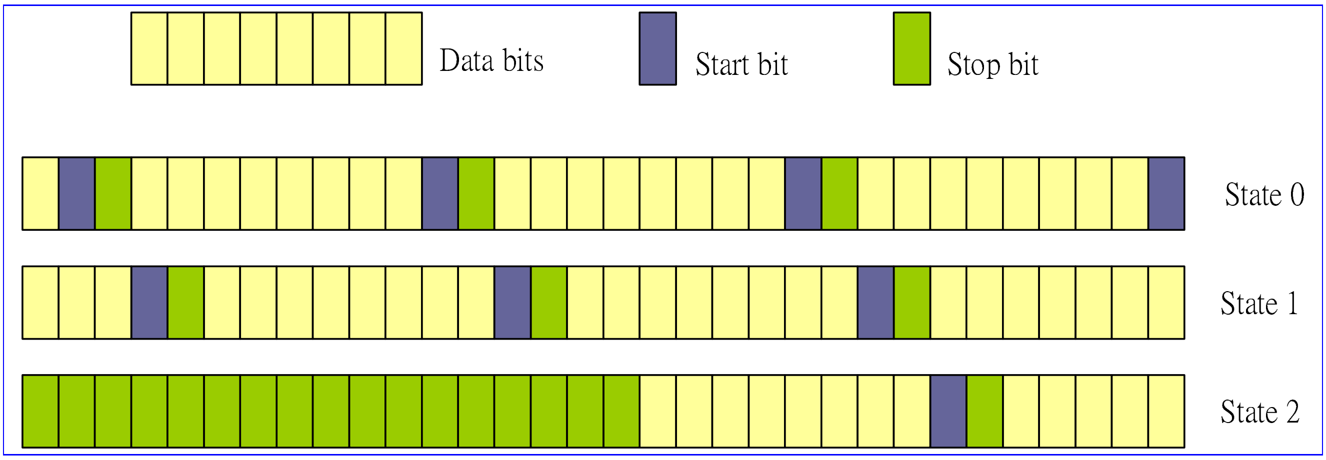

Figure 49 Example of Back to state 0

RST Reset RA0 converter. In case, erroneously operation makes data disordered. This bit can restore all state to original state.

0 Reserved

1 Reset

0x8209_0004 CSD RA0 Status Register CSD_RA0_STA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					BYTECNT				CRTSTA			RDYWD				
Type					RO				RO			RC				
Reset					0				0			0				

RDYWD0~4 Ready word. To indicate which state word is ready for withdrawal. Data should be withdrawn before next data fills into CSD_RA0_DI, if there are any bits asserted.

0 Not ready

1 Ready

CRTSTA Current state. State0 ~ State4. To indicate which state word software is filling in.

BYTECNT The total number of bytes software is filling in.

0x8209_0008 CSD RA0 Input Data Register CSD_RA0_DI

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIN															
Type	WO															
Reset	0															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DIN															
Type	WO															

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Reset	0

DIN The RA0 convert input data. Ready word indicator shall be check before filling in data. If any words are ready, withdraw them first; otherwise the ready data in RA0 converter will be replaced.

0x8209_000C CSD RA0 Output Data Register CSD_RA0_DO

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOUT															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	RO															
Reset	0															

DOUT RA0 converted data. The return data corresponds to the ready word indicator defined in CSD_RA0_STA register. The five bit of RDYWD map to state0 ~ state 4 accordingly. When CSD_RA0_DO is read, the asserted state word will be returned. If there are two state words asserted at the same time, the lower one will be returned.

0x8209_0100 CSD RA1 6K/12K Uplink Input Data Register 0 CSD_RA1_6K_12K_ULDI0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIN															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	WO															
Reset	0															

DIN The D1 to D32 of RA1 uplink data.

0x8209_0104 CSD RA1 6K/12K Uplink Input Data Register 1 CSD_RA1_6K_12K_ULDI1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	WO															
Reset	0															

DIN The D33 to D48 of RA1 uplink data.

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0x8209_0108 CSD RA1 6K/12K Uplink Status Data Register CSD_RA1_6K_12K_ULSTUS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										E7	E6	E5	E4	X	SB	SA
Type										WO	WO	WO	WO	WO	WO	WO
Reset										0	0	0	0	0	0	0

SA Represents S1, S3, S6, and S8 of status bits.

SB Represents S4 and S9 of status bits.

X Represents X of status bits.

E4 Represents E4 of status bits.

E5 Represents E5 of status bits.

E6 Represents E6 of status bits.

E7 Represents E7 of status bits.

0x8209_010C CSD RA1 6K/12K Uplink Output Data Register 0 CSD_RA1_6K_12K_ULDO0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOUT															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOU															
Type	RO															
Reset	0															

DOUT The bit 0 to bit 31 of RA1 6K/12K uplink frame.

0x8209_0110 CSD RA1 6K/12K Uplink Output Data Register 1 CSD_RA1_6K_12K_ULDO1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DOUT											
Type					RO											
Reset					0											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	RO															
Reset	0															

DOUT The bit32 to bit 59 of RA1 6K/12K uplink frame.

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0x8209_0200 CSD RA1 6K/12K Downlink Input Data Register 0 CSD_RA1_6K_12K_DLDI0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIN															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	WO															
Reset	0															

DIN The bit 0 to bit 31 of RA1 6K/12K downlink frame.

0x8209_0204 CSD RA1 6K/12K Downlink Input Data Register 1 CSD_RA1_6K_12K_DLDI1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DIN											
Type					WO											
Reset					0											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	WO															
Reset	0															

DIN The bit32 to bit 59 of RA1 6K/12K downlink frame.

0x8209_0208 CSD RA1 6K/12K Downlink Output Data Register 0 CSD_RA1_6K_12K_DLDO0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOUT															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	RO															
Reset	0															

DOUT The D1 to D32 of RA1 downlink data.

0x8209_020C CSD RA1 6K/12K Downlink Output Data Register 1 CSD_RA1_6K_12K_DLDO1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															

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Type	RO
Reset	0

DOUT The D33 to D48 of RA1 downlink data.

0x8209_0210 CSD RA1 6K/12K Downlink Status Data Register CSD_RA1_6K_12K_DLSTUS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										E7	E6	E5	E4	X	SB	SA
Type										RO	RO	RO	RO	RO	RO	RO
Reset										0	0	0	0	0	0	0

SA The result of majority votes of S1, S3, S6 and S8. SA is “0” if equal vote.
SB The result of majority votes of S4 and S9. SB is “0” if equal vote.
X The result of majority votes of two X bits in downlink frame. X is “0” if equal vote.
E4 Represents E4 of status bits.
E5 Represents E5 of status bits.
E6 Represents E6 of status bits.
E7 Represents E7 of status bits.

0x8209_0300 CSD RA1 3.6K Uplink Input Data Register 0 CSD_RA1_3P6K_ULDI0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									DIN							
Type									WO							
Reset									0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	WO															
Reset	0															

DIN The D1 to D24 of RA1 3.6K uplink data.

0x8209_0304 CSD RA1 3.6K Uplink Status Data Register CSD_RA1_3P6K_ULSTUS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										E7	E6	E5	E4	X	SB	SA
Type										WO	WO	WO	WO	WO	WO	WO
Reset										0	0	0	0	0	0	0

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SA Represents S1, S3, S6, and S8 of status bits.
SB Represents S4 and S9 of status bits.
X Represents X of status bits.
E4 Represents E4 of status bits.
E5 Represents E5 of status bits.
E6 Represents E6 of status bits.
E7 Represents E7 of status bits.

0x8209_0308 CSD RA1 3.6K Uplink Output Data Register 0 CSD_RA1_3P6K_ULDO0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOUT															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	RO															
Reset	0															

DOUT The bit 0 to bit 31 of RA1 3.6K uplink frame

0x8209_030C CSD RA1 3.6K Uplink Output Data Register 1 CSD_RA1_3P6K_ULDO1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DOUT			
Type													RO			
Reset													0			

DOUT The bit 32 to bit 35 of RA1 3.6K uplink frame

0x8209_0400 CSD RA1 3.6K Downlink Input Data Register 0 CSD_RA1_3P6K_DLDI0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIN															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	WO															
Reset	0															

DIN The bit 0 to bit 31 of RA1 3.6K downlink frame

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0x8209_0404 CSD RA1 3.6K Downlink Input Data Register 1 CSD_RA1_3P6K_DLDI1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name													DIN			
Type													WO			
Reset													0			

DIN The bit 32 to bit 35 of RA1 3.6K downlink frame

0x8209_0408 CSD RA1 3.6K Downlink Output Data Register 0 CSD_RA1_3P6K_DLDO0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									DOUT							
Type									RO							
Reset									0							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DOUT															
Type	RO															
Reset	0															

DIN The D1 to D24 of RA1 3.6K downlink data.

0x8209_040C CSD RA1 3.6K Downlink Status Data Register CSD_RA1_3P6K_DLSTUS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name										E7	E6	E5	E4	X	SB	SA
Type										RO	RO	RO	RO	RO	RO	RO
Reset										0	0	0	0	0	0	0

SA The result of majority votes of S1, S3, S6 and S8. SA is “0” if equal vote.
SB The result of majority votes of S4 and S9. SB is “0” if equal vote.
X The result of majority votes of two X bits in downlink frame. X is “0” if equal vote.
E4 Represents E4 of status bits.
E5 Represents E5 of status bits.
E6 Represents E6 of status bits.
E7 Represents E7 of status bits.

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0x8209_0500 CSD FAX Bit Reverse Type 1 Input Data Register CSD_FAX_BR1_DI

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIN															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	WO															
Reset	0															

DIN 32-bit input data for type 1 bit reverse of FAX data. The action of Type 1 bit reverse is to reverse this word by word.

0x8209_0504 CSD FAX Bit Reverse Type 1 Output Data Register CSD_FAX_BR1_DO

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOUT															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	RO															
Reset	0															

DOUT 32-bit result data for type 1 bit reverse of FAX data.

0x8209_0510 CSD FAX Bit Reverse Type 2 Input Data Register CSD_FAX_BR2_DI

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIN															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	WO															
Reset	0															

DIN 32-bit input data for type 2 bit reverse of FAX data. The action of Type 1 bit reverse is to reverse this word by byte.

0x8209_0514 CSD FAX Bit Reverse Type 2 Output Data Register CSD_FAX_BR2_DO

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOUT															
Type	RO															
Reset	0															

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	RO															
Reset	0															

DOUT 32-bit result data for type 2 bit reverse of FAX data.

5.3 FCS Codec

5.3.1 General Description

FCS (Frame Check Sequence) is used to detect errors in the following information bits:

- RLP-frame of CSD services in GSM. The frame length is fixed as 240 or 576 bits including the 24-bit FCS field.
- LLC-frame of GPRS service. The frame length is determined by the information field, and length of the FCS field is 24-bit.

Generation of the frame check sequence is very similar to the CRC coding in baseband signal processing. ETSI GSM specifications 04.22 and 04.64 both define the coding rule. The coding rules are:

1. The CRC shall be ones complement of the modulo-2 sum of:

- the remainder of $x^k \cdot (x^{23}+x^{22}+x^{21}+\ldots+x^2+x+1)$ modulo-2 divided by the generator polynomial, where k is the number of bits of the dividend. (i.e. fill the shift registers with all ones initially before feeding data)
- the remainder of the modulo-2 division by the generator polynomial of the product of x^{24} by the dividend, which are the information bits.

2. The CRC-24 generator polynomial is:

$G(x)=x^{24}+x^{23}+x^{21}+x^{20}+x^{19}+x^{17}+x^{16}+x^{15}+x^{13}+x^8+x^7+x^5+x^4+x^2+1$

3. The 24-bit CRC are appended to the data bits in the MSB-first manner.

4. Decoding is identical to encoding except that data fed into the syndrome circuit is 24-bit longer than the information bits at encoding. The dividend is also multiplied by x^{24}. If no error occurs, the remainder should satisfy

$R(x)=x^{22}+x^{21}+x^{19}+x^{18}+x^{16}+x^{15}+x^{11}+x^8+x^5+x^4$ (0x6d8930)

And the parity output word will be 0x9276cf.

In contrast to conventional CRC, this special coding scheme makes the encoder fully identical to the decoder and simplifies the hardware design.

5.3.2 Register Definitions

Register Address	Register Function	Acronym
0x8207_0000	FCS input data register	FCS_DATA

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0x8207_0004	Input data length indication register	FCS_DLEN
0x8207_0008	FCS parity output register 1, MSB part	FCS_PAR1
0x8207_000C	FCS parity output register 2, LSB part	FCS_PAR2
0x8207_0010	FCS codec status register	FCS_STAT
0x8207_0014	FCS codec reset register	FCS_RST

Table 40 FCS Registers

0x8207_0000 FCS input data register FCS_DATA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DX The data bits input. First write of this register is the starting point of the encode or decode process. X=0…15. The input format is D15·x^{n}+ D14·x^{n-1}+ D13·x^{n-2}+ … + Dk·x^{k}+ …, thus D15 is the first bit being pushed into the shift register. If the last data word is less than 16 bits, the rest bits are neglected.

0x8207_0004 Input data length indication register FCS_DLEN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LEN															
Type	WO															

LEN The MCU specifies the total data length in bits to be encoded or decoded. The data length. A number of multiple-of-8 is required (Number_of_Bytes x 8).

0x8207_0008 FCS parity output register 1, MSB part FCS_PAR1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
Type	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8207_000C FCS parity output register 2, LSB part FCS_PAR2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									P23	P22	P21	P20	P19	P18	P17	P16
Type									RC	RC	RC	RC	RC	RC	RC	RC
Reset									0	0	0	0	0	0	0	0

PX Parity bits output. For FCS_PAR2, bit 8 to bit15 will be filled by zeros when reading. X=0…23. The output format is P23·D^{23}+ P22·D^{22}+ P21·D^{21}+ … + Pk·D^{k}+ …+P1·D^{1}+P0, thus P23 is the earliest bit being popped out from the shift register and first appended to the information bits. In other words, {FCS_PAR2[7:0], FCS_PAR1[15:8], FCS_PAR1[7:0] } is the order of appending parity to data.

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0x8207_0010 FCS codec status register FCS_STAT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														BUSY	FER	RDY
Type														RC	RC	RC
Reset														0	1	0

BUSY Since the codec works in serial manner and the data word is input in parallel manner, BUSY = 1 indicates that current data word is being processed and write to FCS_DATA is invalid. BUSY = 0 allows write of FCS_DATA during encode or decode process.

- **0** IDLE
- **1** BUSY

FER Frame error indication, only for decode mode. FER = 0 means no error occurs and FER = 1 means the parity check has failed. Write of FCS_RST.RST or first write of FCS_DATA will reset this bit to 0.

- **0** Parity Check Pass
- **1** Parity Check Fail

RDY When RDY = 1, the encode or decode process has been finished. For encode, the parity data in FCS_PAR1 and FCS_PAR2 are correctly available. For decode, FCS_STAT.FER indication is valid. Write of FCS_RST.RST or first write of FCS_DATA will reset this bit to 0.

- **0** Process is on-going.
- **1** Process is finished.

0x8207_0014 FCS codec reset register FCS_RST

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													EN_DE	PAR	BIT	RST
Type													WO	WO	WO	WO

RST RST = 0 resets the CRC coprocessor. Before setup of FCS codec, the MCU needs to set RST = 0 to flush the shift register content before encode or decode.

- **0** Reset
- **1** Reserved

BIT BIT = 0 means not to invert the bit order in a byte of data words when the codec is running. BIT = 1 means the bit order in a byte written in FCS_DATA should be reversed.

- **0** Not invert the bit order of data words
- **1** Invert the bit order of data

PAR PAR = 0 means not to invert the bit order in a byte of parity words when the codec is running, include reading of FCS_PAR1 and FCS_PAR2. PAR = 1 means bit order of parity words should be reversed, in decoding or encoding.

- **0** Not invert the bit order of data words
- **1** Invert the bit order of data

EN_DE EN_DE = 0 means encode; EN_DE = 1 means decode

- **0** Encode

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1 Decode

5.4 GPRS Cipher Unit

5.4.1 General Description

The unit implements the GPRS encryption/decryption scheme that accelerates the computation of encryption and decryption GPRS pattern. The block accelerates the computation of the key stream. However the bit-wise encryption/decryption of the data is still done by the MCU.

Both GEA, GEA2 and GEA3 are supported.

Register Address	Register Function	Acronym
0x8208_0000	GPRS Encryption Algorithm Control Register	GCU_CON
0x8208_0004	GPRS Encryption Algorithm Status Register	GCU_SAT
0x8208_0008	GPRS Secret Key Kc 0 Register	GCU_SKEY0
0x8208_000C	GPRS Secret Key Kc 1 Register	GCU_SKEY1
0x8208_0010	GPRS Message Key Register	GCU_MKEY
0x8208_0014	GPRS Ciphered Data Register	GCU_CDATA

Table 41 GCU Registers

5.4.2 Register Definitions

0x8208_0000 GPRS Encryption Algorithm Control Register GCU_CON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RBO	KS		SINIT	DIR	ALG	
Type										R/W	R/W		WO	R/W	R/W	
Reset										0	10		0	0	0	

This register controls the key generation function of the GPRS Encryption Algorithm.

ALG Choose the encryption/decryption algorithm.

- 00 = GEA
- 01 = GEA2
- 10 = GEA3
- 11 = Reserved

DIR The DIRECTION input of the GPRS Encryption Algorithm.

SINIT Start initialization. The MCU writes 1 to start initialization. The bit is always read at 0.

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KS Control the read access. 00 = byte access, 01 = half word (16 bits) access, 10 = word access, 11 reserved. Default value is 10.

RBO Reversal Byte Order bit. If the bit was set to 1, the byte order of GCU_SKEY0, GCU_SKEY1, GCU_MKEY in write operation and GCU_SKEY0, GCU_SKEY1, GCU_MKEY, GCU_CKEY in read operation would be the reverse of baseband processor, and if the bit was 0, the behavior would be the same as baseband processor. Byte-order of GCU_CON and GCU_SAT is not affected. The default value is 0 which is different from that in MT6218B.

0x8208_0004 GPRS Encryption Algorithm Status Register GCU_STA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STAT													KEY_COM	INIT	
Type	RO													RO	RO	
Reset	110													0	0	

This register shows the status of the GPRS Encryption unit.

INIT Initialization flag.

- **0** Otherwise
- **1** GCU is currently performing the initialization phase of GEA or GEA2.

KEY_COM Key-stream computation.

- **0** a new key is available or the GCU is in initialization phase of GEA , GEA2 or GEA3
- **1** the GCU is computing new key stream for GEA, GEA2, or GEA3

STAT The state of GCU core of GEA and GEA2. For debug purpose

.

0x8208_0008 GPRS Secret Key Kc 0 Register GCU_SKEY0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	KC[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KC[15:0]															
Type	R/W															
Reset	0															

0x8208_000C GPRS Secret Key Kc 1 Register GCU_SKEY1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	KC[63:48]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KC[47:32]															

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Type	R/W
Reset	0

KC This set of registers shall be programmed with the GPRS Encryption Algorithm secret key.

0x8208_0010 GPRS Message Key Register GCU_MKEY

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MKEY[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MKEY[15:0]															
Type	R/W															
Reset	0															

MKEY This register shall be programmed with the “message key” for the GPRS Encryption Algorithm.

0x8208_0014 GPRS Ciphered DATA Register GCU_CDATA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDATA[31:16]															
Type	RO															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDATA[15:0]															
Type	RO															

CDATA The register contains the key stream. GCU will continue to generate next word of key while current word of key is removed. Note : Before read CDATA, make cure KEY_COM to be 1.

5.4.3 Programming Guide

To trigger the hardware, all register fields in GCU_SKEY0, GCU_SKEY1, and GCU_MKEY must be well informed. Then program GCU_STA to kick-off hardware operation. Then confirm the KEY_COM register to be high before read-back the CDATA.

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6 Multi-Media Subsystem

MT6253 is specially designed to support multi-media terminals. It integrates several hardware based accelerators, like advanced LCD display controller and hardware Image Resizer. Besides, MT6253 also incorporates NAND Flash, USB Device and SD/MMC/MS/MS Pro Controllers for massive data transfers and storages. This chapter describes those functional blocks in detail.

6.1 LCD Interface

6.1.1 General Description

MT6253 contains a versatile LCD controller which is optimized for multimedia applications. This controller supports many types of LCD modules and contains a rich feature set to enhance the functionality. These features are:

- Up to 320 x 240 resolution
- The frame buffer supports 8bpp indexed color, RGB 565, RGB 888 and ARGB 8888 format.
- Supports 8-bpp (RGB332), 12-bpp (RGB444), 16-bpp (RGB565), 18-bpp (RGB666) and 24-bpp (RGB888) LCD modules.
- 4 Layers Overlay with individual color depth, window size, vertical and horizontal offset, source key, alpha value and display rotation control(90°,180°, 270°, mirror and mirror then 90°, 180° and 270°)
- One Color Look-Up Table
- Three Gamma Correction Tables

For parallel LCD modules, the LCD controller use dedicated 8/9-bit parallel interface to access them and 8080 type interface is supported. It can transfer the display data from the internal SRAM or external SRAM/Flash Memory to the off-chip LCD modules.

For serial LCD modules, this interface performs parallel to serial conversion and both 8- and 9- bit serial interface is supported. The 8-bit serial interface uses four pins – LSCE#, LSDA, LSCK and LSA0 – to enter commands and data. Meanwhile, the 9-bit serial interface uses three pins – LSCE#, LSDA and LSCK – for the same purpose. Data read is not available with the serial interface and data entered must be 8 bits.

The signals of serial interface share the pin NLD[8:6] with parallel interface. NLD[8] is for serial clock, NLD[7] is for serial data out, and NLD[6] is for serial A0. The two parallel chip select pins LPCE0B and LPCE1B can be configured for serial interface chip selects individually. Please see register LCD_IOCNF at 0x9000_0020.

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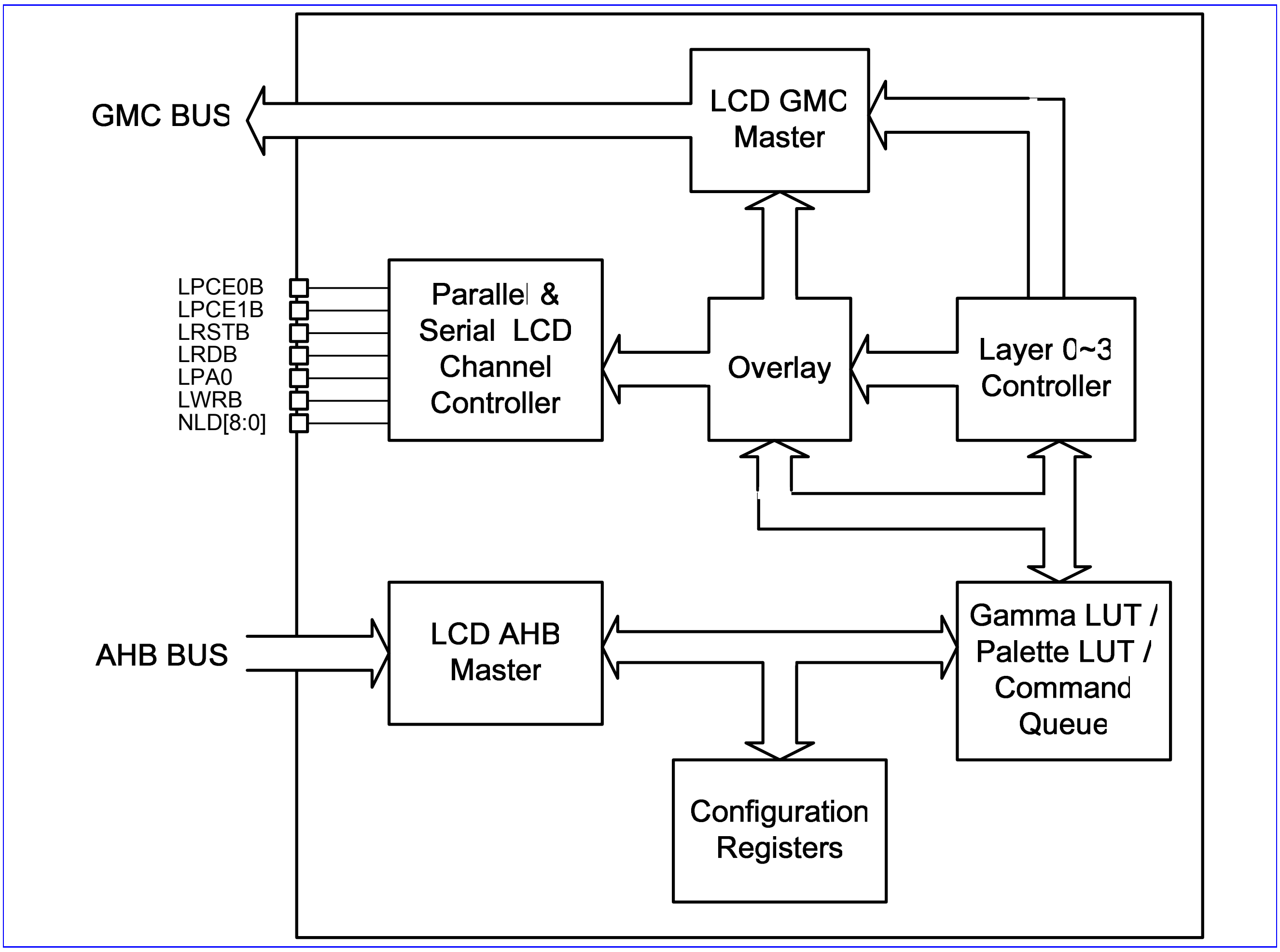

Figure 50 LCD Interface Block Diagram

LCD = 0x9000_0000

Address	Register Function	Width	Acronym	Doubled regsiter
0X9000_0000h	LCD Interface Status Register	16	**LCD_STA**	
0X9000_0004h	LCD Interface Interrupt Enable Register	16	**LCD_INTEN**	
0X9000_0008h	LCD Interface Interrupt Status Register	16	**LCD_INTSTA**	
0X9000_000ch	LCD Interface Frame Transfer Register	16	**LCD_START**	
0X9000_0010h	LCD Parallel/Serial LCM Reset Register	16	**LCD_RSTB**	
0X9000_0014h	LCD Serial Interface Configuration Register	16	**LCD_SCNF**	
0X9000_0018h	LCD Parallel Interface 0 Configuration Register	32	**LCD_PCNF0**	
0X9000_001ch	LCD Parallel Interface 1 Configuration Register	32	**LCD_PCNF1**	

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0X9000_0020h	LCD Parallel/Serial Interface Configuration Register	16	**LCD_IOCNF**	
0X9000_0024h	LCD Tearing Control Register	16	**LCD_TECON**	
0X9000_0028h	LCD Miscellaneous Register	16	**LCD_MISC**	
0X9000_002Ch	LCD GMC Port Throttle Register	32	**LCD_GMC_THROTTLE**	
0X9000_0030h	LCD ROI Window Write to Memory Address Register 0	32	**LCD_WROI_W2MADD**	Yes
0X9000_0040h	LCD Main Window Size Register	32	**LCD_MWINSIZE**	
0X9000_0044h	LCD ROI Window Write to Memory Offset Register	32	**LCD_WROI_W2MOFS**	Yes
0X9000_0048h	LCD ROI Window Write to Memory Control Register	16	**LCD_WROI_W2MCON**	Yes
0X9000_0050h	LCD ROI Window Control Register	32	**LCD_WROICON**	Yes
0X9000_0054h	LCD ROI Window Offset Register	32	**LCD_WROIOFS**	Yes
0X9000_0058h	LCD ROI Window Command Start Address Register	16	**LCD_WROICADD**	Yes
0X9000_005ch	LCD ROI Window Data Start Address Register	16	**LCD_WROIDADD**	Yes
0X9000_0060h	LCD ROI Window Size Register	32	**LCD_WROISIZE**	Yes
0X9000_0064h	LCD ROI Window Hardware Refresh Register	32	**LCD_WROI_HWREF**	
0X9000_0068h	LCD ROI Direct Couple Register	32	**LCD_WROI_DC**	
0X9000_006Ch	LCD ROI Window Background Color Register	32	**LCD_WROI_BGCLR**	Yes
0X9000_0070h	LCD Layer 0 Window Control Register	32	**LCD_L0WINCON**	Yes
0X9000_0074h	LCD Layer 0 Source Color Key Register	32	**LCD_L0WINSKEY**	Yes
0X9000_0078h	LCD Layer 0 Window Display Offset Register	32	**LCD_L0WINOFS**	Yes
0X9000_007ch	LCD Layer 0 Window Display Start Address Register	32	**LCD_L0WINADD**	Yes
0X9000_0080h	LCD Layer 0 Window Size	32	**LCD_L0WINSIZE**	Yes
0X9000_0084h	LCD Layer 0 Scroll Start Offset	32	**LCD_L0WINSCRL**	Yes
0X9000_0090h	LCD Layer 1 Window Control Register	32	**LCD_L1WINCON**	Yes
0X9000_0094h	LCD Layer 1 Source Color Key Register	32	**LCD_L1WINSKEY**	Yes
0X9000_0098h	LCD Layer 1 Window Display Offset Register	32	**LCD_L1WINOFS**	Yes
0X9000_009ch	LCD Layer 1 Window Display Start Address Register	32	**LCD_L1WINADD**	Yes
0X9000_00a0h	LCD Layer 1 Window Size	32	**LCD_L1WINSIZE**	Yes
0X9000_00a4h	LCD Layer 1 Scroll Start Offset	32	**LCD_L1WINSCRL**	Yes
0X9000_00b0h	LCD Layer 2 Window Control Register	32	**LCD_L2WINCON**	Yes
0X9000_00b4h	LCD Layer 2 Source Color Key Register	32	**LCD_L2WINSKEY**	Yes
0X9000_00b8h	LCD Layer 2 Window Display Offset Register	32	**LCD_L2WINOFS**	Yes
0X9000_00bch	LCD Layer 2 Window Display Start Address Register	32	**LCD_L2WINADD**	Yes
0X9000_00c0h	LCD Layer 2 Window Size	32	**LCD_L2WINSIZE**	Yes
0X9000_00c4h	LCD Layer 2 Scroll Start Offset	32	**LCD_L2WINSCRL**	Yes
0X9000_00d0h	LCD Layer 3 Window Control Register	32	**LCD_L3WINCON**	Yes

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0X9000_00d4h	LCD Layer 3 Source Color Key Register	32	**LCD_L3WINSKEY**	**Yes**
0X9000_00d8h	LCD Layer 3 Window Display Offset Register	32	**LCD_L3WINOFS**	**Yes**
0X9000_00dch	LCD Layer 3 Window Display Start Address Register	32	**LCD_L3WINADD**	**Yes**
0X9000_00e0h	LCD Layer 3 Window Size	32	**LCD_L3WINSIZE**	**Yes**
0X9000_00e4h	LCD Layer 3 Scroll Start Offset	32	**LCD_L3WINSCRL**	**Yes**
0X9000_0300h	Image Rotator DMA GMC Port Controller Register	32	**LCD_IRT_GMCCON**	
0X9000_0304h	Image Rotator DMA FIFO Base Address Register	32	**LCD_IRT_FIFO_BASE**	
0X9000_0308h	Image Rotator DMA FIFO Length Register	32	**LCD_IRT_FIFO_LEN**	
0X9000_030Ch	Image Rotator DMA Write FIFO Count Register	32	**LCD_IRT_WR_CNT**	
0X9000_0310h	Image Rotator DMA Read FIFO Count Register	32	**LCD_IRT_RD_CNT**	
0X9000_0314h	Image Rotator DMA FIFO Line Count Register	32	**LCD_IRT_FIFO_LINE_CNT**	
0X9000_0318h	Image Rotator DMA Read/Write FIFO Line Index Register	32	**LCD_IRT_YIDX**	
0X9000_0320h	Image Rotator DMA Frame Base Address	32	**LCD_FRAME_BASE**	
0X9000_0324h	Image Rotator DMA Size	32	**LCD_IRT_SIZE**	
0X9000_0328h	Image Rotator DMA Background X Size	16	**LCD_IRT_BKGD_XSIZE**	
0X9000_032Ch	Image Rotator DMA Clip Pixel Number	16	**LCD_IRT_CLIP_PXLNUM**	
0X9000_4000h	LCD Parallel Interface 0 Data	32	**LCD_PDAT0**	
0X9000_4100h	LCD Parallel Interface 0 Command	32	**LCD_PCMD0**	
0X9000_5000h	LCD Parallel Interface 1 Data	32	**LCD_PDAT1**	
0X9000_5100h	LCD Parallel Interface 1 Command	32	**LCD_PCMD1**	
0X9000_8000h	LCD Serial Interface 1 Data	16	**LCD_SDAT1**	
0X9000_8100h	LCD Serial Interface 1 Command	16	**LCD_SCMD1**	
0X9000_9000h	LCD Serial Interface 0 Data	16	**LCD_SDAT0**	
0X9000_9100h	LCD Serial Interface 0 Command	16	**LCD_SCMD0**	
0X9000_C000h ~ C3FFh	LCD Color Palette LUT Register	32	**LCD_PAL**	
0X9000_C400h ~ C4FFh	LCD Gamma Correction LUT Register	32	**LCD_GAMMA**	
0X9000_C500h ~ C57Fh	LCD Interface Command/Parameter0 Register	32	**LCD_COMD0**	
0X9000_C580h ~ C5FFh	LCD Interface Command/Parameter1 Register	32	**LCD_COMD1**	

Table 42 Memory map of LCD Interface

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6.1.2 Register Definitions

The base address of LCD is 0x9000_0000.

0X9000_0000h LCD Interface Status Register LCD_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													WAIT_SYNC	WAIT_VSYNC	WAIT_HWTRIG	RUN
Type													R	R	R	R
Reset													0	0	0	0

RUN LCD Interface Running Status. Note: This status bit

WAIT_HWTRIG LCD is waiting for hardware trigger signal

WAIT_VSYNC LCD is waiting for vertical mode LCM tearing-free sync signal

WAIT_SYNC LCD is waiting for LCM tearing-free sync signal

0X9000_0004h LCD Interface Interrupt Enable Register LCD_INTEN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SYNC	VSYNC	HWTRIG	CPL
Type													R/W	R/W	R/W	R/W
Reset													0	0	0	0

CPL Enable the interrupt when LCD frame transfer completes.

HWTRIG Enable the interrupt when hardware trigger signal arrives.

VSYNC Enable the interrupt when vertical mode LCM tearing-free sync signal arrives.

SYNC Enable the interrupt when LCM tearing-free sync signal arrives.

0X9000_0008h LCD Interface Interrupt Status Register LCD_INTSTA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SYNC	VSYNC	HWTRIG	CPL
Type													R	R	R	R
Reset													0	0	0	0

CPL Interrupt of LCD frame transfer completion occurs.

HWTRIG Interrupt of the arrival of hardware trigger signal occurs.

VSYNC Interrupt of the arrival of vertical mode LCM tearing-free sync signal for occurs.

SYNC Interrupt of the arrival of LCM tearing-free sync signal occurs.

0X9000_000Ch LCD Interface Frame Transfer Register LCD_START

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	START															
Type	R/W															
Reset	0															

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START Start Control of LCD Frame Transfer

0X9000_0010h LCD Parallel/Serial Interface Reset Register LCD_RSTB

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RSTB
Type																R/W
Reset																1

RSTB Parallel/Serial LCD Module Reset Control

0X9000_0014h LCD Serial Interface Configuration Register LCD _SCNF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IF_CLK		GAMMA_ID			NON_DBI	CSP1	CSP0				3-WIRE	DIV		SPH	SPO
Type	R/W	R/W	R/W	R/W		R/W	R/W	R/W				R/W	R/W		R/W	R/W
Type	0	0	1	1		0	0	0				0	0		0	0

SPO Clock Polarity Control, see **Figure 51**.

SPH Clock Phase Control, see **Figure 51**.

DIV Serial Clock Divide Select Bits

- **00** The output LSCK frequency = Serial interface base clock frequency /2
- **01** The output LSCK frequency = Serial interface base clock frequency /4
- **10** The output LSCK frequency = Serial interface base clock frequency /8
- **11** The output LSCK frequency = Serial interface base clock frequency /16

Serial interface base clock frequency depends on the value of IF_CLK.

3-WIRE 3-wire or 4-wire Interface Selection

- **0** 4-wire interface mode. Use LSA0 to indicate the transaction is command or data.
- **1** 3-wire interface mode. Use the first bit (A0) on LSDA to indicate the transaction is command or data.

CSP0 Serial Interface Chip Select 0 Polarity Control

- **0** Low active
- **1** High active

CSP1 Serial Interface Chip Select 1 Polarity Control

- **0** Low active
- **1** High active

NON_DBI Non-DBI type C serial interface.

- **0** DBI type C serial interface. Transfer 8 bits per transaction in 4-wire mode or 9 bits per transaction in 3-wire mode.
- **1** Non-DBI type C serial interface. Transfer N bits per transaction in 4-wire mode or N+1 bits per transaction in 3-wire mode. N is specified by AHB data size if AHB directly writes the ports mapped to serial interface, or by bit7-6 of LCD_WROICON if LCD_WROICADD and LCD_WROIDADD are set to the ports mapped to serial interface.

GAMMA_ID Gamma correction LUT ID

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00	table 0
01	table 1
10	table 2
11	no gamma correction applied

IF_CLK Serial interface base clock frequency.

00	52MHz
01	13MHz
10	26MHz
11	reserved

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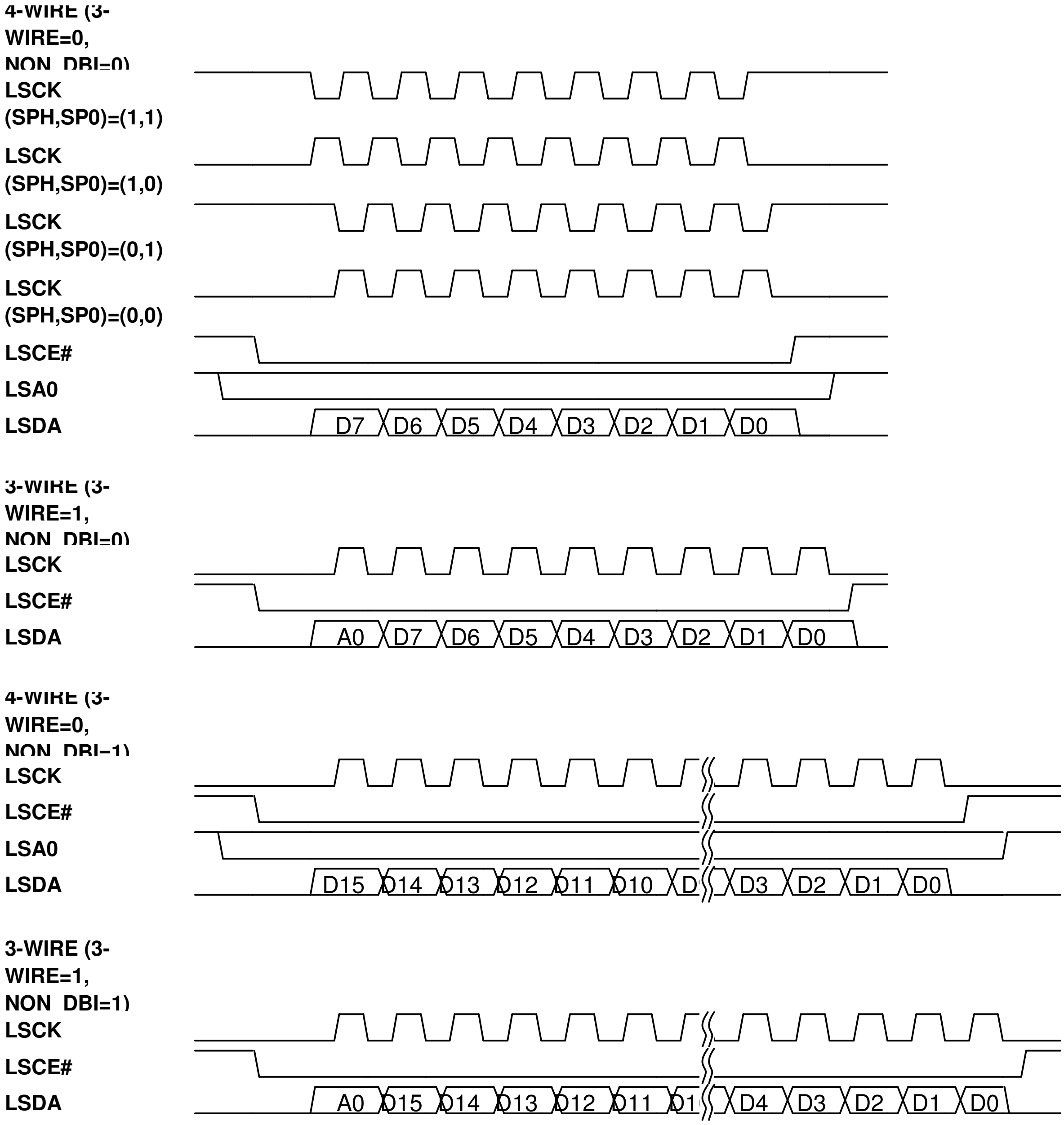

Figure 51 Serial interface timing diagram

0X9000_0018h LCD Parallel Interface Configuration Register 0 LCD_PCNF0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	C2WS		C2WH		C2RS				GAMMA_ID_R		GAMMA_ID_G		GAMMA_ID_B		DW	
Type	R/W		R/W		R/W				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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	0		0		0				1	1	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IF_CLK			WST					DOEN_DIS	RW_DIS		RLT				
Type	R/W	R/W		R/W					R/W	R/W		R/W				
Reset	0	0		0					0	0		0				

RLT Read Latency Time, must >=1, see **Figure 53**.

RW_DIS Disable wr_b, rd_b, cs_b
- **0** Enable wr_b, rd_b, cs_b
- **1** Disable wr_b, rd_b, cs_b.

DOEN_DIS Disable parallel interface data output enable
- **0** Enable parallel interface data output enable
- **1** Disable parallel interface data output enable

WST Write Wait State Time, see **Figure 52**.

IF_CLK Parallel interface base clock frequency.
- **00** 52MHz
- **01** 13MHz
- **10** 26MHz
- **11** reserved

DW Data width of parallel interface 0
- **00** 8 bit
- **01** 9 bit
- **Others** reserved

GAMMA_ID_R Gamma Correction LUT ID for Red Component
- **00** table 0
- **01** table 1
- **10** table 2
- **11** no gamma correction applied

GAMMA_ID_G Gamma correction LUT ID for Green Component
- **00** table 0
- **01** table 1
- **10** table 2
- **11** no gamma correction applied

GAMMA_ID_B Gamma correction LUT ID for Blue Component
- **00** table 0
- **01** table 1
- **10** table 2
- **11** no gamma correction applied

Note: If the value of any GAMMA_ID_* is not 3, then all of these three fields can't be 3.

C2RS Chip Select (LPCE#) to Read Strobe (LRD#) Setup Time, see **Figure 53**.

C2WH Chip Select (LPCE#) to Write Strobe (LWR#) Hold Time, see **Figure 52**.

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C2WS Chip Select (LPCE#) to Write Strobe (LWR#) Setup Time, see **Figure 52**.

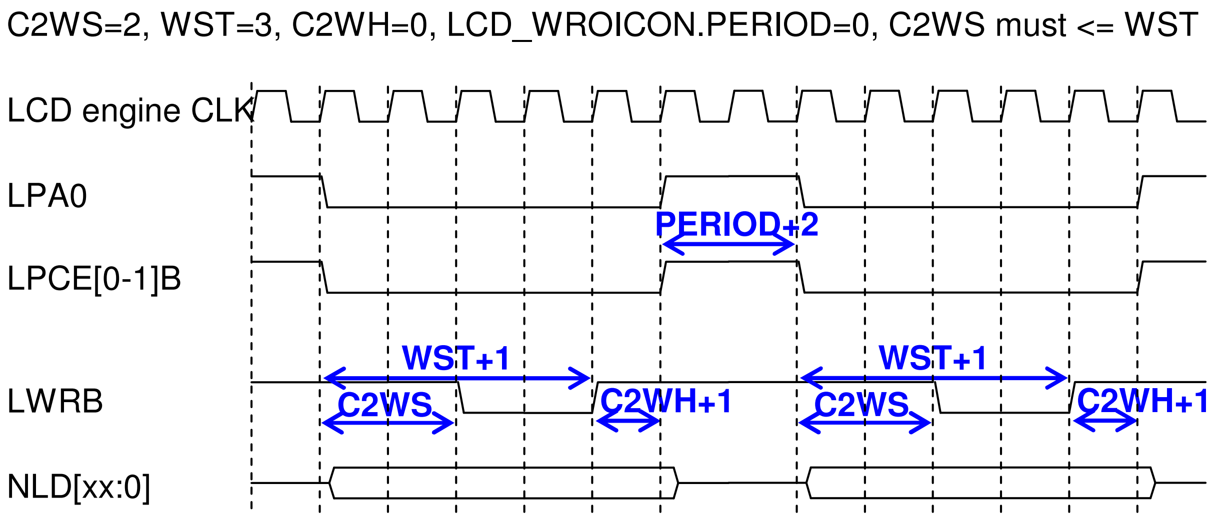

Figure 52 Parallel interface write timing diagram

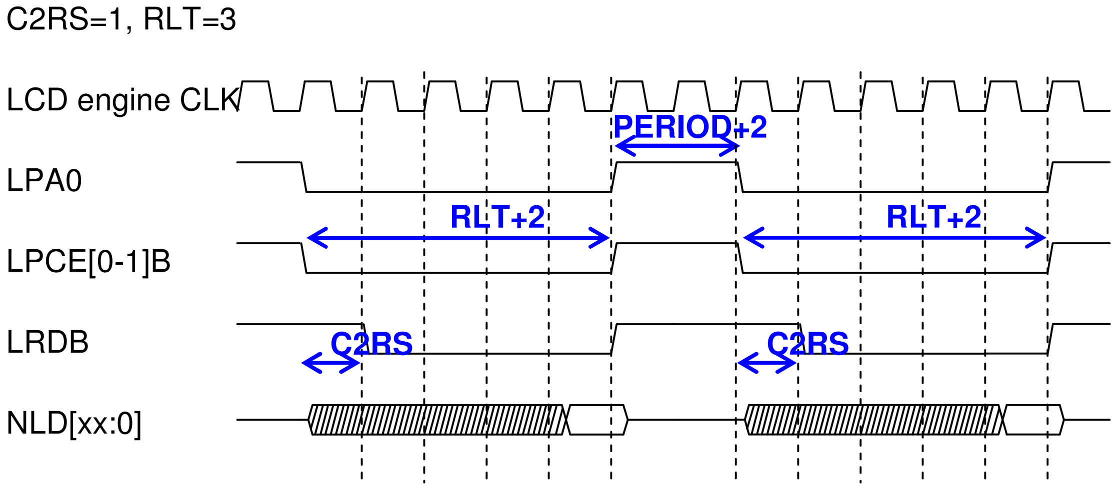

Figure 53 Parallel interface read timing diagram

0X9000_001Ch LCD Parallel Interface Configuration Register 1 LCD_PCNF1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	C2WS		C2WH		C2RS						GAMMA_ID				DW	
Type	R/W		R/W		R/W						R/W	R/W			R/W	
	0		0		0						1	1			00	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	26M	13M		WST								RLT				
Type	R/W	R/W		R/W								R/W				

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Reset	0	0		0								0				

RLT Read Latency Time, must >=1, see **Figure 53**.

WST Write Wait State Time, see **Figure 52**.

IF_CLK Parallel interface base clock frequency.

- **00** 52MHz
- **01** 13MHz
- **10** 26MHz
- **11** reserved

DW Data width of parallel interface 0

- **00** 8 bit
- **01** 9 bit
- **Others** reserved

GAMMA_ID Gamma correction LUT ID

- **00** table 0
- **01** table 1
- **10** table 2
- **11** no gamma correction applied

C2RS Chip Select (LPCE#) to Read Strobe (LRD#) Setup Time, **Figure 53**.

C2WH Chip Select (LPCE#) to Write Strobe (LWR#) Hold Time, see **Figure 52**.

C2WS Chip Select (LPCE#) to Write Strobe (LWR#) Setup Time, see **Figure 52**.

0X9000_0020h LCD Parallel/Serial Interface Configuration Register LCD_IOCNF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CS1	CS0
Type															R/W	R/W
Reset															0	0

CS0 chip select 0 selection

- **0** chip select 0 (LPCE0B) is for parallel interface 0
- **1** chip select 0 (LPCE0B) is for serial interface 0

CS1 chip select 1 selection

- **0** chip select 1 (LPCE1B) is for parallel interface 1
- **1** chip select 1 (LPCE1B) is for serial interface 1

LCD Controller Synchronization Modes

When TE_EN is enabled, LCD controller will synchronize its updating to LCM refresh timing. And it supports two synchronizing modes depending on TE_MODE.

TE_MODE value	Synchronization Mode
0	Vertical Synchronization mode. LCD controller starts to update LCM when it detects a TE signal.
1	Vertical and Horizontal Synchronization mode.

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TE_MODE value	Synchronization Mode
	LCD controller starts to update LCM when it detects a vertical TE and following (TE_HS_CNT_MATCH_VALUE+1) horizontal TEs.

Table 43 LCD Controller Synchronization Mode

TE Signal Polarity

TE_EDGE_SEL can be used to select TE polarity for TE signal detection.

TE_EDGE_SEL value	TE signal detection
0	Detect a TE signal at its rising edge. This setting is for active high TE signal.
1	Detect a TE signal at its falling edge. This setting if for active low TE signal.

Table 44 TE Signal Polarity

Vertical Synchronization Mode

In Vertical Synchronization mode, the LCD controller assumes TE input is only a vertical synchronization signal.

In this mode, LCD controller starts to update LCM after each rising edge of the TE input (or falling edge, if TE_EDGE_SEL is set to 1) (see **Figure 54**).

In this mode, TE_VS_WIDTH_LIMIT, TE_VS_WIDTH_CNT_DIV, TE_HS_CNT_MATCH_VALUE are not used.

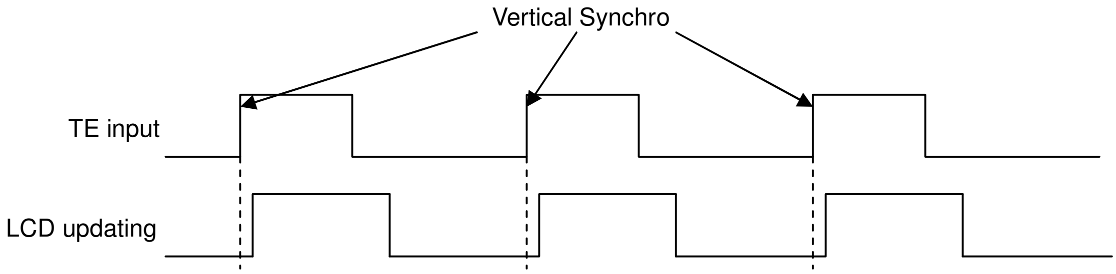

Figure 54 Vertical Synchronization Mode

Vertical and Horizontal Synchronization Mode

In Vertical and Horizontal Synchronization mode, the LCD controller assumes TE input is an OR of vertical and horizontal synchronization signal.

TE_VS_WIDTH_LIMIT gives the minimum time that TE input must stay active to be detected by the LCD controller as a vertical synchronization. This time is (TE_VS_WIDTH_LIMIT+1)*(divisor specified by TE_VS_WIDTH_CNT_DIV) clock cycles. Any pulse longer than this time is considered a vertical synchronization. Any pulse shorter than this time is considered a horizontal synchronization.

Once a vertical synchronization has been detected, the LCD controller counts the active edges on the TE input.

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When the number of active edges reaches TE_HS_CNT_MATCH_VALUE, LCD controller starts to update LCM. If a new vertical synchronization is detected before HS_CNT_MATCH_VALUE horizontal synchro have been detected, the counter is reset and horizontal synchronization count begins once again (see **Figure 55**).

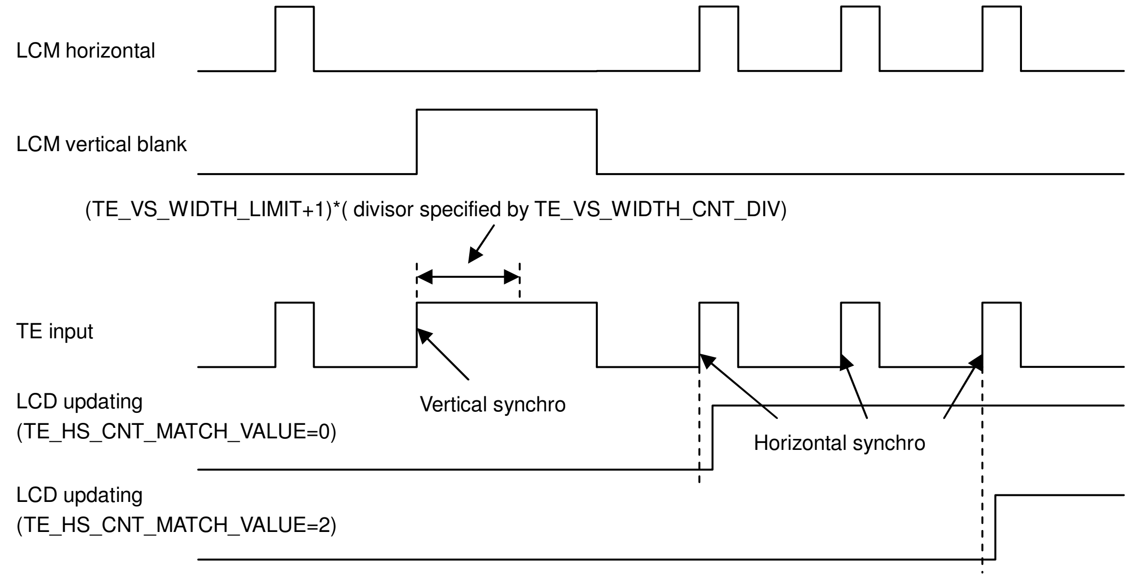

Figure 55 Vertical and Horizontal Synchronization Mode

0X9000_0024h LCD Tearing Control Register LCD_TECON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TE_VS_WIDTH_LIMIT														TE_VS_WIDTH_CNT_DIV	
Type	R/W														R/W	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TE_HS_CNT_MATCH_VALUE											TE_REPEAT	TE_MODE	TE_EDGE_SEL	TE_EN
Type		R/W											R/W	R/W	R/W	R/W
Reset		NA											0	0	0	0

TE_EN Enable tearing control. LCD controller will synchronize to LCM refresh timing.

TE_EDGE_SEL Select sync edge.

- **0** Rising edge
- **1** Falling edge

TE_MODE Tearing control mode.

- **0** Start transmission to LCD after TE edge.
- **1** Wait (TE_HS_CNT_MATCH_VALUE+1) lines after vertical TE edge to start transmission to LCD.

TE_REPEAT Repeat mode.

- **0** update LCM once every TE signal coming.

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1 repeat updating LCM after TE signal coming.

TE_HS_CNT_MATCH_VALUE Trigger LCD update after delaying (TE_HS_CNT_MATCH_VALUE+1) lines after vertical TE edge.

TE_VS_WIDTH_CNT_DIV Engine clock divisor for vertical TE detection.

00 divide engine clock by 8
01 divide engine clock by 16
10 divide engine clock by 32
11 divide engine clock by 64

TE_VS_WIDTH_LIMIT If the width of a TE pulse is larger than (TE_VS_WIDTH_LIMIT+1)* (divisor specified by TE_VS_WIDTH_CNT_DIV), it is a vertical TE, otherwise it is a horizontal TE.

0X9000_0028 LCD Miscellaneous Register LCD_MISC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SET_COMP	SET_COMP_EN
Type															R/W	R/W
Reset															0	0

SET_COMP_EN Enable bit of group setting completion indicator (SET_COMP).

SET_COMP A group setting completion indicator.

When LCD is in hardware trigger mode, the timing of starting to update a frame is decided by LCD previous module. It sends hardware trigger signal to LCD, and then LCD starts to update a frame. Software doesn't know the timing. If a group of setting, which changes layers setting, ROI setting, or commands in command queue, are split by hardware trigger, the next frame updating is incorrect. SET_COMP_EN can enable the protection of the indivisibility of the group of setting. After the group of setting is completed, set SET_COMP, and then the new setting will be applied at the next hardware trigger.

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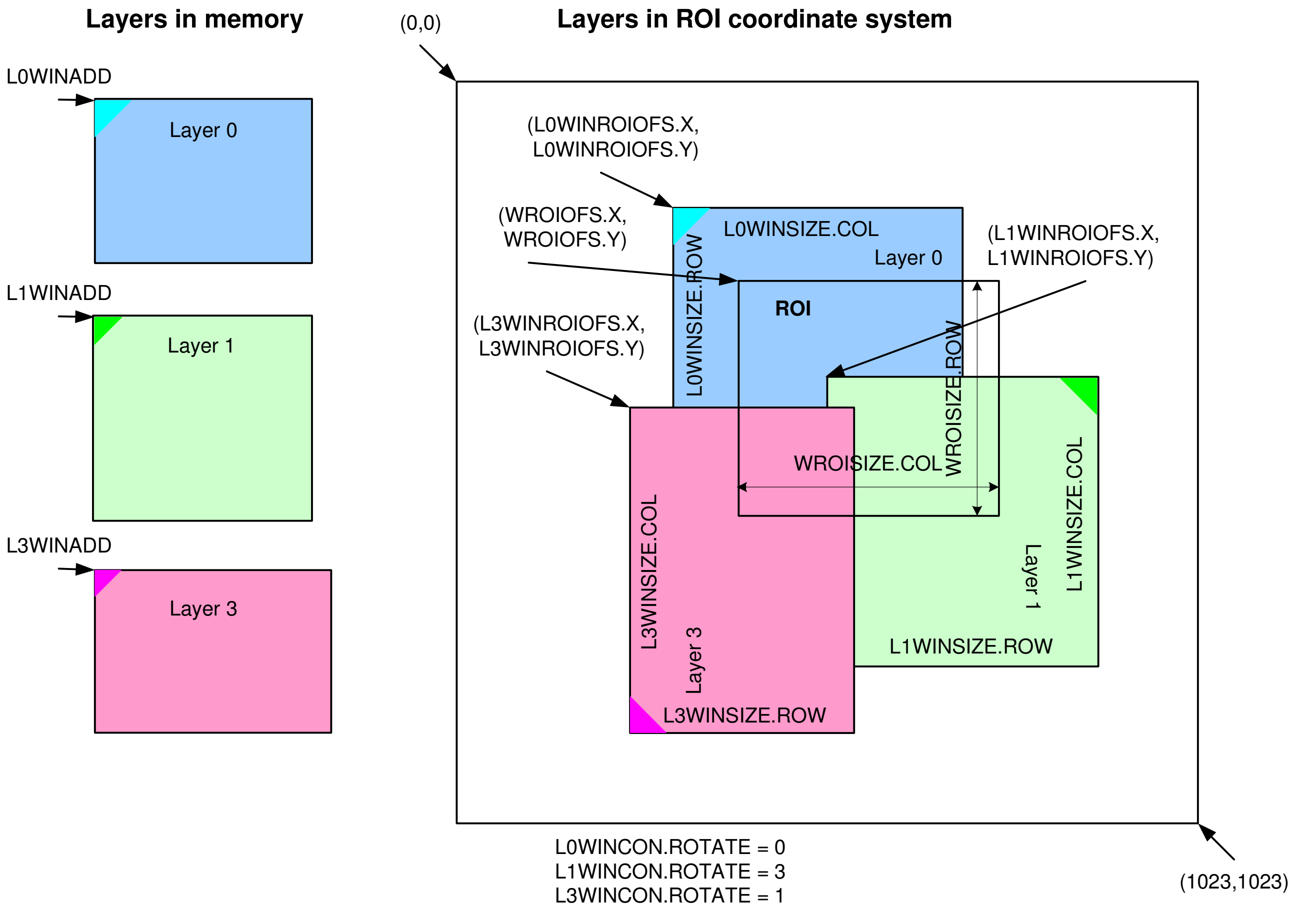

Figure 56 Layers and ROI setting

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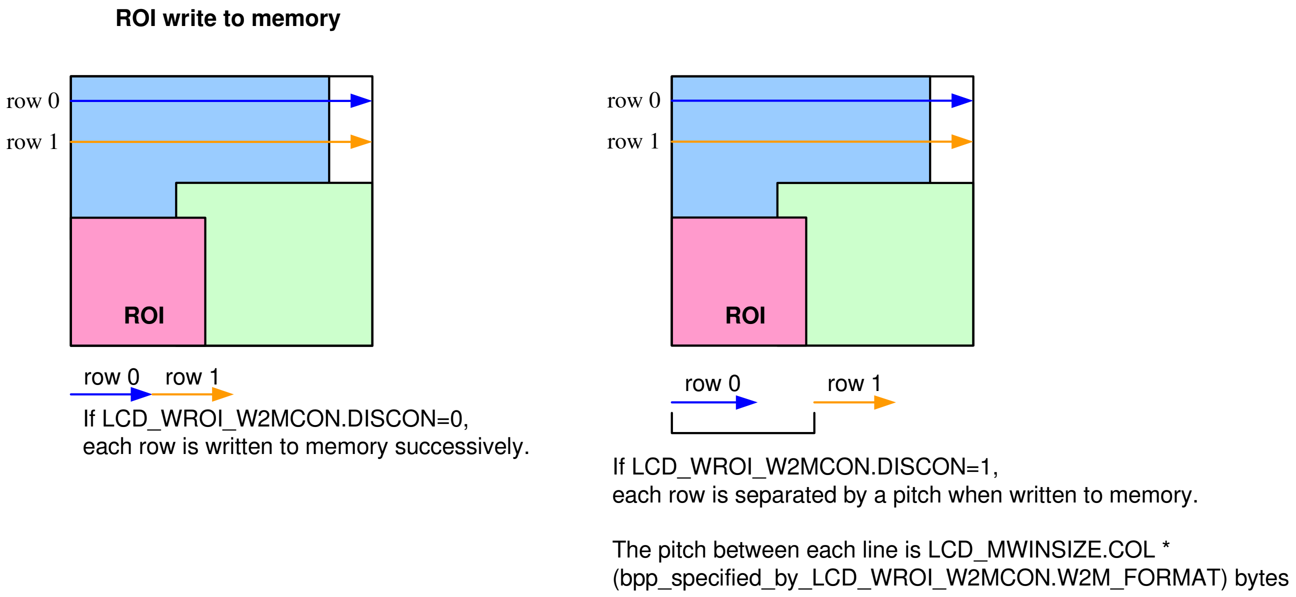

Figure 57 ROI write to memory setting

0X9000_002Ch LCD GMC Port Control Register LCD_GMCCON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	THROTTLE_PERIOD															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												THROTTLE_EN		MAX_BURST		
Type												R/W		R/W	R/W	R/W
Reset												0		0	1	0

MAX_BURST Specify the maximum burst length of GMC request.

- **000** Single 4 bytes access
- **001** Burst 4 beats access, and one beat is 2 bytes. Total data amount is 8 bytes per access.
- **010** Burst 4 beats access, and one beat is 4 bytes. Total data amount is 16 bytes per access.
- **011** Burst 8 beats access, and one beat is 4 bytes. Total data amount is 32 bytes per access.
- **100** Burst 16 beats access, and one beat is 4 bytes. Total data amount is 64 bytes per access.
- **Others** Single 4 bytes access

THROTTLE_EN Enable GMC port throttling.

THROTTLE_PERIOD Throttle down LCD GMC port access speed. It specifies how many AHB bus cycles between two GMC requests. There is a down counter, throttle_cnt, to count down for the interval between two GMC requests. It counts from THROTTLE_PERIOD when lcd_greq rising to zero, and the next GMC request is allowed to issue when throttle_cnt=0. Please see **Figure 58**. The maximum GMC bandwidth is limited to

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$$\frac{\text{bytes_per_GMC_access} \times 1000}{\text{throttle_period} \times \text{AHB_cycle_time(ns)}} = \frac{\text{bytes_per_GMC_access} \times 1000}{\text{throttle_period} \times 19.2\text{(ns)}} \text{MBytes/sec}$$

Bytes_per_GMC_access is specified by MAX_BURST.

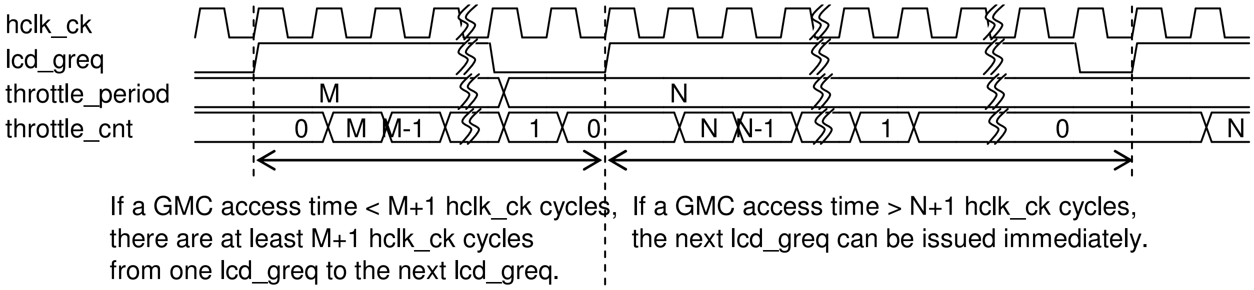

Figure 58 GMC throttle mechanism

0X9000_0030h Region of Interest Window Write to Memory Address FB Register LCD_WROI_W2MADD

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	W2M_ADDR0															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	W2M_ADDR0															
Type	R/W															

W2M_ADDR Write to memory address (byte address) for Frame Buffer.

0X9000_0040h Main Window Size Register LCD_MWINSIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ROW									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							COLUMN									
Type							R/W									

COLUMN 10-bit Virtual Image Window Column Size in unit of pixel

ROW 10-bit Virtual Image Window Row Size in unit of pixel

0X9000_0044h Region of Interest Window Write to Memory Offset Register LCD_WROI_W2MOFS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							Y-OFFSET									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							X-OFFSET									
Type							R/W									

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This control register is used to specify the offset of the ROI window from the LCD_WROI_W2MADDR when writing the ROI window's content to memory.

X-OFFSET the x offset of ROI window in the destination memory.

Y-OFFSET the y offset of ROI window in the destination memory.

0X9000_0048h Region of Interest Window Write to Memory Control Register LCD_WROI_W2MCON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	OUTPUT_ALPHA											ADDINC_DISABLE	DISCON	W2M_FORMAT		W2LCM
Type	R/W											R/W	R/W	R/W		R/W
Reset	0xff											0	0	0		0

This control register is effective only when the W2M bit is set in LCD_WROICON register.

W2LCM Write to LCM simultaneously. It is effective only when LCD_WROICON.W2M=1.

- **0** Not output to LCM, only write to memory.
- **1** Output to LCM and write to memory.

LCD_WROICON.W2M, LCD_WROI_W2MCON.W2LCM possible combinations

0x only output LCM

10 only output memory

11 output LCM and memory

W2M_FORMAT Write to memory format.

- **00** RGB565
- **01** RGB888
- **10** ARGB8888
- **11** Reserved

DISCON Block Write Enable Control. By setting both DISCON and W2M to 1, the LCD controller will write out the ROI pixel data as a part of MAIN window, using the width of MAIN window to calculate the write-out address. If this bit is not set, the ROI window will be written to memory in continuous addresses.

ADDINC_DISABLE Disable address increasing when writing to memory. Always write to the same address. It is only for debugging.

0X9000_0050h Region of Interest Window Control Register LCD_WROICON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN0	EN1	EN2	EN3				PERIOD								
Type	R/W	R/W	R/W	R/W				R/W								

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC	W2M	COM_SEL	COMMAND					FORMAT							
Type	R/W	R/W	R/W	R/W					R/W							

FORMAT LCD Module Data Format, see table 4.

Bit 0 : Sequence

0 BGR sequence.

1 RGB sequence.

Bit 1 : Significance.

Bit 2 : Padding.

0 Padding bits on LSBs.

1 Padding bits on MSBs.

Bit 5-3 : Color format

000 for RGB332, 001 for RGB444, 010 for RGB565, 011 for RGB666, 100 for RGB888.

Bit 7-6 : Interface width

00 for 8-bit interface, 10 for 9-bit interface, others reserved.

COM_SEL Command Queue ID Selection.

0 Send commands in command queue 0.

1 Send commands in command queue 1.

COMMAND Number of Commands to be sent to LCD module. Maximum is 31.

W2M Enable Write to Memory

ENC Command Transfer Enable Control.

0 Only send pixel data to LCM, not send commands in command queue.

1 Send commands in command queue first, and then send pixel data to LCM. The number of commands to be sent is specified by COMMAND, and the command queue to be sent is specified by COM_SEL.

PERIOD Waiting period between two consecutive transfers, effective for both data and command.

ENn Layer Window Enable Control

Note : If there are two pixels in one row, the pixel in blue is the prior one in scan direction, and the pixel in black is the later one. The scan direction is from left-top to right-bottom, and horizontal scan first.

format	I/F width	padding	significance	sequence	throughput (pixel/cycle)	output sequence
RGB332	8	x	x	0	1pixel/1cycle	$R_2R_1R_0G_2G_1G_0B_1B_0$
		x	x	1	1pixel/1cycle	$B_1B_0G_2G_1G_0R_2R_1R_0$
	9	x	x	0	1pixel/1cycle	$B_0R_2R_1R_0G_2G_1G_0B_1B_0$
		x	x	1	1pixel/1cycle	$R_0B_1B_0G_2G_1G_0R_2R_1R_0$

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format	I/F width	padding	significance	sequence	throughput (pixel/cycle)	output sequence
RGB444	8	x	0	0	2pixel/3cycle	$R_3R_2R_1R_0G_3G_2G_1G_0$ $B_3B_2B_1B_0R_3R_2R_1R_0$ $G_3G_2G_1G_0B_3B_2B_1B_0$
		x	0	1	2pixel/3cycle	$B_3B_2B_1B_0G_3G_2G_1G_0$ $R_3R_2R_1R_0B_3B_2B_1B_0$ $G_3G_2G_1G_0R_3R_2R_1R_0$
		x	1	0	2pixel/3cycle	$G_3G_2G_1G_0B_3B_2B_1B_0$ $B_3B_2B_1B_0R_3R_2R_1R_0$ $R_3R_2R_1R_0G_3G_2G_1G_0$
		x	1	1	2pixel/3cycle	$G_3G_2G_1G_0R_3R_2R_1R_0$ $R_3R_2R_1R_0B_3B_2B_1B_0$ $B_3B_2B_1B_0G_3G_2G_1G_0$
	9	x	0	0	2pixel/3cycle	$G_0R_3R_2R_1R_0G_3G_2G_1G_0$ $R_0B_3B_2B_1B_0R_3R_2R_1R_0$ $B_0G_3G_2G_1G_0B_3B_2B_1B_0$
		x	0	1	2pixel/3cycle	$G_0B_3B_2B_1B_0G_3G_2G_1G_0$ $B_0R_3R_2R_1R_0B_3B_2B_1B_0$ $R_0G_3G_2G_1G_0R_3R_2R_1R_0$
RGB444	9	x	1	0	2pixel/3cycle	$B_0G_3G_2G_1G_0B_3B_2B_1B_0$ $R_0B_3B_2B_1B_0R_3R_2R_1R_0$ $G_0R_3R_2R_1R_0G_3G_2G_1G_0$
		x	1	1	2pixel/3cycle	$R_0G_3G_2G_1G_0R_3R_2R_1R_0$ $B_0R_3R_2R_1R_0B_3B_2B_1B_0$ $G_0B_3B_2B_1B_0G_3G_2G_1G_0$
RGB565	8	x	0	0	1pixel/2cycle	$R_4R_3R_2R_1R_0G_5G_4G_3$ $G_2G_1G_0B_4B_3B_2B_1B_0$
		x	0	1	1pixel/2cycle	$B_4B_3B_2B_1B_0G_5G_4G_3$ $G_2G_1G_0R_4R_3R_2R_1R_0$

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format	I/F width	padding	significance	sequence	throughput (pixel/cycle)	output sequence
		x	1	0	1pixel/2cycle	$G_2G_1G_0B_4B_3B_2B_1B_0$ $R_4R_3R_2R_1R_0G_5G_4G_3$
		x	1	1	1pixel/2cycle	$G_2G_1G_0R_4R_3R_2R_1R_0$ $B_4B_3B_2B_1B_0G_5G_4G_3$
	9	x	0	0	1pixel/2cycle	$G_3R_4R_3R_2R_1R_0G_5G_4G_3$ $B_0G_2G_1G_0B_4B_3B_2B_1B_0$
		x	0	1	1pixel/2cycle	$G_3B_4B_3B_2B_1B_0G_5G_4G_3$ $R_0G_2G_1G_0R_4R_3R_2R_1R_0$
		x	1	0	1pixel/2cycle	$B_0G_2G_1G_0B_4B_3B_2B_1B_0$ $G_3R_4R_3R_2R_1R_0G_5G_4G_3$
		x	1	1	1pixel/2cycle	$R_0G_2G_1G_0R_4R_3R_2R_1R_0$ $G_3B_4B_3B_2B_1B_0G_5G_4G_3$
RGB666	8	0	0	0	1pixel/3cycle	$R_5R_4R_3R_2R_1R_0$xx $G_5G_4G_3G_2G_1G_0$xx $B_5B_4B_3B_2B_1B_0$xx
		0	0	1	1pixel/3cycle	$B_5B_4B_3B_2B_1B_0$xx $G_5G_4G_3G_2G_1G_0$xx $R_5R_4R_3R_2R_1R_0$xx
		0	1	0	1pixel/3cycle	$B_5B_4B_3B_2B_1B_0$xx $G_5G_4G_3G_2G_1G_0$xx $R_5R_4R_3R_2R_1R_0$xx
RGB666	8	0	1	1	1pixel/3cycle	$R_5R_4R_3R_2R_1R_0$xx $G_5G_4G_3G_2G_1G_0$xx $B_5B_4B_3B_2B_1B_0$xx
		1	0	0	1pixel/3cycle	xx$R_5R_4R_3R_2R_1R_0$ xx$G_5G_4G_3G_2G_1G_0$ xx$B_5B_4B_3B_2B_1B_0$

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format	I/F width	padding	significance	sequence	throughput (pixel/cycle)	output sequence
		1	0	1	1pixel/3cycle	$xxB_5B_4B_3B_2B_1B_0$ $xxG_5G_4G_3G_2G_1G_0$ $xxR_5R_4R_3R_2R_1R_0$
		1	1	0	1pixel/3cycle	$xxB_5B_4B_3B_2B_1B_0$ $xxG_5G_4G_3G_2G_1G_0$ $xxR_5R_4R_3R_2R_1R_0$
		1	1	1	1pixel/3cycle	$xxR_5R_4R_3R_2R_1R_0$ $xxG_5G_4G_3G_2G_1G_0$ $xxB_5B_4B_3B_2B_1B_0$
	9	x	0	0	1pixel/2cycle	$R_5R_4R_3R_2R_1R_0G_5G_4G_3$ $G_2G_1G_0B_5B_4B_3B_2B_1B_0$
		x	0	1	1pixel/2cycle	$B_5B_4B_3B_2B_1B_0G_5G_4G_3$ $G_2G_1G_0R_5R_4R_3R_2R_1R_0$
		x	1	0	1pixel/2cycle	$G_2G_1G_0B_5B_4B_3B_2B_1B_0$ $R_5R_4R_3R_2R_1R_0G_5G_4G_3$
		x	1	1	1pixel/2cycle	$G_2G_1G_0R_5R_4R_3R_2R_1R_0$ $B_5B_4B_3B_2B_1B_0G_5G_4G_3$
RGB888	8	x	0	0	1pixel/3cycle	$R_7R_6R_5R_4R_3R_2R_1R_0$ $G_7G_6G_5G_4G_3G_2G_1G_0$ $B_7B_6B_5B_4B_3B_2B_1B_0$
		x	0	1	1pixel/3cycle	$B_7B_6B_5B_4B_3B_2B_1B_0$ $G_7G_6G_5G_4G_3G_2G_1G_0$ $R_7R_6R_5R_4R_3R_2R_1R_0$
		x	1	0	1pixel/3cycle	$B_7B_6B_5B_4B_3B_2B_1B_0$ $G_7G_6G_5G_4G_3G_2G_1G_0$ $R_7R_6R_5R_4R_3R_2R_1R_0$

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format	I/F width	padding	significance	sequence	throughput (pixel/cycle)	output sequence
RGB888	8	x	1	1	1pixel/3cycle	$R_7R_6R_5R_4R_3R_2R_1R_0$ $G_7G_6G_5G_4G_3G_2G_1G_0$ $B_7B_6B_5B_4B_3B_2B_1B_0$
	9	x	0	0	1pixel/3cycle	$R_0R_7R_6R_5R_4R_3R_2R_1R_0$ $G_0G_7G_6G_5G_4G_3G_2G_1G_0$ $B_0B_7B_6B_5B_4B_3B_2B_1B_0$
		x	0	1	1pixel/3cycle	$B_0B_7B_6B_5B_4B_3B_2B_1B_0$ $G_0G_7G_6G_5G_4G_3G_2G_1G_0$ $R_0R_7R_6R_5R_4R_3R_2R_1R_0$
		x	1	0	1pixel/3cycle	$B_0B_7B_6B_5B_4B_3B_2B_1B_0$ $G_0G_7G_6G_5G_4G_3G_2G_1G_0$ $R_0R_7R_6R_5R_4R_3R_2R_1R_0$
		x	1	1	1pixel/3cycle	$R_0R_7R_6R_5R_4R_3R_2R_1R_0$ $G_0G_7G_6G_5G_4G_3G_2G_1G_0$ $B_0B_7B_6B_5B_4B_3B_2B_1B_0$

Table 45 WROICON.FORMAT List

Blue color indicates the prior pixel in scan direction, and black color means the later pixel. The scan direction is from left-top to right-bottom, horizontal scan first.

The skin color means the dummy bit of 9 bit interface.

0X9000_0054h Region of Interest Window Offset Register LCD_WROIOFS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							Y-OFFSET									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							X-OFFSET									
Type							R/W									

X-OFFSET ROI Window Column Offset
Y-OFFSET ROI Window Row Offset

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0X9000_0058h Region of Interest Window Command Start Address Register LCD_WROICADD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADDR															
Type	R/W															

ADDR ROI Window Command Address. Specify the address that the commands will be sent to. Only four possible values are allowed.

- **4100h** Commands are sent to LCD parallel interface 0 and LPA0 will be set to 1.
- **5100h** Commands are sent to LCD parallel interface 1 and LPA0 will be set to 1.
- **9100h** Commands are sent to LCD serial interface 0 and LPA0 will be set to 1.
- **8100h** Commands are sent to LCD serial interface 1 and LPA0 will be set to 1.

0X9000_005Ch Region of Interest Window Data Start Address Register LCD_WROIDADD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADDR															
Type	R/W															

ADDR ROI Window Data Address. Specify the address that the data will be sent to. Only five possible values are allowed.

- **4000h** Data are sent to LCD parallel interface 0 and LPA0 will be set to 0.
- **5000h** Data are sent to LCD parallel interface 1 and LPA0 will be set to 0.
- **6000h** Data are sent to LCD parallel interface 2 and LPA0 will be set to 0.
- **9000h** Data are sent to LCD serial interface 0 and LPA0 will be set to 0.
- **8000h** Data are sent to LCD serial interface 1 and LPA0 will be set to 0.

0X9000_0060h Region of Interest Window Size Register LCD_WROISIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ROW									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							COLUMN									
Type							R/W									

COLUMN ROI Window Column Size in unit of pixel

ROW ROI Window Row Size in unit of pixel

0X9000_0064h Region of Interest Window Hardware Refresh Register LCD_WROI_HWREF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN0	EN1	EN2	EN3											HWREF_SEL	
Type	R/W	R/W	R/W	R/W											R/W	
Reset	0	0	0	0											0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	MISSED_HWTRIG_CNT				CLR_MISSED_CNT				HWEN							HWREF
Type	RO	RO	RO	RO	R/W				R/W							R/W
Reset	0	0	0	0	0				0							0

When hardware trigger mode is enabled, LCD controller will start to update a frame when triggered by the module specified by HWREF_SEL. It also uses the address from the same module as layer's base address.

HWREF Starting the hardware triggered LCD frame transfer.

HWEN Enable hardware triggered LCD fresh.

CLR_MISSED_CNT Clear MISSED_HWTRIG_CNT

MISSED_HWTRIG_CNT Missed hardware trigger counter. This counter increases when hardware trigger comes and LCD is not at the state waiting for it.

HWREF_SEL Select hardware triggered source.

- **00** triggered by resizer
- **01** reserved.
- **10** reserved.
- **11** reserved.

EN*n* Enable layer n source address from the module specified by HWREF_SEL.

0X9000_0068h Region of Interest Window Direct Couple Register LCD_WROI_DC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN0	EN1	EN2	EN3												
Type	R/W	R/W	R/W	R/W												
Reset	0	0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DC_SEL0		DC_SEL1		DC_SEL2		DC_SEL3									
Type	R/W		R/W		R/W		R/W									
Reset	0		0		0		0									

EN*n* Enable layer n source data from other module.

DC_SELn Select source layer n data.

- **00** reserved
- **01** Resizer
- **10** reserved
- **11** reserved

Note : When direct couple is enabled on multiple layers, the source data of each layer should be different.

0X9000_006Ch Region of Interest Background Color Register LCD_WROI_BGCLR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									RED[7:0]							
Type									R/W							
Reset									1111_1111							

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN[7:0]								BLUE[7:0]							
Type	R/W								R/W							
Reset	1111_1111								1111_1111							

RED Red component of ROI window's background color
GREEN Green component of ROI window's background color
BLUE Blue component of ROI window's background color

0X9000_0070h Layer 0 Window Control Register LCD_L0WINCON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														IRT_EN	SCRL_EN	SWP
Type														R/W	R/W	R/W
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC	KEYEN	ROTATE			CLRDPT		OPAEN	OPA							
Type	R/W	R/W	R/W			R/W		R/W	R/W							

OPA Opacity value, used as constant alpha value.
OPAEN Opacity enabled
CLRDPT Color format
- **00** 8bpp indexed color.
- **01** RGB 565
- **10** ARGB 8888
- **11** RGB 888

ROTATE Rotation Configuration
- **000** 0 degree rotation
- **001** 90 degree rotation counterclockwise
- **010** 180 degree rotation counterclockwise
- **011** 270 degree rotation counterclockwise
- **100** Horizontal flip
- **101** Horizontal flip then 90 degree rotation counterclockwise
- **110** Horizontal flip then 180 degree rotation counterclockwise
- **111** Horizontal flip then 270 degree rotation counterclockwise

KEYEN Source Key Enable Control
SRC Disable auto-increment of the source pixel address
SWP Swap high byte and low byte of pixel data
SCRL_EN Enable scroll effect
IRT_EN Using internal image rotator to do rotation

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0X9000_0074h Layer 0 Source Color Key Register LCD_L0WINSKEY

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY[31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRCKEY[15:0]															
Type	R/W															

SRCKEY Transparent color key of the source image. The effect bits number is the same of the color depth of this layer. That is, if color depth is 8bpp index color, the effect bits are SRCKEY[7:0]. If color depth is RGB565, the effect bits are SRCKEY[15:0], etc.

0X9000_0078h Layer 0 Window Display Offset Register LCD_L0WINOFS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							Y-OFFSET									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							X-OFFSET									
Type							R/W									

Y-OFFSET Layer 0 Window Row Offset in unit of pixel opposite to the zero point of ROI coordinate system.
X-OFFSET Layer 0 Window Column Offset in unit of pixel opposite to the zero point of ROI coordinate system.

LCD+007Ch Layer 0 Window Display Start Address Register LCD_L0WINADD

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADDR															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADDR															
Type	R/W															

ADDR Layer 0 Window Data Address.

0X9000_0080h Layer 0 Window Size LCD_L0WINSIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ROW									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							COLUMN									
Type							R/W									

ROW Layer 0 Window Row Size in unit of pixel.
COLUMN Layer 0 Window Column Size in unit of pixel.

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0X9000_0084h Layer 0 Scroll Start Offset LCD_L0WINSCRL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							Y-OFFSET									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							X-OFFSET									
Type							R/W									

Y-OFFSET Layer 0 Scroll Start Row Offset in unit of pixel, its value must satisfy Y-OFFSET < LCD_L0WINSIZE.ROW

X-OFFSET Layer 0 Scroll Start Column Offset in unit of pixel, its value must satisfy X-OFFSET < LCD_L0WINSIZE.COLUMN

0X9000_0090h Layer 1 Window Control Register LCD_L1WINCON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														IRT_EN	SCRL_EN	SWP
Type														R/W	R/W	R/W
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC	KEYEN	ROTATE			CLRDPT		OPAEN	OPA							
Type	R/W	R/W	R/W			R/W		R/W	R/W							

OPA Opacity value, used as constant alpha value.

OPAEN Opacity enabled

CLRDPT Color format

- **00** 8bpp indexed color.
- **01** RGB 565
- **10** ARGB 8888
- **11** RGB 888

ROTATE Rotation Configuration

- **000** 0 degree rotation
- **001** 90 degree rotation counterclockwise
- **010** 180 degree rotation counterclockwise
- **011** 270 degree rotation counterclockwise
- **100** Horizontal flip
- **101** Horizontal flip then 90 degree rotation counterclockwise
- **110** Horizontal flip then 180 degree rotation counterclockwise
- **111** Horizontal flip then 270 degree rotation counterclockwise

KEYEN Source Key Enable Control

SRC Disable auto-increment of the source pixel address

SWP Swap high byte and low byte of pixel data

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SCRL_EN Enable scroll effect

IRT_EN Using internal image rotator to do rotation

0X9000_0094h Layer 1 Source Color Key Register LCD_L1WINSKEY

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY[31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRCKEY[15:0]															
Type	R/W															

SRCKEY Transparent color key of the source image. The effect bits number is the same of the color depth of this layer. That is, if color depth is 8bpp index color, the effect bits are SRCKEY[7:0]. If color depth is RGB565, the effect bits are SRCKEY[15:0], etc.

0X9000_0098h Layer 1 Window Display Offset Register LCD_L1WINOFS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							Y-OFFSET									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							X-OFFSET									
Type							R/W									

Y-OFFSET Layer 1 Window Row Offset in unit of pixel opposite to the zero point of ROI coordinate system.

X-OFFSET Layer 1 Window Column Offset in unit of pixel opposite to the zero point of ROI coordinate system.

LCD+009Ch Layer 1 Window Display Start Address Register LCD_L1WINADD

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADDR															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADDR															
Type	R/W															

ADDR Layer 1 Window Data Address.

0X9000_00A0h Layer 1 Window Size LCD_L1WINSIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ROW									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							COLUMN									
Type							R/W									

ROW Layer 1 Window Row Size in unit of pixel

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COLUMN Layer 1 Window Column Size in unit of pixel

0X9000_00A4h Layer 1 Scroll Start Offset LCD_L1WINSCRL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							Y-OFFSET									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							X-OFFSET									
Type							R/W									

Y-OFFSET Layer 1 Scroll Start Row Offset in unit of pixel, its value must satisfy Y-OFFSET < LCD_L1WINSIZE.ROW

X-OFFSET Layer 1 Scroll Start Column Offset in unit of pixel, its value must satisfy X-OFFSET < LCD_L1WINSIZE.COLUMN

0X9000_00B0h Layer 2 Window Control Register LCD_L2WINCON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														IRT_EN	SCRL_EN	SWP
Type														R/W	R/W	R/W
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC	KEYEN	ROTATE			CLRDPT		OPAEN	OPA							
Type	R/W	R/W	R/W			R/W		R/W	R/W							

OPA Opacity value, used as constant alpha value.

OPAEN Opacity enabled

CLRDPT Color format

- **00** 8bpp indexed color.
- **01** RGB 565
- **10** ARGB 8888
- **11** RGB 888

ROTATE Rotation Configuration

- **000** 0 degree rotation
- **001** 90 degree rotation counterclockwise
- **010** 180 degree rotation counterclockwise
- **011** 270 degree rotation counterclockwise
- **100** Horizontal flip
- **101** Horizontal flip then 90 degree rotation counterclockwise
- **110** Horizontal flip then 180 degree rotation counterclockwise
- **111** Horizontal flip then 270 degree rotation counterclockwise

KEYEN Source Key Enable Control

SRC Disable auto-increment of the source pixel address

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SWP Swap high byte and low byte of pixel data
SCRL_EN Enable scroll effect
IRT_EN Using internal image rotator to do rotation

0X9000_00B4h Layer 2 Source Color Key Register LCD_L2WINSKEY

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY[31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRCKEY[15:0]															
Type	R/W															

SRCKEY Transparent color key of the source image. The effect bits number is the same of the color depth of this layer. That is, if color depth is 8bpp index color, the effect bits are SRCKEY[7:0]. If color depth is RGB565, the effect bits are SRCKEY[15:0], etc.

0X9000_00B8h Layer 2 Window Display Offset Register LCD_L2WINOFS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							Y-OFFSET									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							X-OFFSET									
Type							R/W									

Y-OFFSET Layer 2 Window Row Offset in unit of pixel opposite to the zero point of ROI coordinate system.
X-OFFSET Layer 2 Window Column Offset in unit of pixel opposite to the zero point of ROI coordinate system.

LCD+00BCh Layer 2 Window Display Start Address Register LCD_L2WINADD

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADDR															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADDR															
Type	R/W															

ADDR Layer 2 Window Data Address.

0X9000_00C0h Layer 2 Window Size LCD_L2WINSIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ROW									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							COLUMN									
Type							R/W									

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ROW Layer 2 Window Row Size in unit of pixel
COLUMN Layer 2 Window Column Size in unit of pixel

0X9000_00C4h Layer 2 Scroll Start Offset LCD_L2WINSCRL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							Y-OFFSET									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							X-OFFSET									
Type							R/W									

Y-OFFSET Layer 2 Scroll Start Row Offset in unit of pixel, its value must satisfy Y-OFFSET < LCD_L2WINSIZE.ROW
X-OFFSET Layer 2 Scroll Start Column Offset in unit of pixel, its value must satisfy X-OFFSET < LCD_L2WINSIZE.COLUMN

0X9000_00D0h Layer 3 Window Control Register LCD_L3WINCON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														IRT_EN	SCRL_EN	SWP
Type														R/W	R/W	R/W
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC	KEYEN	ROTATE			CLRDPT		OPAEN	OPA							
Type	R/W	R/W	R/W			R/W		R/W	R/W							

OPA Opacity value, used as constant alpha value.
OPAEN Opacity enabled
CLRDPT Color format
- **00** 8bpp indexed color.
- **01** RGB 565
- **10** ARGB 8888
- **11** RGB 888

ROTATE Rotation Configuration
- **000** 0 degree rotation
- **001** 90 degree rotation counterclockwise
- **010** 180 degree rotation counterclockwise
- **011** 270 degree rotation counterclockwise
- **100** Horizontal flip
- **101** Horizontal flip then 90 degree rotation counterclockwise
- **110** Horizontal flip then 180 degree rotation counterclockwise
- **111** Horizontal flip then 270 degree rotation counterclockwise

KEYEN Source Key Enable Control

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SRC Disable auto-increment of the source pixel address
SWP Swap high byte and low byte of pixel data
SCRL_EN Enable scroll effect
IRT_EN Using internal image rotator to do rotation

0X9000_00D4h Layer 3 Source Color Key Register — LCD_L3WINSKEY

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY[31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRCKEY[15:0]															
Type	R/W															

SRCKEY Transparent color key of the source image. The effect bits number is the same of the color depth of this layer. That is, if color depth is 8bpp index color, the effect bits are SRCKEY[7:0]. If color depth is RGB565, the effect bits are SRCKEY[15:0], etc.

0X9000_00D8h Layer 3 Window Display Offset Register — LCD_L3WINOFS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							Y-OFFSET									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							X-OFFSET									
Type							R/W									

Y-OFFSET Layer 3 Window Row Offset in unit of pixel opposite to the zero point of ROI coordinate system.
X-OFFSET Layer 3 Window Column Offset in unit of pixel opposite to the zero point of ROI coordinate system.

LCD+00DCh Layer 3 Window Display Start Address Register — LCD_L3WINADD

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADDR															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADDR															
Type	R/W															

ADDR Layer 3 Window Data Address.

0X9000_00E0h Layer 3 Window Size — LCD_L3WINSIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ROW									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							COLUMN									
Type							R/W									

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ROW Layer 3 Window Row Size in unit of pixel.

COLUMN Layer 3 Window Column Size in unit of pixel.

0X9000_00E4h Layer 3 Scroll Start Offset — LCD_L3WINSCRL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							Y-OFFSET									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							X-OFFSET									
Type							R/W									

Y-OFFSET Layer 3 Scroll Start Row Offset in unit of pixel, its value must satisfy Y-OFFSET < LCD_L3WINSIZE.ROW

X-OFFSET Layer 3 Scroll Start Column Offset in unit of pixel, its value must satisfy X-OFFSET < LCD_L3WINSIZE.COLUMN

0X9000_0300h Image Rotator DMA GMC Port Control Register — LCD_IRT_GMCCON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	THROTTLE_PERIOD															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												THROTTLE_EN			MAX_BURST	
Type												R/W			R/W	R/W
Reset												0			1	0

MAX_BURST Specify the maximum burst length of GMC request.

- **00** Single 4 bytes access
- **01** Burst 4 beats access, and one beat is 2 bytes. Total data amount is 8 bytes per access.
- **10** Burst 4 beats access, and one beat is 4 bytes. Total data amount is 16 bytes per access.
- **11** Burst 4 beats access, and one beat is 4 bytes. Total data amount is 16 bytes per access.

THROTTLE_EN Enable GMC port throttling.

THROTTLE_PERIOD Throttle down LCD GMC port access speed. It specifies how many AHB bus cycles between two GMC requests. There is a down counter, throttle_cnt, to count down for the interval between two GMC requests. It counts from THROTTLE_PERIOD when lcd_greq rising to zero, and the next GMC request is allowed to issue when throttle_cnt=0. Please see **Figure 59**. The maximum GMC bandwidth is limited to

$$\frac{bytes_per_GMC_access \times 1000}{throttle_period \times AHB_cycle_time(ns)} = \frac{bytes_per_GMC_access \times 1000}{throttle_period \times 19.2(ns)} \text{MBytes/sec}$$

Bytes_per_GMC_access is specified by MAX_BURST.

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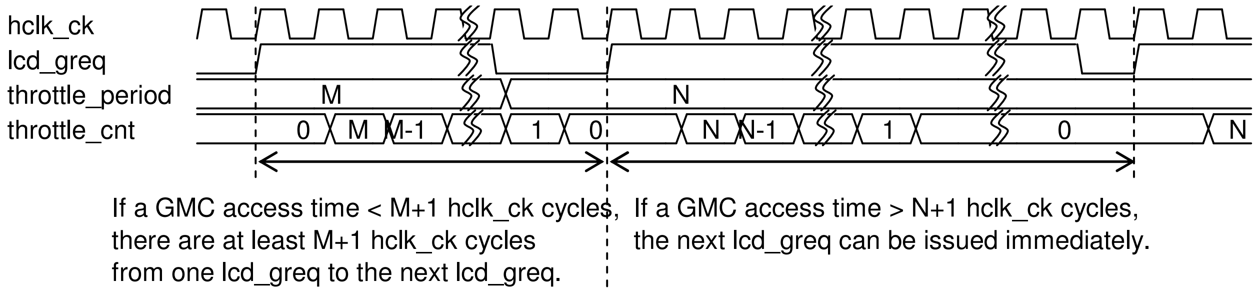

Figure 59 GMC throttle mechanism

0X9000_0304h Image Rotator DMA FIFO Base Address Register — LCD_IRT_FIFO_BASE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRT_FIFO_BASE															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRT_FIFO_BASE															
Type	R/W															

IRT_FIFO_BASE:

Base address of IRT line buffer. ***It should align at 4x address***, or IRT will read/write wrong data. Besides, it should be set in the internal memory to get better performance.

It should place IRT line buffer and SW code in different bank to get better performance. And if possible, place IRT line buffer and Resizer line buffer in different bank too.

0X9000_0308h Image Rotator DMA FIFO Length Register — LCD_IRT_FIFO_LEN

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRT_FIFO_LEN															
Type	R/W															

IRT_FIFO_LEN:

IRT FIFO Length. It must be the multiple of 8, and recommended values are at least 16 to support double buffer.

Note:

When rotation is 90° or 270° :

FIFO_SIZE in internal SYSRAM = layer_source_height (before rotation) * 2 * IRT_FIFO_LEN

When rotation is 0° or 180° :

FIFO_SIZE in internal SYSRAM = 0

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0X9000_030Ch Image Rotator DMA Write FIFO Horizontal Count Register LCD_IRT_WR_CNT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							IRT_WR_YCNT									
Type							RO									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							IRT_WR_XCNT									
Type							RO									

IRT_WR_XCNT:

Horizontal pixel count of input image that IRT WRINT (write internal) is now processing. It is a 10-bit up counter.

Note:

When rotation is 0° or 180° :

If its value is C, then it represents IRT WRINT now processes (C+1)th pixel of a line of the input image. It will be increased by 1 each time a pixel is processed. While it counts to (IRT_XSIZE – 1) and a pixel is processed, it will be reset to 0.

When rotation is 90° or 270° :

If its value is C, then it represents IRT WDMA now at (C+1) th ~ (C+8) th column of the input image. It will be increased by 8 while all data in a segment (8 columns) are written into FIFO, i.e., IRT_WR_XCNT counts to (IRT_YSIZE – 1) and FIFO written is completed.

IRT_WR_YCNT:

Vertical line count of input image that IRT WRINT is now processing. It is a 10-bit up counter.

Note 1:

When rotation is 0° or 180° :

If its value is C, then it represents IRT WRINT is now at (C+1)th line of the input image. It will be increased by 1 each time IRT_WR_XCNT counts to (IRT_XSIZE – 1) and a pixel is processed.

When rotation is 90° or 270° :

If its value is C, then it represents IRT2 WDMA now at (C+1) th line of the input image. It will be increase by 1 each time 8 pixels are written into FIFO. And it would be reset 0 each time it counts to (IRT_YSIZE – 1) and 8-pixels write are finished.

Note 2:

When IRT DMA starts:

(IRT_WR_XCNT, IRT2_WR_YCNT) = (0, 0);

When IRT DMA finishes:

When rotation is 0° or 180° :

(IRT2_WR_XCNT, IRT_WR_YCNT) = (0, IRT_YSIZE);

When rotation is 90° or 270° :

PAD_IRT_XSIZE_8X = (IRT_XSIZE + 8)>>3) << 3;

(IRT_WR_XCNT, IRT_WR_YCNT) = (PAD_IRT_XSIZE_8X, 0);

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0X9000_0310h Image Rotator DMA Read FIFO Horizontal Count Register LCD_IRT_RD_CNT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							IRT_RD_YCNT									
Type							RO									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							IRT_RD_XCNT									
Type							RO									

IRT_RD_XCNT:

Horizontal pixel count of input image that IRT RDINT (read internal) is now transmitted. It is a 10-bit up counter.

Note:

When rotation is 0° or 180° :

If its value is C, then it represents IRT RDINT now processes (C+1)th pixel of a line of the input image. It will be increased by 1 each time a pixel is processed. While it counts to (IRT_XSIZE – 1) and a pixel is transmitted out, it will be reset to 0.

When rotation is 90° or 270° :

If its value is C, then it represents IRT RDINT now at (C+1)th column of the input image. It will be increased by 1 while IRT_RD_YCNT counts to (IRT_YSIZE – 1) and a pixel is transmitted out.

IRT_RD_YCNT:

Vertical line count of input image that IRT RDINT is now at. It is a 10-bit up counter.

Note 1:

When rotation is 0° or 180° :

If its value is C, then it represents IRT2 RDINT now at (C+1)th line of the input image. It will be increased by 1 each time IRT_RD_XCNT counts to (IRT_XSIZE – 1) and a pixel is transmitted out.

When rotation is 90° or 270° :

If its value is C, then it represents IRT2 RDINT now at (C+1)th column of the input image. It will be increased by 1 each time IRT_RD_YCNT counts to (IRT_YSIZE – 1) and a pixel is transmitted out.

Note 2:

When IRT DMA starts:

(IRT_RD_XCNT, IRT_RD_YCNT) = (0, 0);

When IRT DMA finishes:

When rotation is 0° or 180° :

(IRT_RD_XCNT, IRT_RD_YCNT) = (0, IRT_YSIZE);

When rotation is 90° or 270° :

(IRT_RD_XCNT, IRT_RD_YCNT) = (IRT_XSIZE, 0);

0X9000_0314h Image Rotator DMA FIFO Line Count Register LCD_IRT_FIFO_LINE_CNT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							IRT_FIFO_LINE_CNT									
Type							RO									

IRT_FIFO_LINE_CNT:

Display how many lines are stored in FIFO now. It could count up or count down.

Count up:

Each time data of a segment (8 lines) are written into FIFO, it will increased by 8.

Count down:

Each time data of a segment (8 lines) are read out of FIFO, it will decreased by 8.

0X9000_0318h Image Rotator DMA Write FIFO Line Index Register LCD_IRT_ YIDX

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							IRT_RD_YIDX									
Type							RO									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							IRT_WR_YIDX									
Type							RO									

IRT_WR_YIDX:

Display which FIFO line IRT WRINT is now writing.

Note:

It will be increased by 8 each time data of a segment (8 lines) are written. When its value is equal to IRT_FIFO_YLEN (at the bottom of the FIFO) and the current segment data are written into FIFO, it will be reset to 8 to acknowledge IRT WRINT to write to top of the FIFO again.

IRT_RD_YIDX:

Display which FIFO line IRT RDINT is now reading. It will be increased by 1 each time a line data are read out of the FIFO. When its value is equal to IRT_FIFO_YLEN (at the bottom of the FIFO) and the current line data are read out of the FIFO, it will be reset to 1 to acknowledge IRT RDINT to read from the top the FIFO again.

0X9000_0320h Image Rotator DMA Frame Base Address LCD_FRAME_BASE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FRAME_BASE[31:16]															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FRAME_BASE[15:0]															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

FRAM_BASE The base address of the intersection part of the rotated layer and ROI. See **Figure 60**.

0X9000_0324h Image Rotator DMA Size LCD_IRT_SIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name							ROW									
Type							RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							COL									
Type							RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

COL The column size of the intersection part of the rotated layer and ROI.

ROW The row size of the intersection part of the rotated layer and ROI. See figure 10.

0X9000_0328h Image Rotator DMA Background X Size LCD_IRT_BKGD_XSIZE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							COLUMN									
Type							RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

COL The original column size of the rotated layer. See figure 10.

0X9000_032Ch Image Rotator DMA Clip Pixel Number LCD_IRT_CLIP_PXLNUM

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CLIP_PXLNUM[19:16]			
Type													RO	RO	RO	RO
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLIP_PXLNUM[15:0]															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

CLIP_PXLNUM This value should be equal to LCD_IRT_BKGD_XSIZE.COLUMN * LCD_IRT_SIZE.ROW

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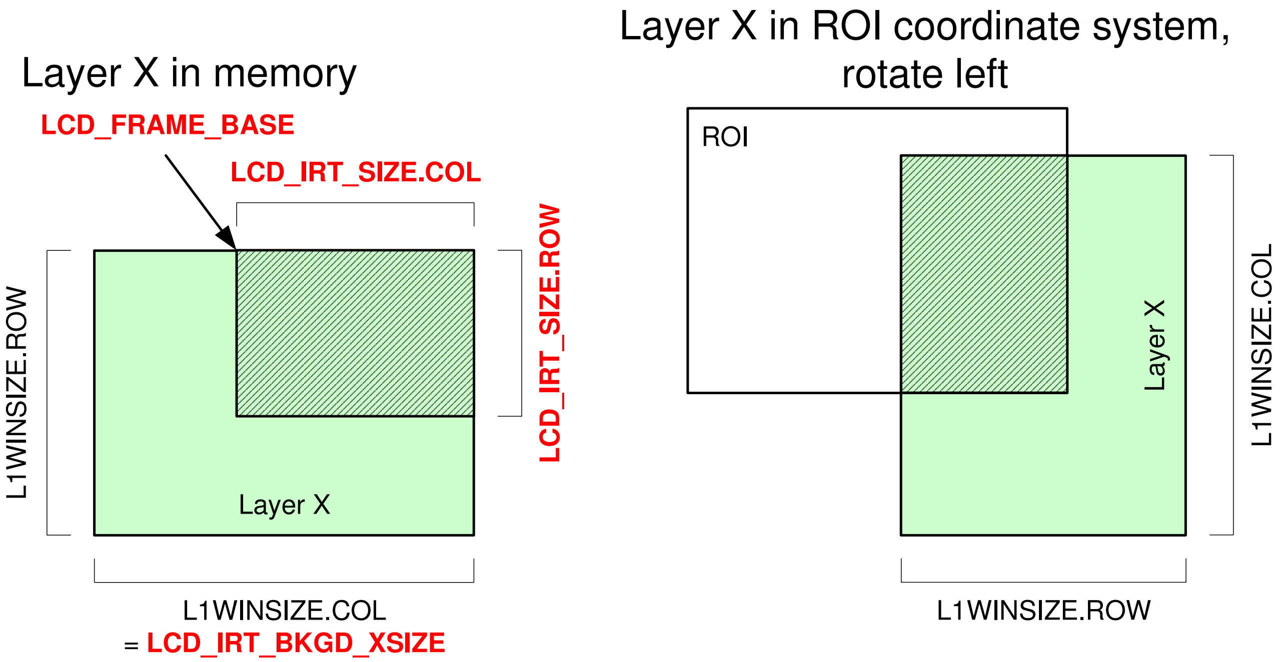

Figure 60 The parameters (red words) of the intersection part of the rotated layer and ROI

0X9000_4000h LCD Parallel 0 Interface Data Port — LCD_PDAT0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA[31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA[15:0]															
Type	R/W															

DATA LCD parallel 0 data interface is mapped to this address. Read from/Write to this address will assert LCD parallel 0 chips select, and LPA0=0.

0X9000_4100h LCD Parallel 0 Interface Command Port — LCD_PCMD0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMD[31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMD[15:0]															
Type	R/W															

CMD LCD parallel 0 command interface is mapped to this address. Read from/Write to this address will assert LCD parallel 0 chips select, and LPA0=1.

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0X9000_5000h LCD Parallel 1 Interface Data LCD_PDAT1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA[31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA[15:0]															
Type	R/W															

DATA LCD parallel 1 data interface is mapped to this address. Read from/Write to this address will assert LCD parallel 1 chips select, and LPA0=0.

0X9000_5100h LCD Parallel 1 Interface Command Port LCD_PCMD1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMD[31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMD[15:0]															
Type	R/W															

CMD LCD parallel 1 command interface is mapped to this address. Read from/Write to this address will assert LCD parallel 1 chips select, and LPA0=1.

Parallel I/F data width (bits)	AHB write transaction size (bits)	data sequence in parallel I/F
8	8	hwdata[7:0]
	16	hwdata[7:0] hwdata[15:8]
	32	hwdata[7:0] hwdata[15:8] hwdata[23:16] hwdata[31:24]
9	8	hwdata[8:0]
	16	hwdata[8:0]
	32	hwdata[8:0] hwdata[24:16]
16	8	hwdata[15:0]
	16	hwdata[15:0]

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	32	hwdata[15:0] hwdata[31:16]
18	8	hwdata[17:0]
	16	hwdata[17:0]
	32	hwdata[17:0]

Table 46 Parallel interface transmission sequence when MCU directly writes LCD_PDAT* or LCD_PCMD*.

0X9000_8000h LCD Serial 1 Interface Data LCD_SDAT1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA[31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA[15:0]															
Type	R/W															

DATA LCD serial 1 data interface is mapped to this address. Write to this address will assert LCD serial 1 chips select, and LSA0=0 in 4-wire mode or A0 bit=0 in 3-wire mode.

0X9000_8100h LCD Serial 1 Interface Command Port LCD_SCMD1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMD[31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMD[15:0]															
Type	R/W															

CMD LCD serial 1 command interface is mapped to this address. Write to this address will assert LCD serial 1 chips select, and LSA0=1 in 4-wire mode or A0 bit=1 in 3-wire mode.

0X9000_9000h LCD Serial 0 Interface Data Port LCD_SDAT0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA[31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA[15:0]															
Type	R/W															

DATA LCD serial 0 data interface is mapped to this address. Write to this address will assert LCD serial 0 chips select, and LSA0=0 in 4-wire mode or A0 bit=0 in 3-wire mode.

0X9000_9100h LCD Serial 0 Interface Command Port LCD_SCMD0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMD[31:16]															

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Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMD[15:0]															
Type	R/W															

CMD LCD serial 0 command interface is mapped to this address. Write to this address will assert LCD serial 0 chips select, and and LSA0=1 in 4-wire mode or A0 bit=1 in 3-wire mode.

LCD_SCNF.NON_DBI	LCD_SCNF.3_WIRE	AHB write transaction size (bits)	data sequence in serial I/F
0	0	8	hwdata[7:0]
		16	hwdata[7:0]
		32	hwdata[7:0]
	1	8	{cmd_data, hwdata[7:0]}
		16	{cmd_data, hwdata[7:0]}
		32	{cmd_data, hwdata[7:0]}
1	0	8	hwdata[7:0]
		16	hwdata[15:0]
		32	hwdata[31:0]
	1	8	{cmd_data, hwdata[7:0]}
		16	{cmd_data, hwdata[15:0]}
		32	{cmd_data, hwdata[31:0]}

Table 47 Serial interface transmission sequence when MCU directly writes LCD_SDAT0, LCD_SCMD0, LCD_SDAT1 or LCD_SCMD1.

Serial transmission starts from the MSB of "data sequence in serial I/F". “cmd_data” is the command/data indicator, 1 for command and 0 for data. If MCU writes the command port, cmd_data=1. If MCU writes the data port, cmd_data=0.

0X9000_C000h~C3FFh LCD Interface Color Palette LUT Registers LCD_PAL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															R[7:6]	
Type															R/W	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R[5:2]				G[7:2]						B[7:2]					
Type	R/W				R/W						R/W					

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The Color Palette is RGB666 format. And its output will add two bits “0” in LSB to form RGB888 format, so the output is {R[7:2], 2’b0, G[7:2], 2’b0, B[7:2], 2’b0}.

0X9000_C400h~C4FFh LCD Interface Gamma Correction LUT Registers LCD_GAMMA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															GAMMA_LUT 2[7:6]	
Type															R/W	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAMMA_LUT 2[5:2]				GAMMA_LUT 1[7:2]						GAMMA_LUT0[7:2]					
Type	R/W				R/W						R/W					

GAMMA_LUT0 These Bits Set Gamma LUT 0.
GAMMA_LUT1 These Bits Set Gamma LUT 1.
GAMMA_LUT2 These Bits Set Gamma LUT 2.
The gamma correction LUT output will add two bits “0” in LSB to from RGB888 format.

0X9000_C500h~C57F LCD Interface Command/Parameter0 Registers LCD_COMD0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															C0	
Type															R/W	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMM[15:0]															
Type	R/W															

COMM Command Data and Parameter Data for LCD Module
C0 Write to ROI Command Address if C0 = 1, otherwise write to ROI Data Address

0X9000_C580h~C5FF LCD Interface Command/Parameter1 Registers LCD_COMD1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															C0	
Type															R/W	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMM[15:0]															
Type	R/W															

COMM Command Data and Parameter Data for LCD Module
C0 Write to ROI Command Address if C0 = 1, otherwise write to ROI Data Address

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6.2 Image Resizer

6.2.1 General Description

This block provides the image resizing function for image and video capturing scenarios. It receives image data from the ISP module or from memory input, performs the image resizing function and outputs either RGB565 or YUV420 to the GMC module. Another output path is direct couple to LCD. **Figure 61** shows the block diagram. The resizer is composed of horizontal and vertical resizing blocks. It can scale up or down the input image by any ratio. However, the maximum sizes of input and output images are limited to 1600x1200.

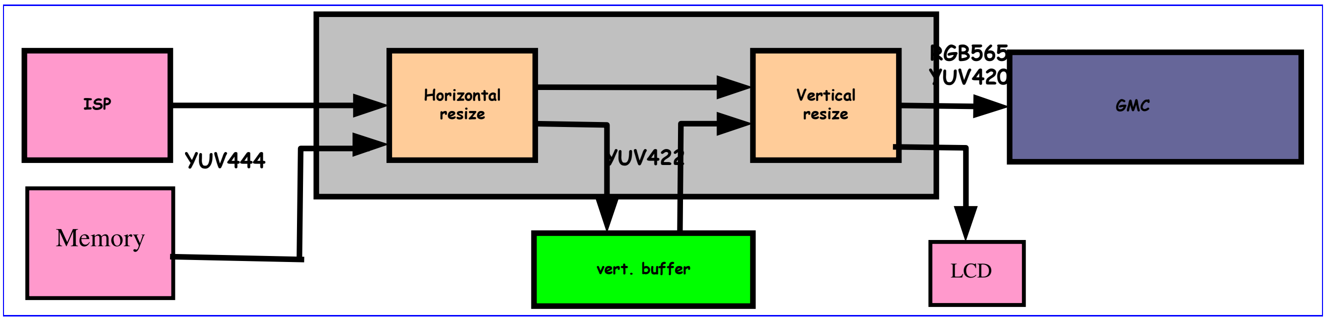

Figure 61 Overview of Image Resizer

6.2.2 Fine Resizing

Fine resizing is composed of horizontal resizing and vertical resizing. It has fractional resizing capability. The image input to fine resizing has size limit of maximum 1600x1200, so does the output of fine resizing. For the sake of cost and speed, the algorithm used in fine resizing is bilinear algorithm. In horizontal resizing working memory enough to fill in two scan-lines is needed. Of course dual buffer or more can be used. For pixel-based image, horizontal or vertical resizing can be trigged if necessarily or disabled if unnecessarily. However, if horizontal/vertical resizing is unnecessary and trigged, then horizontal/vertical resizing must be reset after resizing finishes.

6.2.3 YUV2RGB

Format translation from YUV domain to RGB domain is provided after vertical resizing. The sources of YUV2RGB are image data on the fly after vertical resizing. RGB is in format of 5-6-5. RGB output from YUV2RGB is in format of 5-6-5. That is, one pixel occupies two bytes.

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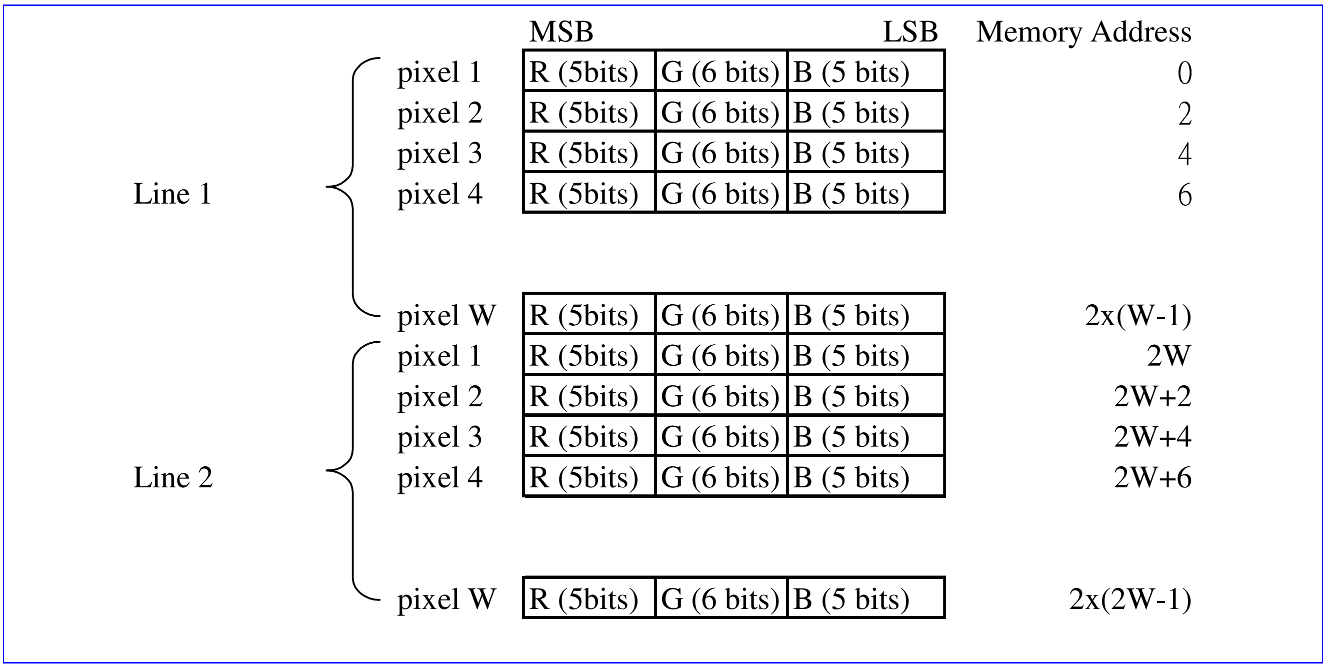

Figure 62 RGB Format

6.2.4 Register Definitions

REGISTER ADDRESS	REGISTER NAME	SYNONYM
0x84010000h	Image Resizer Configuration Register	RESZ_CFG
0x84010004h	Image Resizer Control Register	RESZ_CON
0x84010008h	Image Resizer Status Register	RESZ_STA
0x8401000Ch	Image Resizer Interrupt Register	RESZ_INT
0x84010010h	Image Resizer Source Image Size Register 1	RESZ_SRCSZ1
0x84010014h	Image Resizer Target Image Size Register 1	RESZ_TARSZ1
0x84010018h	Image Resizer Horizontal Ratio Register 1	RESZ_HRATIO1
0x8401001Ch	Image Resizer Vertical Ratio Register 1	RESZ_VRATIO1
0x84010020h	Image Resizer Horizontal Residual Register 1	RESZ_HRES1
0x84010024h	Image Resizer Vertical Residual Register 1	RESZ_VRES1
0x84010040h	Image Resizer Fine Resizing Configuration Register	RESZ_FRCFG
0x8401005Ch	Image Resizer Pixel-Based Resizing Working Memory Base Address	RESZ_PRWMBASE
0x84010060h	Image Resizer Source Image Size Register 2	RESZ_SRCSZ2
0x84010064h	Image Resizer Target Image Size Register 2	RESZ_TARSZ2

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0x84010068h	Image Resizer Horizontal Ratio Register 2	RESZ_HRATIO2
0x8401006Ch	Image Resizer Vertical Ratio Register 2	RESZ_VRATIO2
0x84010070h	Image Resizer Horizontal Residual Register 2	RESZ_HRES2
0x84010074h	Image Resizer Vertical Residual Register 2	RESZ_VRES2
0x84010080h	Image Resizer Output Mode	RESZ_OUTMODE
0x84010084h	Image Resizer Target Memory Base Address Register 1 (RGB565)	RESZ_TMBASE1
0x84010088h	Image Resizer Target Memory Base Address Register 2 (RGB565)	RESZ_TMBASE2
0x840100B0h	Image Resizer Information Register 0	RESZ_INFO0
0x840100B4h	Image Resizer Information Register 1	RESZ_INFO1
0x840100B8h	Image Resizer Information Register 2	RESZ_INFO2
0x840100BCh	Image Resizer Information Register 3	RESZ_INFO3
0x840100C0h	Image Resizer Information Register 4	RESZ_INFO4
0x840100C4h	Image Resizer Information Register 5	RESZ_INFO5
0x840100D0h	Image Resizer Target Memory Base Address for Y (YUV420 mode)	RESZ_TMBASE_Y
0x840100D4h	Image Resizer Target Memory Base Address for U (YUV420 mode)	RESZ_TMBASE_U
0x840100D8h	Image Resizer Target Memory Base Address for V (YUV420 mode)	RESZ_TMBASE_V
0x840100DCh	Image Resizer Source Memory Base Address for Y (MEMORY INPUT mode)	RESZ_SMBASE_Y
0x840100E0h	Image Resizer Source Memory Base Address for U (MEMORY INPUT mode)	RESZ_SMBASE_U
0x840100E4h	Image Resizer Source Memory Base Address for V (MEMORY INPUT mode)	RESZ_SMBASE_V
0x840100E8h	Image Resizer GMC Ultra-High Control Register 1	RESZ_GUC1
0x840100ECh	Image Resizer GMC Ultra-High Control Register 2	RESZ_GUC2
0x840100F0h	Image Resizer GMC Control Register	RESZ_GMCCON
0x840100F4h	Image Resizer Clip Horizontal Register	RESZ_CLIPLR
0x840100F8h	Image Resizer Clip Vertical Register	RESZ_CLIPTB
0x840100FCh	Image Resizer Pitch Register	RESZ_PITCH

0x84010000 Image Resizer Configuration Register RESZ_CFG

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name							NORGBDB	VSRSTEN			PRUN2	PCON			SRC2	SRC1
Type							R/W	R/W			R/W	R/W			R/W	R/W

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Reset							0	0	0	0		0	0

The register is for global configuration of Image Resizer.

SRC1 **The register bit specified the input source of 1st pass of resizer.**
- **0** **Camera input**
- **1** **Memory input. Only YUV420 input is supported.**

SRC2 **The register bit specified the input source of 2nd pass of resizer.**
- **0** **Camera input**
- **1** **Memory input. Only YUV420 input is supported.**

PCON The register bit specifies if resizing continues whenever an image finishes processing. Once continuous run for pixel-based resizing is enabled and pixel-based resizing is running, the only way to stop is to reset Capture Resize. If to stop immediately is desired, reset Capture Resize directly. If the last image is desired, set the register bit to '0' first. Then wait until image resizer is not busy again. Finally reset image resizer.
- **0** Single run
- **1** Continuous run

PRUN2 The register specifies if resizer runs with one pass or two pass.
- **0** One pass.
- **1** Two pass

VSRSTEN[0] Resizer auto reset when src is camera and new frame comes.
- **0** Disable.
- **1** Enable.

VSRSTEN[1] Resizer auto reset when src is camera and new frame comes and previous input is complete but output not complete.
- **0** Disable. (skip current frame) Enable. (Give up previous frame)
- **1** Enable. (Give up previous frame)

VSRSTEN[2] Resizer auto reset when src is camera and pixel drop is detected.
- **0** Disable.
- **1** Enable.

NORGBDB The register bit specifies if resizer use double buffer for RGB565 buffer.
- **0** Use double buffer for RGB565 buffer.
- **1** Use single buffer for RGB565 buffer.

0x84010004 Image Resizer Control Register RESZ_CON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RST
Type																R/W
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ENA
Type																R/W
Reset																0

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The register is for global control of Image Resizer. **Furthermore, software reset will NOT reset all register setting. Remember trigger Image Resizer first before trigger image sources to Image Resizer.**

ENA Writing '1' to the register bit will cause resizing proceed to work.

RST Writing '1' to the register will cause resizing to stop immediately and have resizing keep in reset state. In order to have resizing go to normal state, writing '0' to the register bit.

0x84010008 Image Resizer Status Register RESZ_STA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							MAXLBCNT									
Type							RO									
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name						ERR2	ERR1	ERR0		RUN2ST	INBUSY	MEMINBUSY	OUTBUSY	PELVRBUSY	PELHRBUSY	LCDBUSY
Type						RO	RO	RO		RO	RO	RO	RO	RO	RO	RO
Reset																

The register indicates global status of Image Resizer.

LCDBUSY Direct couple to LCD Busy Status

PELHRBUSY Pixel-based HR (Horizontal Resizing) Busy Status

PELVRBUSY Pixel-based VR (Vertical Resizing) Busy Status

OUTBUSY Output Busy Status

MEMINBUSY Memory input Busy Status

INBUSY Input Busy Status

RUN2ST Status of two pass resizing

- **0** 1st run
- **1** 2nd run

ERR0 Error status. Pixel over run (Camera request but resizer not ack)

ERR1 Error status. Input pixel is not enough.

ERR2 Error status. Input complete but output not complete when new frame comes.

MAXLBCNT Max line buffer used.

0x8401000C Image Resizer Interrupt Register RESZ_INT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name												MEMO2INT	PXDINT	FSTARTINT	MEMO1INT	LCDINT
Type												RC	RC	RC	RC	RC
Reset												0	0	0	0	0

The register shows up the interrupt status of resizer.

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LCDINT Interrupt for LCD direct couple. No matter the register bit RESZ_FRCFG.LCDINTEN is enabled or not, the register bit will be active whenever LCD direct couple completes. It could be as software interrupt by polling the register bit. Clear it by reading the register.

MEMO1INT Interrupt for Memory Output for 1st pass of two pass resizing or one pass resizing. No matter the register bit RESZ_FRCFG.MEMOINTEN is enabled or not, the register bit will be active whenever Memory Output completes. It could be as software interrupt by polling the register bit. Clear it by reading the register.

FSTARTINT Interrupt for frame start. No matter the register bit RESZ_FRCFG.FSTARTINTEN is enabled or not, the register bit will be active whenever a new frame arrives. It could be as software interrupt by polling the register bit. Clear it by reading the register. **Useful for digital zooming.**

PXDINT Interrupt for pixel drop. No matter the register bit RESZ_FRCFG.PXDINTEN is enabled or not, the register bit will be active whenever pixel drop occurs. It could be as software interrupt by polling the register bit. Clear it by reading the register. **Useful for error detection.**

MEMO2INT Interrupt for Memory Output for 2nd pass of two pass resizing or one pass resizing. No matter the register bit RESZ_FRCFG.MEMOINTEN is enabled or not, the register bit will be active whenever Memory Output completes. It could be as software interrupt by polling the register bit. Clear it by reading the register.

0x84010010 Image Resizer Source Image Size Register 1 RESZ_SRCSZ1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HS										
Type						R/W										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						WS										
Type						R/W										

The register specifies the size of source image after coarse shrinking. **The allowable maximum size is 1600x1200**.

WS The register field specifies the width of source image after coarse shrinking.

- **2** The width of source image is 2.
- **4** The width of source image is 4.

…

HS The register field specifies the height of source image after coarse shrinking.

- **2** The height of source image is 2.
- **4** The height of source image is 4.

…

Note: WS and HS must be even number.

Note: If the source is memory input, 16's multiples for WS is suggested. Otherwise, the input memory content should be 16's multiples padded which is consistent with resizer YUV420 output.

0x84010014 Image Resizer Target Image Size Register 1 RESZ_TARSZ1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HT										
Type						R/W										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name		WT
Type		R/W

The register specifies the size of target image. **The allowable maximum size is 1600x1200.**

WT The register field specifies the width of target image.
- **2** The width of target image is 2.
- **4** The width of target image is 4.
- …

HT The register field specifies the height of target image.
- **2** The height of target image is 2.
- **4** The height of target image is 4.
- …

Note: WT and HT must be even number.

Note: WT would be padded to 16's multiples if the output mode is YUV420

0x84010018 Image Resizer Horizontal Ratio Register 1 RESZ_HRATIO1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RATIO [30:16]														
Type		R/W														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RATIO [15:0]															
Type	R/W															

The register specifies horizontal resizing ratio. It is obtained by RESZ_SRCSZ.WS * 2^{20} / RESZ_TARSZ.WT.

0x8401001C Image Resizer Vertical Ratio Register 1 RESZ_VRATIO1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RATIO [30:16]														
Type		R/W														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RATIO [15:0]															
Type	R/W															

The register specifies vertical resizing ratio. It is obtained by RESZ_SRCSZ.HS * 2^{20} / RESZ_TARSZ.HT.

0x84010020 Image Resizer Horizontal Residual Register 1 RESZ_HRES1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RESIDUAL										
Type						R/W										

The register specifies horizontal residual. It is obtained by RESZ_SRCSZ.WS % RESZ_TARSZ.WT

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0x84010024 Image Resizer Vertical Residual Register 1 RESZ_VRES1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RESIDUAL										
Type						R/W										

The register specifies vertical residual. It is obtained by RESZ_SRCSZ.HS % RESZ_TARSZ.HT.

0x84010040 Image Resizer Fine Resizing Configuration Register RESZ_FRCFG

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							WMSZ									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			FSTART21EN	MEMO2INTEN	PXDINTEN	FSTARTINTEN	MEMO1INTEN	LCDINTEN	PCSF2		PCSF1			AVG1	AVG0	VRSS
Type			R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W			R/W	R/W	R/W
Reset			0	0	0	0	0	0	00		00			0	0	0

The register specifies various setting of control for fine resizing, including of horizontal and vertical resizing. **Note that all parameters must be set before horizontal and vertical resizing proceeds.**

VRSS The register bit specifies whether subsampling for vertical resizing is enabled. For throughput issue, vertical resizing may be simplified by subsampling lines vertically. The register bit is only valid in pixel-based mode.

- **0** Subsampling for vertical resizing is disabled.
- **1** Subsampling for vertical resizing is enabled.

AVG0 Average if src/tar = 1/n

- **0** Average is disabled.
- **1** Average is enabled.

AVG1 Average always. (Suggestion: Turn on if ratio is small)

- **0** Average is disabled.
- **1** Average is enabled.

LCDINTEN LCD direct couple Interrupt Enable.

- **0** Interrupt for LCD direct couple is disabled.
- **1** Interrupt for LCD direct couple is enabled.

MEMO1INTEN Memory output Interrupt Enable for 1st pass of two pass resizing or one pass resizing.

- **0** Interrupt for Memory output is disabled.
- **1** Interrupt for Memory output is enabled.

FSTARTINTEN Frame start Interrupt Enable.

- **0** Interrupt for frame start is disabled.
- **1** Interrupt for frame start is enabled.

PXDINTEN Pixel drop Interrupt Enable.

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0 Interrupt for frame start is disabled.
1 Interrupt for frame start is enabled.

MEMO2INTEN Memory output Interrupt Enable of 2nd pass of two pass resizing.
0 Interrupt for Memory output of 1st pass of two pass resizing is disabled.
1 Interrupt for Memory output of 1st pass of two pass resizing is enabled.

FSTART21EN Frame start Interrupt Enable of 1st pass of two pass resizing.
0 Interrupt for frame start of 1st pass of two pass resizing is disabled.
1 Interrupt for frame start of 1st pass of two pass resizing is enabled.

PCSF1 Coarse Shrinking Factor 1. **Only horizontal coarse shrinking is supported.**
00 No coarse shrinking.
01 Image width becomes 1/2 of original size after coarse shrink pass.
10 Image width becomes 1/4 of original size after coarse shrink pass.
11 Image width becomes 1/8 of original size after coarse shrink pass.

PCSF2 Coarse Shrinking Factor 2. **Only horizontal coarse shrinking is supported.**
00 No coarse shrinking.
01 Image width becomes 1/2 of original size after coarse shrink pass.
10 Image width becomes 1/4 of original size after coarse shrink pass.
11 Image width becomes 1/8 of original size after coarse shrink pass.

WMSZ It stands for Working Memory Size. The register specifies how many lines after horizontal resizing can be filled into working memory. **Its minimum value is 4.**
4 Working memory is 4.
5 Working memory is 5.
…

0x8401005C Image Resizer Pixel-Based Resizing Working Memory Base Address Register RESZ_PRWMBASE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PRWMBASE [31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRWMBASE [15:2]															
Type	R/W															

The register specifies the base address of working memory in pixel-based resizing mode. It must be word-aligned. **And it can be placed at internal memory only.**

Note: Please be careful NOT to allow MCU to access the same bank of internal memory while resizer is running. Otherwise, resizer will be disturbed by MCU access, and the performance would be degraded.

0x84010060 Image Resizer Source Image Size Register 2 RESZ_SRCSZ2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HS										

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Type						R/W										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						WS										
Type						R/W										

The register specifies the size of source image after coarse shrinking. **The allowable maximum size is 1600x1200**.

WS The register field specifies the width of source image after coarse shrinking.

- **2** The width of source image is 2.
- **4** The width of source image is 4.
- …

HS The register field specifies the height of source image after coarse shrinking.

- **2** The height of source image is 2.
- **4** The height of source image is 4.
- …

Note: WS and HS must be even number.

Note: If the source is memory input, 16's multiples for WS is suggested. Otherwise, the input memory content should be 16's multiples padded which is consistent with resizer YUV420 output.

0x84010064 Image Resizer Target Image Size Register 2 RESZ_TARSZ2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HT										
Type						R/W										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						WT										
Type						R/W										

The register specifies the size of target image. **The allowable maximum size is 1600x1200.**

WT The register field specifies the width of target image.

- **2** The width of target image is 2.
- **4** The width of target image is 4.
- …

HT The register field specifies the height of target image.

- **2** The height of target image is 2.
- **4** The height of target image is 4.
- …

Note: WT and HT must be even number.

Note: WT would be padded to 16's multiples if the output mode is YUV420

0x84010068 Image Resizer Horizontal Ratio Register 2 RESZ_HRATIO2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RATIO [30:16]														
Type		R/W														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	RATIO [15:0]
Type	R/W

The register specifies horizontal resizing ratio. It is obtained by RESZ_SRCSZ.WS * 2^{20} / RESZ_TARSZ.WT.

0x8401006C Image Resizer Vertical Ratio Register 2 RESZ_VRATIO2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RATIO [30:16]														
Type		R/W														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RATIO [15:0]															
Type	R/W															

The register specifies vertical resizing ratio. It is obtained by RESZ_SRCSZ.HS * 2^{20} / RESZ_TARSZ.HT.

0x84010070 Image Resizer Horizontal Residual Register 2 RESZ_HRES2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RESIDUAL										
Type						R/W										

The register specifies horizontal residual. It is obtained by RESZ_SRCSZ.WS % RESZ_TARSZ.WT

0x84010074 Image Resizer Vertical Residual Register 2 RESZ_VRES2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RESIDUAL										
Type						R/W										

The register specifies vertical residual. It is obtained by RESZ_SRCSZ.HS % RESZ_TARSZ.HT.

0x84010080 Image Resizer YUV2RGB Configuration Register RESZ_OUTMODE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												HTLCD	OMODE2		OMODE1	
Type												R/W	R/W		R/W	
Reset												0	0		0	

OMODE1 Output mode for 1st pass.

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0 RGB565 output.
1 YUV420 output.
2 Direct couple to LCD.
3 YUV420 output + Direct couple to LCD.

OMODE2 Output mode for 2nd pass.
0 RGB565 output.
1 YUV420 output.
2 Direct couple to LCD.
3 YUV420 output + Direct couple to LCD.

HTLCD Hardware trigger for LCD when resizer finishes one RGB565 frame.
0 Disable.
1 Enable.

0x84010084 Image Resizer Target Memory Base Address Register RESZ_TMBASE1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TMBASE1 [31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TMBASE1 [15:4]															
Type	R/W															

The register specifies the base address of target memory for RGB565 mode. Target memory is memory space for destination of YUV2RGB. It must be 16 bytes aligned. RESZ_TMBASE1 and RESZ_TMBASE2 are auto-switched by hardware.

0x84010088 Image Resizer Target Memory Base Address Register RESZ_TMBASE2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TMBASE2 [31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TMBASE2 [15:4]															
Type	R/W															

The register specifies the base address of target memory for RGB565 mode. Target memory is memory space for destination of YUV2RGB. It must be 16 bytes aligned.

0x84010090 Image Resizer Debug Configuration Register RESZ_DBGCFG

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name					NODB	PHR1	PVR1						
Type					R/W	R/W	R/W						
Reset					0	0	1						

The register is used to help debug.

NODB Force register not double buffered

- **0** Double buffered, registers are effective when camera vsync arrives or memory input starts.
- **1** No double buffered

PVR1 Force vertical resizing to execute even though it's not necessary.

- **0** Normal operation
- **1** Force vertical resizing to execute even though it's not necessary.

PHR1 Force horizontal resizing to execute even though it's not necessary.

- **0** Normal operation
- **1** Force horizontal resizing to execute even though it's not necessary.

0x840100B0 Image Resizer Information Register 0 RESZ_INFO0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INFO[31:16]															
Type	RO															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INFO[15:0]															
Type	RO															

The register shows the max working memory really used

INFO[31:16] Input interface vertical counter
INFO[15:00] Input interface horizontal counter

0x840100B4 Image Resizer Information Register 1 RESZ_INFO1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INFO[31:16]															
Type	RO															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INFO[15:0]															
Type	RO															

INFO[31:16] LCD direct couple vertical counter.
INFO[15:00] LCD direct couple horizontal counter.

0x840100C4 Image Resizer Information Register 5 RESZ_INFO5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INFO[31:16]															
Type	RO															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INFO[15:0]															
Type	RO															

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INFO[31:16] Memory output vertical counter.
INFO[15:00] Memory output horizontal counter

0x840100D0 Image Resizer YUV420 Y-Component Target Memory Base Address Register RESZ_TMBASE_Y

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TMBASE_Y[31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TMBASE_Y[15:4]															
Type	R/W															

The register specifies the base address of YUV420 output for Y-component. It should be 16 bytes aligned. It's only useful in YUV420 mode.

0x840100D4 Image Resizer YUV420 U-Component Target Memory Base Address Register RESZ_TMBASE_U

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TMBASE_U[31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TMBASE_U[15:4]															
Type	R/W															

The register specifies the base address of YUV420 output for U-component. It should be 16 bytes aligned. It's only useful in YUV420 mode.

0x840100D8 Image Resizer YUV420 V-Component Target Memory Base Address Register RESZ_TMBASE_V

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TMBASE_V[31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TMBASE_V[15:4]															
Type	R/W															

The register specifies the base address of YUV420 output for V-component. It should be 16 bytes aligned. It's only useful in YUV420 mode.

0x840100DC Image Resizer Y-Component Source Memory Base Address Register RESZ_SMBASE_Y

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMBASE_Y[31:16]															

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Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMBASE_Y[15:4]															
Type	R/W															

The register specifies the base address of YUV420 input for Y-component. It should be 16 bytes aligned. It's only useful in Memory input mode.

0x840100E0 Image Resizer U-Component Source Memory Base Address Register RESZ_SMBASE_U

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMBASE_U[31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMBASE_U[15:4]															
Type	R/W															

The register specifies the base address of YUV420 input for U-component. It should be 16 bytes aligned. It's only useful in Memory input mode.

0x840100E4 Image Resizer V-Component Source Memory Base Address Register RESZ_SMBASE_V

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMBASE_V[31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMBASE_V[15:4]															
Type	R/W															

The register specifies the base address of YUV420 input for V-component. It should be 16 bytes aligned. It's only useful in Memory input mode.

0x840100E8 Image Resizer GMC Ultra-High Control Register 1 RESZ_GUC1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UEN						ULINE									
Type	R/W						R/W									
Reset	0						0									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						UPXL										
Type						R/W										
Reset						0										

Resizer issues ultra high request to gain more bandwidth when (**UEN** == 1) & (lines in line buffer >= **ULINE**) & (pixel count >= **UPXL**).

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0x840100EC Image Resizer GMC Ultra-High Control Register 2 RESZ_GUC2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ULTRA0				ULTRA1			
Type									R/W				R/W			
Reset									0				1			

GMC issues request **with ultra high** for successive **ULTRA1** transactions, and then issues request **without ultra high** for successive **ULTRA0** transactions.

0x840100F0 Image Resizer GMC Control Register RESZ_GMCCON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RD_MIN_REQ_INTERVAL												WR_MIN_REQ_INTERVAL [11:8]			
Type	R/W												R/W			
Reset	0												0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WR_MIN_REQ_INTERVAL [7:0]								RD_MIN_REQ_EN	WR_MIN_REQ_EN	RD_MAX_BURST_LENGTH			WR_MAX_BURST_LENGTH		
Type	R/W								R/W	R/W	R/W			R/W		
Reset	0								0	0	0			0		

WR_MAX_BURST_LENGTH Specify the maximum burst length of GMC request for write port.

- **4** Burst 4 beats access, and one beat is 2 bytes. Total data amount is 8 bytes per access.
- **3** Single 4 bytes access
- **2** Burst 4 beats access, and one beat is 4 bytes. Total data amount is 16 bytes per access.
- **1** Burst 8 beats access, and one beat is 4 bytes. Total data amount is 32 bytes per access.
- **0** Burst 16 beats access, and one beat is 4 bytes. Total data amount is 64 bytes per access.

RD_MAX_BURST_LENGTH Specify the maximum burst length of GMC request for read port.

- **2** Single 4 bytes access
- **1** Burst 4 beats access, and one beat is 2 bytes. Total data amount is 8 bytes per access.
- **0** Burst 4 beats access, and one beat is 4 bytes. Total data amount is 16 bytes per access.

WR_MIN_REQ_EN Enable GMC port minimum request control for write port.

RD_MIN_REQ_EN Enable GMC port minimum request control for read port.

WR_MIN_REQ_INTERVAL It specifies how many AHB bus cycles between two GMC requests for write port.

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RD_MIN_REQ_INTERVAL It specifies how many AHB bus cycles between two GMC requests for read port.

0x840100F4 Image Resizer GMC Horizontal Register RESZ_CLIPLR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLIPEN					CLIP_L										
Type	R/W					R/W										
Reset	0					0										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						CLIP_R										
Type						R/W										
Reset						0										

CLIP_R Right boundary of clipping. CLIP_R itself is including in the clipped region. The pixel counter starts from 0.

CLIP_L Left boundary of clipping. CLIP_L itself is including in the clipped region.

CLIP_EN Enable Clip function. Clip function is used to clip resized image before writing to memory. Useful for **RGB mode only**.

Note: (CLIP_R – CLIP_L + 1) = WT should be an even number

0x840100F8 Image Resizer Clip Vertical Register RESZ_CLIPTB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CLIP_T										
Type						R/W										
Reset						0										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						CLIP_B										
Type						R/W										
Reset						0										

CLIP_B Bottom boundary of clipping. CLIP_B itself is including in the clipped region. The line counter starts from 0.

CLIP_T Top boundary of clipping. CLIP_T itself is including in the clipped region.

Note: (CLIP_B – CLIP_T + 1) = HT should be an even number

0x840100FC Image Resizer Pitch Register RESZ_PITCH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PITCH_EN															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						PITCH_WD										
Type						R/W										
Reset						0										

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PITCH_EN Enable Pitch function. Useful for **RGB mode only**.

0 Enabled

1 Disabled

PITCH_WD Width of background image.

Note: PITCH_WD should be an even number.

6.2.5 Application Notes

- Working memory. Maximum value is 1023 and minimum 4. **Remember that each pixel occupies 2 bytes**. Thus minimum requirement for working memory in pixel-based resizing is (pixel number in a line)x2x4 bytes.
- Configuration procedure when source is cam

```
RESZ_CFG = 0x10 (continuous), 0x0 (single run);
RESZ_TMBASE1 = target memory 1 base address (RGB565 mode);
RESZ_TMBASE2 = target memory 2 base address (RGB565 mode);
RESZ_TMBASE_Y = target memory for Y base address (YUV420 mode);
RESZ_TMBASE_U = target memory for U base address (YUV420 mode);
RESZ_TMBASE_V = target memory for V base address (YUV420 mode);
RESZ_SRCSZ1 = source image size;
RESZ_TARSZ1 = target image size;
RESZ_HRATIO1 = horizontal ratio;
RESZ_VRATIO1 = vertical ratio;
RESZ_HRES1 = horizontal residual;
RESZ_VRES1 = vertical residual;
RESZ_FRCFG = working memory size, interrupt enable;
RESZ_PRWMBASE = working memory base;
RESZ_OUTMODE = Output mode select;
RESZ_CON = 0x1;
```

- Configuration procedure when source is memory

```
RESZ_CFG = 0x1 (single run);
RESZ_TMBASE1 = target memory 1 base address (RGB565 mode);
RESZ_TMBASE2 = target memory 2 base address (RGB565 mode);
RESZ_TMBASE_Y = target memory for Y base address (YUV420 mode);
RESZ_TMBASE_U = target memory for U base address (YUV420 mode);
RESZ_TMBASE_V = target memory for V base address (YUV420 mode);
RESZ_SMBASE_Y = source memory for Y base address;
RESZ_SMBASE_U = source memory for U base address;
RESZ_SMBASE_V = source memory for V base address;
RESZ_SRCSZ1 = source image size;
RESZ_TARSZ1 = target image size;
RESZ_HRATIO1 = horizontal ratio;
RESZ_VRATIO1 = vertical ratio;
RESZ_HRES1 = horizontal residual;
RESZ_VRES1 = vertical residual;
```

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```
RESZ_FRCFG = working memory size, interrupt enable;
RESZ_PRWMBASE = working memory base;
RESZ_OUTMODE = Output mode select;
RESZ_CON = 0x1;
```

- Configuration procedure for two pass resizing. (1.CAM=>YUV420, 2.MEM=>RGB565)

```
RESZ_CFG = 0x32;
RESZ_TMBASE1 = target memory 1 base address (RGB565 mode);
RESZ_TMBASE2 = target memory 2 base address (RGB565 mode);
RESZ_TMBASE_Y = target memory for Y base address (YUV420 mode);
RESZ_TMBASE_U = target memory for U base address (YUV420 mode);
RESZ_TMBASE_V = target memory for V base address (YUV420 mode);
RESZ_SMBASE_Y = RESZ_TMBASE_Y;
RESZ_SMBASE_U = RESZ_TMBASE_U;
RESZ_SMBASE_V = RESZ_TMBASE_V;
RESZ_SRCSZ1 = Camera size;
RESZ_TARSZ1 = Video size;
RESZ_HRATIO1 = horizontal ratio;
RESZ_VRATIO1 = vertical ratio;
RESZ_HRES1 = horizontal residual;
RESZ_VRES1 = vertical residual;
RESZ_SRCSZ2 = Video size;
RESZ_TARSZ2 = LCD panel size;
RESZ_HRATIO2 = horizontal ratio;
RESZ_VRATIO2 = vertical ratio;
RESZ_HRES2 = horizontal residual;
RESZ_VRES2 = vertical residual;
RESZ_FRCFG = working memory size, interrupt enable;
RESZ_PRWMBASE = working memory base;
RESZ_OUTMODE = 0x1;
RESZ_CON = 0x1;
```

- Configuration procedure for off-line capture with zoom. (1.CAM=>MEM (ratio = 1), 2. MEM=>RGB565 (lcd size), MEM=>YUV420 (jpeg size))

PHASE1

```
RESZ_CFG = 0x0;
RESZ_TMBASE_Y = Additional Y Frame Buffer;
RESZ_TMBASE_U = Additional U Frame Buffer;
RESZ_TMBASE_V = Additional V Frame Buffer;
RESZ_SRCSZ1 = Zoomed Size;
RESZ_TARSZ1 = Zoomed Size;
RESZ_HRATIO1 = horizontal ratio;
RESZ_VRATIO1 = vertical ratio;
RESZ_HRES1 = horizontal residual;
RESZ_VRES1 = vertical residual;
RESZ_FRCFG = working memory size, interrupt enable;
```


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```
RESZ_PRWMBASE = working memory base;
RESZ_OUTMODE = 0x1;
RESZ_CON = 0x1;
```

PHASE2

```
RESZ_CFG = 0x23; //PRUN2, SRC1=1, SRC2=1
RESZ_TMBASE1 = target memory 1 base address (RGB565 mode);
RESZ_TMBASE2 = target memory 2 base address (RGB565 mode);
RESZ_TMBASE_Y = target memory for Y base address (YUV420 mode);
RESZ_TMBASE_U = target memory for U base address (YUV420 mode);
RESZ_TMBASE_V = target memory for V base address (YUV420 mode);
RESZ_SMBASE_Y = Additional Y Frame Buffer;
RESZ_SMBASE_U = Additional U Frame Buffer;
RESZ_SMBASE_V = Additional V Frame Buffer;
RESZ_SRCSZ1 = Zoomed size;
RESZ_TARSZ1 = LCD size;
RESZ_HRATIO1 = horizontal ratio;
RESZ_VRATIO1 = vertical ratio;
RESZ_HRES1 = horizontal residual;
RESZ_VRES1 = vertical residual;
RESZ_SRCSZ2 = Zoomed size;
RESZ_TARSZ2 = JPEG size;
RESZ_HRATIO2 = horizontal ratio;
RESZ_VRATIO2 = vertical ratio;
RESZ_HRES2 = horizontal residual;
RESZ_VRES2 = vertical residual;
RESZ_FRCFG = working memory size, interrupt enable;
RESZ_PRWMBASE = working memory base;
RESZ_OUTMODE = 0x2; //OMODE11=RGB, OMODE2=YUV
RESZ_CON = 0x1;
```


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6.3 NAND FLASH interface

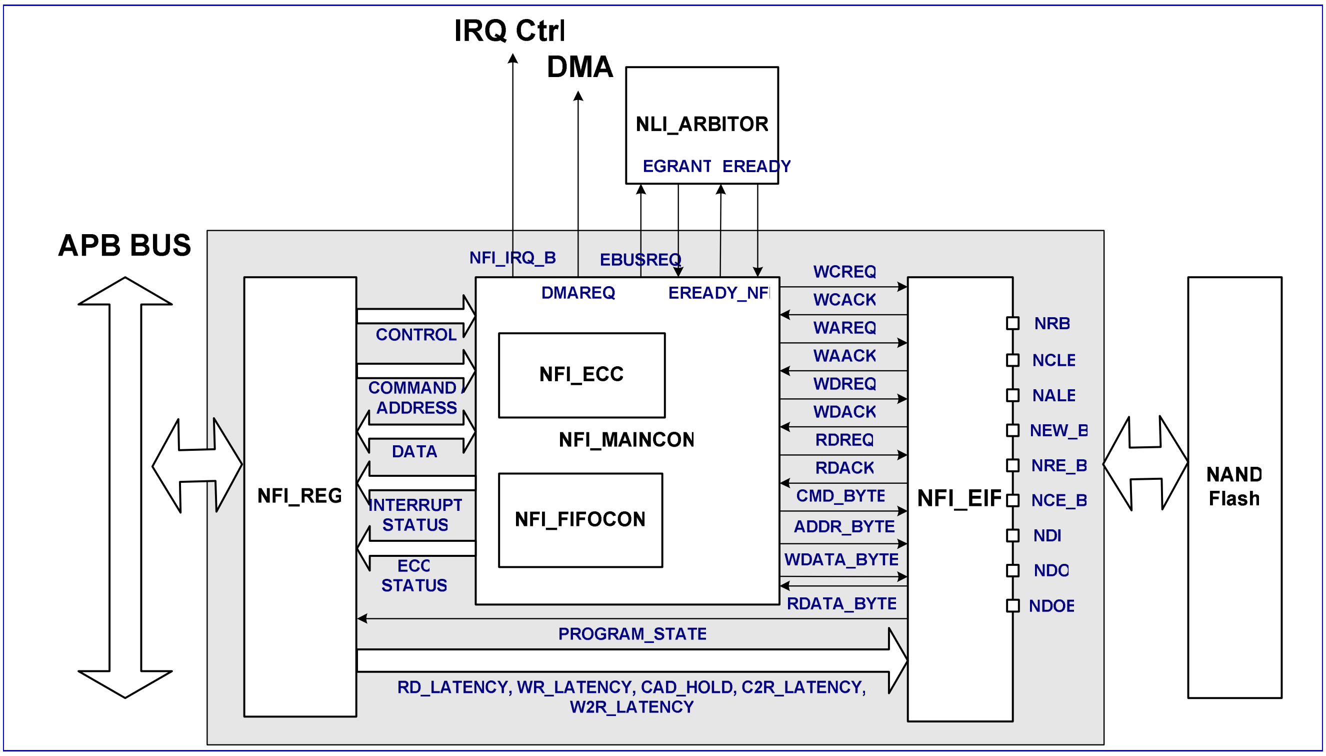

Figure 63 Block Diagram of NAND Flash Interface

MT6251/MT6253 provides NAND flash interface.

The NAND FLASH interface support features as follows:

- ECC (Hamming code) acceleration capable of one-bit error correction or two bits error detection.
- Programmable ECC block size. Support 1, 2 or 4 ECC block within a page.
- Word/byte access through APB bus.
- Direct Memory Access for massive data transfer.
- Latch sensitive interrupt to indicate ready state for read, program, erase operation and error report.
- Programmable wait states, command/address setup and hold time, read enable hold time, and write enable recovery time.
- Support page size: 512(528) bytes and 2048(2112) bytes.
- Support 2 chip select for NAND flash parts.
- Support 8/16 bits I/O interface.

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The NFI core can automatically generate ECC parity bits when programming or reading the device. If the user approves the way it stores the parity bits in the spare area for each page, the AUTOECC mode can be used. Otherwise, the user can prepare the data (may contains operating system information or ECC parity bits) for the spare area with another arrangement. In the former case, the core can check the parity bits when reading from the device. The ECC module features the hamming code, which is capable of correcting one bit error or detecting two bits error within one ECC block.

6.3.1 General description

6.3.1.1 Input and Output Interface

6.3.1.2 DMA/MCU

Signal Name	Direction	Function
damreq	Output	Data request from or to DMA
nfi_irq_b	Output	Interrupt for MCU

Table 48

6.3.1.3 NLI Arbiter and NAND Flash Device

Signal Name	Direction	Function
Egrant	Input	NLI bus grant indication
Eready	Input	NLI bus ready indication
Eready_nfi	Output	NFI ready indication for NLI bus ready
Ebusreq	Output	NLI bus request
NDI	Input	NAND Data Input
NDO	Output	NAND Data Output
NDOE	Output	NANA Data Output Enable
NRB	Output	NAND Flash Ready/Busy
NCE[1:0]	Output	NAND Flash Chip Enable
NWR	Output	NAND Flash Write Enable
NRE	Output	NAND Flash Read Enable
NCLE	Output	NAND Flash Command Latch Enable
NALE	Output	NAND Flash Address Latch Enable

Table 49

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6.3.1.4 APB

Signal Name	Direction	Function
paddr[15:0]	Input	16 LSB of the ARM Address Bus
pwrite	Input	Write Control
penable	Input	Enable Interface
psel	Input	Transmitter Interface Select
pwdata[31:0]	Input	32 Bits of the ARM Writer Data Bus
prdata[31:0]	Output	32 Bits of the ARM Read Data Bus

Table 50

6.3.2 Registers

6.3.2.1 Registers Memory Map

Software responsibility and controllable functions

Register Address	Acronym	Register Function
0x8112_0000h	NFI_ACCCON	NAND Flash Access Control
0x8112_0004h	NFI_PAGEFMT	NFI Page Format Control
0x8112_0008h	NFI_OPCON	Operation Control
0x8112_0010h	NFI_CMD	Command
0x8112_0020h	NFI_ADDRNOB	Address Length
0x8112_0024h	NFI_ADDRL	Least Significant Address
0x8112_0028h	NFI_ADDRM	Most Significant Address
0x8112_0030h	NFI_DATAW	Write Data Buffer
0x8112_0034h	NFI_DATAWB	Write Data Buffer for Byte Access
0x8112_0038h	NFI_DATAR	Read Data Buffer
0x8112_003Ch	NFI_DATARB	Read Data Buffer for Byte Access
0x8112_0040h	NFI_PSTA	NFI Status
0x8112_0044h	NFI_FIFOSTA	NFI FIFO Status
0x8112_0050h	NFI_FIFODATA0	NFI FIFO Data 0
0x8112_0054h	NFI_FIFODATA1	NFI FIFO Data 1

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0x8112_0058h	NFI_FIFODATA2	NFI FIFO Data 2
0x8112_005Ch	NFI_FIFODATA3	NFI FIFO Data 3
0x8112_0060h	NFI_CON	NFI Control
0x8112_0064h	NFI_INTR	NFI Interrupt Status
0x8112_0068h	NFI_INTR_EN	NFI Interrupt Enable
0x8112_0070h	NFI_PAGECNTR	NAND Flash Page Counter
0x8112_0074h	NFI_ADDRCNTR	NAND Flash Page Address Counter
Main Area ECC		
0x8112_0080h	NFI_SYM0_ADDR	ECC Block 0 Parity Error Detect Syndrome Address
0x8112_0084h	NFI_SYM1_ADDR	ECC Block 1 Parity Error Detect Syndrome Address
0x8112_0088h	NFI_SYM2_ADDR	ECC Block 2 Parity Error Detect Syndrome Address
0x8112_008Ch	NFI_SYM3_ADDR	ECC Block 3 Parity Error Detect Syndrome Address
0x8112_0090h	NFI_SYM4_ADDR	ECC Block 4 Parity Error Detect Syndrome Address
0x8112_0094h	NFI_SYM5_ADDR	ECC Block 5 Parity Error Detect Syndrome Address
0x8112_0098h	NFI_SYM6_ADDR	ECC Block 6 Parity Error Detect Syndrome Address
0x8112_009Ch	NFI_SYM7_ADDR	Spare ECC Block 7 Parity Error Detect Syndrome Address
0x8112_00A0h	NFI_SYMS0_ADDR	Spare ECC Block 0 Parity Error Detect Syndrome Address
0x8112_00A4h	NFI_SYMS1_ADDR	Spare ECC Block 1 Parity Error Detect Syndrome Address
0x8112_00A8h	NFI_SYMS2_ADDR	Spare ECC Block 2 Parity Error Detect Syndrome Address
0x8112_00ACh	NFI_SYMS3_ADDR	Spare ECC Block 3 Parity Error Detect Syndrome Address
0x8112_00B0h	NFI_SYM0_DATA	ECC Block 0 Parity Error Detect Syndrome Word
0x8112_00B4h	NFI_SYM1_DATA	ECC Block 1 Parity Error Detect Syndrome Word
0x8112_00B8h	NFI_SYM2_DATA	ECC Block 2 Parity Error Detect Syndrome Word
0x8112_00BCh	NFI_SYM3_DATA	ECC Block 3 Parity Error Detect Syndrome Word
0x8112_00C0h	NFI_SYM4_DATA	ECC Block 4 Parity Error Detect Syndrome Word
0x8112_00C4h	NFI_SYM5_DATA	ECC Block 5 Parity Error Detect Syndrome Word
0x8112_00C8h	NFI_SYM6_DATA	ECC Block 6 Parity Error Detect Syndrome Word
0x8112_00CCh	NFI_SYM7_DATA	ECC Block 7 Parity Error Detect Syndrome Word
0x8112_00D0h	NFI_SYMS0_DATA	Spare ECC Block 0 Parity Error Detect Syndrome Word
0x8112_00D4h	NFI_SYMS1_DATA	Spare ECC Block 1 Parity Error Detect Syndrome Word
0x8112_00D8h	NFI_SYMS2_DATA	Spare ECC Block 2 Parity Error Detect Syndrome Word
0x8112_00DCh	NFI_SYMS3_DATA	Spare ECC Block 3 Parity Error Detect Syndrome Word

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0x8112_00E0h	NFI_PAR_0P	NFI ECC Parity Word 0
0x8112_00E4h	NFI_PAR_0C	NFI ECC Parity Word 0
0x8112_00E8h	NFI_PAR_1P	NFI ECC Parity Word 1
0x8112_00ECh	NFI_PAR_1C	NFI ECC Parity Word 1
0x8112_00F0h	NFI_PAR_2P	NFI ECC Parity Word 2
0x8112_00F4h	NFI_PAR_2C	NFI ECC Parity Word 2
0x8112_00F8h	NFI_PAR_3P	NFI ECC Parity Word 3
0x8112_00FCh	NFI_PAR_3C	NFI ECC Parity Word 3
0x8112_0100h	NFI_PAR_4P	NFI ECC Parity Word 4
0x8112_0104h	NFI_PAR_4C	NFI ECC Parity Word 4
0x8112_0108h	NFI_PAR_5P	NFI ECC Parity Word 5
0x8112_010Ch	NFI_PAR_5C	NFI ECC Parity Word 5
0x8112_0110h	NFI_PAR_6P	NFI ECC Parity Word 6
0x8112_0114h	NFI_PAR_6C	NFI ECC Parity Word 6
0x8112_0118h	NFI_PAR_7P	NFI ECC Parity Word 7
0x8112_011Ch	NFI_PAR_7C	NFI ECC Parity Word 7
0x8112_0120h	NFI_PARS_0P	NFI Spare ECC Parity Word 0
0x8112_0124h	NFI_PARS_0C	NFI Spare ECC Parity Word 0
0x8112_0128h	NFI_PARS_1P	NFI Spare ECC Parity Word 1
0x8112_012Ch	NFI_PARS_1C	NFI Spare ECC Parity Word 1
0x8112_0130h	NFI_PARS_2P	NFI Spare ECC Parity Word 2
0x8112_0134h	NFI_PARS_2C	NFI Spare ECC Parity Word 2
0x8112_0138h	NFI_PARS_3P	NFI Spare ECC Parity Word 3
0x8112_013Ch	NFI_PARS_3C	NFI Spare ECC Parity Word 3
0x8112_0140h	NFI_ECCDET	NFI ECC Error Detect Indication
0x8112_0144h	NFI_PARECC	NFI ECC Parity Error Indication
0x8112_0148h	NFI_SCON	NFI Spare ECC Control
I/O Pin Control		
0x8112_0200h	NFI_CSEL	NAND Flash Device Select
0x8112_0204h	NFI_IOCON	NFI IO Control

Table 51 Registers Memory Map Table

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6.3.2.2 Register definition

0x8112_0000h NAND flash access control register NFI_ACCCON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LCD2NAND										C2R					
Type	R/W										R/W					
Reset	0										0					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	W2R				WH				WST				RLT			
Type	R/W				R/W				R/W				R/W			
Reset	0				0				0				0			

This is the timing access control register for the NAND FLASH interface. In order to accommodate operations for different system clock frequency ranges from 13MHz to 52MHz, wait states and setup/hold time margin can be configured in this register.

C2R The field represents the minimum required time from NCEB low to NREB low.

W2R The field represents the minimum required time from NWEB high to NREB low. It's in unit of 2T. So the actual time ranges from 2T to 8T in step of 2T.

WH Write-enable hold-time.

The field specifies the hold time of NALE, NCLE, NCEB signals relative to the rising edge of NWEB. This field is associated with **WST** to expand the write cycle time, and is associated with **RLT** to expand the read cycle time.

RLT Read Latency Time

The field specifies how many wait states to be inserted to meet the requirement of the read access time for the device.

00 No wait state.
01 1T wait state.
10 2T wait state.
11 3T wait state.

WST Write Wait State

The field specifies the wait states to be inserted to meet the requirement of the pulse width of the NWEB signal.

00 No wait state.
01 1T wait state.
10 2T wait state.
11 3T wait state.

LCD2NAND Arbitration Wait State

The field specifies the wait states to be inserted for the APB arbitrator when bus user changes.

NOTES : **C2R → 2*C2R + 1**
W2R → 2*W2R + 3
WH/RLT/WST → WH/RLT/WST + 1

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0x8112_0004h NFI page format control register NFI_PAGEFMT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								B16EN		ECCBLKSIZE			ADRMODE		PSIZE	
Type								R/W		R/W			R/W		R/W	
Reset								0		0			0		0	

This register manages the page format of the device. It includes the bus width selection, the page size, the associated address format, and the ECC block size.

B16EN 16 bits I/O bus interface enable.

ECCBLKSIZE ECC block size.

This field represents the size of one ECC block. The hardware-fuelled ECC generation provides 2 or 4 blocks within a single page.

- **0** ECC block size: 128 bytes. Used for devices with page size equal to 512 bytes.
- **1** ECC block size: 256 bytes. Used for devices with page size equal to 512 bytes.
- **2** ECC block size: 512 bytes. Used for devices with page size equal to 512 (1 ECC block) or 2048 bytes (4 ECC blocks).
- **3** ECC block size: 1024 bytes. Used for devices with page size equal to 2048 bytes.
- **4~** Reserved.

ADRMODE Address mode. This field specifies the input address format.

- **0** Normal input address mode, in which the half page identifier is not specified in the address assignment but in the command set. As in **Table 52**, A7 to A0 identifies the byte address within half a page, A12 to A9 specifies the page address within a block, and other bits specify the block address. The mode is used mostly for the device with 512 bytes page size.
- **1** Large size input address mode, in which all address information is specified in the address assignment rather than in the command set. As in **Table 53**, A11 to A0 identifies the byte address within a page. The mode is used for the device with 2048 bytes page size and 8bits I/O interface.

- **2** Large size input address mode. As in **Table 53**, A10 to A0 identifies the column address within a page. The mode is used for the device with 2048 byte page size and 16bits I/O interface.

	NLD7	NLD6	NLD5	NLD4	NLD3	NLD2	NLD1	NLD0
First cycle	A7	A6	A5	A4	A3	A2	A1	A0
Second cycle	A16	A15	A14	A13	A12	A11	A10	A9

Table 52 Page address assignment of the first type (ADRMODE = 0)

	NLD7	NLD6	NLD5	NLD4	NLD3	NLD2	NLD1	NLD0
First cycle	A7	A6	A5	A4	A3	A2	A1	A0
Second cycle	0	0	0	0	A11	A10	A9	A8

Table 53 Page address assignment of the second type (ADRMODE = 1 or 2)

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PSIZE Page Size.

The field specifies the size of one page for the device. Two most widely used page size are supported.

0 The page size is 512 bytes or 528 bytes (including 512 bytes data area and 16 bytes spare area).
1 The page size is 2048 bytes or 2112 bytes (including 2048 bytes data area and 64 bytes spare area).
2~ Reserved.

0x8112_0008h Operation control register NFI_OPCON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			NOB		FIFO_RST	FIFO_FLUSH		SRD							BWR	BRD
Type			W/R		WO	WO		WO							R/W	R/W
Reset			0		0	0		0							0	0

This register controls the burst mode and the single of the data access. In burst mode, the core supposes there are one or more than one page of data to be accessed. On the contrary, in single mode, the core supposes there are only less than 4 bytes of data to be accessed. This is recommended to reset the state machine, data FIFO and flush the data FIFO before starting a new command sequence.

BRD *Burst read mode.* Setting this field to be logic-1 enables the data read operation. The NFI core will issue read cycles to retrieve data from the device when the data FIFO is not full or the device is not in the busy state. The NFI core supports consecutive page reading. A page address counter is built in. If the reading reaches to the end of the page, the device will enter the busy state to prepare data of the next page, and the NFI core will automatically pause reading and remain inactive until the device returns to the ready state. The page address counter will restart to count from 0 after the device returns to the ready state and start retrieving data again.

BWR *Burst write mode.* Setting to be logic-1 enables the data burst write operation for DMA operation. Actually the NFI core will issue write cycles once if the data FIFO is not empty even without setting this flag. But if DMA is to be utilized, the bit should be enabled. If DMA is not to be utilized, the bit didn’t have to be enabled.

SRD Setting to be logic-1 initializes the one-shot data read operation. It’s mainly used for read ID and read status command, which requires no more than 4 read cycles to retrieve data from the device.

NOB The field represents the number of bytes to be retrieved from the device in single mode, and the number of bytes per AHB transaction in both single and burst mode.

0 Read 4 bytes from the device.
1 Read 1 byte from the device.
2 Read 2 bytes from the device.
3 Read 3 bytes from the device.

FIFO_RST Reset the state machine and data FIFO.

FIFO_FLUSH Flush the data FIFO.

0x8112_0010h Command register NFI_CMD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CMD							
Type									R/W							

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Reset									45							

This is the command input register. The user should write this register to issue a command. Please refer to device datasheet for the command set. The core can issue some associated commands automatically. Please check out register **NFI_CON** for those commands.

CMD Command word.

0x8112_0020h Address length register NFI_ADDRNOB

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													ADDR_NOB			
Type													R/W			
Reset													0			

This register represents the number of bytes corresponding to current command. The valid number of bytes ranges from 1 to 8. The address format depends on what device to be used and what commands to be applied. The NFI core is made transparent to those different situations except that the user has to define the number of bytes.
The user should write the target address to the address register **NFI_ADDRL** before programming this register.

ADDR_NOB Number of bytes for the address

0x8112_0024h Least significant address register NFI_ADDRL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADDR3								ADDR2							
Type	R/W								R/W							
Reset	0								0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADDR1								ADDR0							
Type	R/W								R/W							
Reset	0								0							

This defines the least significant 4 bytes of the address field to be applied to the device. Since the device bus width is 1 byte, the NFI core arranges the order of address data to be least significant byte first. The user should put the first address byte in the field **ADDR0**, the second byte in the field **ADDR1**, and so on.

ADDRn The n-th address byte.

0x8112_0028h Most significant address register NFI_ADDRM

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADDR7								ADDR6							
Type	R/W								R/W							
Reset	0								0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADDR5								ADDR4							
Type	R/W								R/W							
Reset	0								0							

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This register defines the most significant byte of the address field to be applied to the device. The NFI core supports address size up to 8 bytes. Programming this register implicitly indicates that the number of address field is larger than 4.

ADDRn The n-th address byte.

0x8112_0030h Write data buffer NFI_DATAW

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DW3								DW2							
Type	R/W								R/W							
Reset	0								0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DW1								DW0							
Type	R/W								R/W							
Reset	0								0							

This is the write port of the data FIFO. It supports word access. The least significant byte **DW0** is to be programmed to the device first, then **DW1**, and so on.
If the data to be programmed is not word aligned, byte write access will be needed. Instead, the user should use another register **NFI_DATAWB** for byte programming. Writing a word to **NFI_DATAW** is equivalent to writing four bytes **DW0**, **DW1**, **DW2**, **DW3** in order to **NFI_DATAWB**. Be reminded that the word alignment is from the perspective of the user. The device bus is byte-wide. According to the flash's nature, the page address will wrap around once it reaches the end of the page.

DW3 Write data byte 3.
DW2 Write data byte 2.
DW1 Write data byte 1.
DW0 Write data byte 0.

0x8112_0034h Write data buffer for byte access NFI_DATAWB

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DW0							
Type									R/W							
Reset									0							

This is the write port for the data FIFO for byte access.

DW0 Write data byte.

0x8112_0038h Read data buffer NFI_DATAR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DR3								DR2							
Type	RO								RO							
Reset	0								0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DR1								DR0							
Type	RO								RO							
Reset	0								0							

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This is the read port of the data FIFO. It supports word access. The least significant byte **DR0** is the first byte read from the device, then **DR1**, and so on.

DR3 Read data byte 3.
DR2 Read data byte 2.
DR1 Read data byte 1.
DR0 Read data byte 0.

0x8112_003Ch Read data buffer for byte access NFI_DATARB

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DR0							
Type									RO							
Reset									0							

This is the read port of the data FIFO for byte access.
DR0 Read data byte 0.

0x8112_0040h NFI status NFI_PSTA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				NAND_FSM									NFI_FSM			
Type				RO									RO			
Reset				0									0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							NAND_BUSY	BUSY					DATAW	DATAR	ADDR	CMD
Type							RO	RO					RO	RO	RO	RO
Reset							0	0*					0	0	0	0

This register represents the NFI core control status including command mode, address mode, data program and read mode. The user should poll this register for the end of those operations.

*The value of **BUSY/NAND_BUSY** bit depends on the GPIO configuration. If GPIO is configured for NAND flash application, the reset value should be 0, which represents that NAND flash is in idle status. When the NAND flash is busy, the value will be 1.

BUSY Synchronized busy signal from the NAND flash. It's read-only. This signal is sampled from NFI
NAND_BUSY Asynchronized busy signal from the output pin of the NAND flash. It's read-only.
DATAW The NFI core is in data write mode.
DATAR The NFI core is in data read mode.
ADDR The NFI core is in address mode.
CMD The NFI core is in command mode.
NFI_FSM The field represents the state of NFI internal FSM.
- **0000** idle.
- **0001** reset. Reset command to ready
- **0010** read busy.

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0011 read data.
0100 program busy
0101 program data. Input data command to program command
1000 erase busy. Erase command to ready
1001 erase data. Erase command 1 to erase command 2

NAND_FSM The field represents the state of NAND interface FSM.
00000 IDLE. idle.
00101 CMD_WRST. command write set up
00110 CMD_WR. Command write enable.
00111 CMD_WRHD. Command write hold.
00100 CMD_WRRDY
01001 ADDR_WRST. Address write set up
01010 ADDR_WR. Address write enable
01011 ADDR_WRHD. Address write hold
01000 ADDR_WRRDY.
01100 CA2DEXT. Command address write extension.
10001 DATA_RDST. Data read set up.
10010 DATA_RD. Data read enable.
10011 DATA_RDHD. Data read hold.
11000 DATA_WRRDY.
11001 DATA_WRST. Data write set up.
11010 DATA_WR. Data write enable.
11011 DATA_WRHD. Data write hold.

0x8112_0044h FIFO Status NFI_FIFOSTA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WR_FULL	WR_EMPTY		WR_REMAIN					RD_FULL	RD_EMPTY		RD_REMAIN				
Type	RO	RO		RO					RO	RO		RO				
Reset	0	1		0					0	1		0				

The register represents the status of the data FIFO.

WR_FULL Data FIFO full in burst write mode.
WR_EMPTY Data FIFO empty in burst write mode.
RD_FULL Data FIFO full in burst read mode.
RD_EMPTY Data FIFO empty in burst read mode.
RD_REMAIN Data FIFO remaining byte number in burst read mode.

WR_REMAIN Data FIFO remaining byte number in burst write mode.

0x8112_0050h FIFO Content Data 0 NFI_FIFODATA0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	FIFO_DATA0															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_DATA0															
Type	RO															
Reset	0															

This register represents the content data 0 of fifo.

0x8112_0054h FIFO Content Data 1 NFI_FIFODATA1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_DATA1															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_DATA1															
Type	RO															
Reset	0															

This register represents the content data 1 of fifo.

0x8112_0058h FIFO Content Data 2 NFI_FIFODATA2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_DATA2															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_DATA2															
Type	RO															
Reset	0															

This register represents the content data 2 of fifo.

0x8112_005Ch FIFO Content Data 3 NFI_FIFODATA3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_DATA3															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_DATA3															
Type	RO															
Reset	0															

This register represents the content data 3 of fifo.

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0x8112_0060h NFI control NFI_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE_RW						MAIN_ECC_EN	SPARE_ECC_EN		DMA_PAUSE_EN	SPARE_EN	MULTI_PAGE_RD_EN	AUTOECC_ENC_EN	AUTOECC_DEC_EN	DMA_WR_EN	DMA_RD_EN
Type	R/W						R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0						0	0		0	0	0	0	0	0	0

The register controls the DMA and ECC functions. For all field, Setting to be logic-1 represents enabled, while 0 represents disabled.

BYTE_RW **Enable byte access**. The valid bytes read from NFI_DATAR and NFI_DATAW is only DR0 and DW0 if BYTE_RW is enabled.

SPARE_EN If enabled, the NFI core allows the user to program or read the spare area directly. Otherwise, the spare area can be programmed or read by the core.

MULTI_PAGE_RD_EN Multiple page burst read enable. If enabled, the burst read operation could continue through multiple pages within a block. It's also possible and more efficient to associate with DMA scheme to read a sector of data contained within the same block.

AUTOECC_ENC_EN Automatic ECC encoding enable. If enabled, the ECC parity is written automatically to the spare area. If disable ECC encoding engine, it write the default parity in the spare area.

AUTOECC_DEC_EN Automatic ECC decoding enabled, the error checking and correcting are performed automatically on the data read from the memory and vice versa. If enabled, when the page address reaches the end of the data read of one page

DMA_WR_EN This field is used to control the activity of DMA write transfer.

DMA_RD_EN This field is used to control the activity of DMA read transfer.

DMA_PAUSE_EN DMA pause

MAIN_ECC_EN This field is used to enable generation of ECC parities for main area.

SPARE_ECC_EN This field is used to enable generation of ECC parities for spare area. If **SPARE_EN** is not set, however, the mode can't be enabled since the core can't access the spare area.

0x8112_0064h Interrupt status register NFI_INTR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				BUSY_RETURN	ERRS_COR3	ERRS_COR2	ERRS_COR1	ERRS_COR0	ERR_COR7	ERR_COR6	ERR_COR5	ERR_COR4	ERR_COR3	ERR_COR2	ERR_COR1	ERR_COR0
Type				RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERASE_COMPLETE	RESET_COMPLETE	WR_COMPLETE	RD_COMPLETE	ERRS_DET3	ERRS_DET2	ERRS_DET1	ERRS_DET0	ERR_DET7	ERR_DET6	ERR_DET5	ERR_DET4	ERR_DET3	ERR_DET2	ERR_DET1	ERR_DET0
Type	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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The register indicates the status of all the interrupt sources. Read this register will clear all interrupts.

BUSY_RETURN	Indicates that the device state returns from busy by inspecting the R/B# pin.
ERR_CORn	Indicates that the single bit error in ECC block n needs to be corrected.
ERR_DETn	Indicates an uncorrectable error in ECC block n.
ERRS_CORn	Indicates that the single bit error in spare ECC block n needs to be corrected.
ERRS_DETn	Indicates an uncorrectable error in spare ECC block n.
ERASE_COMPLETE	Indicates that the erase operation is completed.
RESET_COMPLETE	Indicates that the reset operation is completed.
WR_COMPLETE	Indicates that the write operation is completed.
RD_COMPLETE	Indicates that the single page read operation is completed.

0x8112_0068h Interrupt enable register NFI_INTR_EN

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				BUSY_RETURN_EN	ERRS_COR3_EN	ERRS_COR2_EN	ERRS_COR1_EN	ERRS_COR0_EN	ERR_COR7_EN	ERR_COR6_EN	ERR_COR5_EN	ERR_COR4_EN	ERR_COR3_EN	ERR_COR2_EN	ERR_COR1_EN	ERR_COR0_EN
Type				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERASE_COMPLETE_EN	RESET_COMPLETE_EN	WR_COMPLETE_EN	RD_COMPLETE_EN	ERRS_DET3_EN	ERRS_DET2_EN	ERRS_DET1_EN	ERRS_DET0_EN	ERR_DET7_EN	ERR_DET6_EN	ERR_DET5_EN	ERR_DET4_EN	ERR_DET3_EN	ERR_DET2_EN	ERR_DET1_EN	ERR_DET0_EN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register controls the activity for the interrupt sources.

ERR_CORn_EN	The error correction interrupt enable for the n ECC block.
ERR_DETn_EN	The error detection interrupt enable for the n ECC block.
ERRS_DETn_EN	The error detection interrupt enable for the n spare ECC block.
ERRS_DETn_EN	The error detection interrupt enable for the n spare ECC block.
BUSY_RETURN_EN	The busy return interrupt enable.
ERASE_COMPLETE_EN	The erase completion interrupt enable.
RESET_COMPLETE_EN	The reset completion interrupt enable.
WR_COMPLETE_EN	The single page write completion interrupt enable.
RD_COMPLETE_EN	The single page read completion interrupt enable.

NFI+0070h NAND flash page counter NFI_PAGECNTR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CNTR							
Type									RO							
Reset									0							

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The register represents the number of pages that the NFI has read since the issuing of the read command. For some devices, the data can be read consecutively through different pages without the need to issue another read command. The user can monitor this register to know current page count, particularly when read DMA is enabled.

CNTR The page counter.

NFI+0074h NAND flash page address counter NFI_ADDRCNTR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CNTR											
Type					RO											
Reset					0											

The register represents the current read/write address with respect to initial address input. It counts in unit of byte. In page read and page program operation, the address should be the same as that in the state machine in the target device.

NFI supports the address counter up to 4096 bytes.

CNTR The address count.

0x8112_0080h ECC block 0 parity error detect syndrome address NFI_ SYM0_ADDR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SYM									
Type							RO									
Reset							0									

This register identifies the address within ECC block 0 that a single bit error has been detected.

SYM The byte address of the error-correctable bit.

Register Address	Register Function	Acronym
0x8112_0080h	NFI ECC Syndrome address 0	NFI_SYM0_ADDR
0x8112_0084h	NFI ECC Syndrome address 1	NFI_SYM1_ADDR
0x8112_0088h	NFI ECC Syndrome address 2	NFI_SYM2_ADDR
0x8112_008Ch	NFI ECC Syndrome address 3	NFI_SYM3_ADDR
0x8112_0090h	NFI ECC Syndrome address 4	NFI_SYM4_ADDR
0x8112_0094h	NFI ECC Syndrome address 5	NFI_SYM5_ADDR
0x8112_0098h	NFI ECC Syndrome address 6	NFI_SYM6_ADDR
0x8112_009Ch	NFI ECC Syndrome address 7	NFI_SYM7_ADDR
0x8112_00A0h	NFI Spare ECC Syndrome address 0	NFI_SYMS0_ADDR
0x8112_00A4h	NFI Spare ECC Syndrome address 1	NFI_SYMS1_ADDR
0x8112_00A8h	NFI Spare ECC Syndrome address 2	NFI_SYMS2_ADDR
0x8112_00ACh	NFI Spare ECC Syndrome address 3	NFI_SYMS3_ADDR

Table 54 NFI Syndrome address register table

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0x8112_00B0h ECC block 0 parity error detect syndrome word NFI_SYM0_DATA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ED3								ED2							
Type	RO								RO							
Reset	0								0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ED1								ED0							
Type	RO								RO							
Reset	0								0							

This register represents the syndrome word for the corrected ECC block 0. To correct the error, the user should first read **NFI_ SYM0_ADDR** for the address of the correctable word, and then read **NFI_SYM0_DAT**, directly XOR the syndrome word with the data word to obtain the correct word.

Register Address	Register Function	Acronym
0x8112_00B0h	NFI ECC Syndrome data 0	NFI_SYM0_DATA
0x8112_00B4h	NFI ECC Syndrome data 1	NFI_SYM1_DATA
0x8112_00B8h	NFI ECC Syndrome data 2	NFI_SYM2_DATA
0x8112_00BCh	NFI ECC Syndrome data 3	NFI_SYM3_DATA
0x8112_00C0h	NFI ECC Syndrome data 4	NFI_SYM4_DATA
0x8112_00C4h	NFI ECC Syndrome data 5	NFI_SYM5_DATA
0x8112_00C8h	NFI ECC Syndrome data 6	NFI_SYM6_DATA
0x8112_00CCh	NFI ECC Syndrome data 7	NFI_SYM7_DATA
0x8112_00D0h	NFI Spare ECC Syndrome data 0	NFI_SYMS0_DATA
0x8112_00D4h	NFI Spare ECC Syndrome data 1	NFI_SYMS1_DATA
0x8112_00D8h	NFI Spare ECC Syndrome data 2	NFI_SYMS2_DATA
0x8112_00DCh	NFI Spare ECC Syndrome data 3	NFI_SYMS3_DATA

Table 55 NFI Syndrome data register table

0x8112_00E0h NFI ECC parity word 0 NFI_PAR_0P

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PAR												
Type				RO												
Reset				0												

This register represents the ECC parity for the ECC block 0. It's calculated by the NFI core and can be read by the user. It's generated when writing or reading a page.

Register Address	Register Function	Acronym
0x8112_00E0h	NFI ECC parity word 0	NFI_PAR_0P
0x8112_00E4h	NFI ECC parity word 0	NFI_PAR_0C

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0x8112_00E8h	NFI ECC parity word 1	NFI_PAR_1P
0x8112_00ECh	NFI ECC parity word 1	NFI_PAR_1C
0x8112_00F0h	NFI ECC parity word 2	NFI_PAR_2P
0x8112_00F4h	NFI ECC parity word 2	NFI_PAR_2C
0x8112_00F8h	NFI ECC parity word 3	NFI_PAR_3P
0x8112_00FCh	NFI ECC parity word 3	NFI_PAR_3C
0x8112_0100h	NFI ECC parity word 4	NFI_PAR_4P
0x8112_0104h	NFI ECC parity word 4	NFI_PAR_4C
0x8112_0108h	NFI ECC parity word 5	NFI_PAR_5P
0x8112_010Ch	NFI ECC parity word 5	NFI_PAR_5C
0x8112_0110h	NFI ECC parity word 6	NFI_PAR_6P
0x8112_0114h	NFI ECC parity word 6	NFI_PAR_6C
0x8112_0118h	NFI ECC parity word 7	NFI_PAR_7P
0x8112_011Ch	NFI ECC parity word 7	NFI_PAR_7C
0x8112_0120h	NFI ECC parity word 0	NFI_PARS_0P
0x8112_0124h	NFI ECC parity word 0	NFI_PARS_0C
0x8112_0128h	NFI ECC parity word 1	NFI_PARS_1P
0x8112_012Ch	NFI ECC parity word 1	NFI_PARS_1C
0x8112_0130h	NFI ECC parity word 2	NFI_PARS_2P
0x8112_0134h	NFI ECC parity word 2	NFI_PARS_2C
0x8112_0138h	NFI ECC parity word 3	NFI_PARS_3P
0x8112_013Ch	NFI ECC parity word 3	NFI_PARS_3C

Table 56 NFI parity bits register table

0x8112_0140h NFI ECC error detect indication register NFI_ERRDET

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CES_BLK3	CES_BLK2	CES_BLK1	CES_BLK0	CE_BLK7	CE_BLK6	CE_BLK5	CE_BLK4	CE_BLK3	CE_BLK2	CE_BLK1	CE_BLK0
Type					RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ESBLK3	ESBLK2	ESBLK1	ESBLK0	EBLK7	EBLK6	EBLK5	EBLK4	EBLK3	EBLK2	EBLK1	EBLK0
Type					RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset					0	0	0	0	0	0	0	0	0	0	0	0

This register identifies the block in which an uncorrectable error has been detected.

EBLKn The uncorrectable errors in the block n.

CE_BLKn The correctable error of the block n.

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ESBLKn The uncorrectable errors in the spare block n.
CES_BLKn The correctable error of the spare block n.

0x8112_0144h NFI ECC parity error indication register NFI_PARERR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					PES_BLK3	PES_BLK2	PES_BLK1	PES_BLK0	PE_BLK7	PE_BLK6	PE_BLK5	PE_BLK4	PE_BLK3	PE_BLK2	PE_BLK1	PE_BLK0
Type					RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					NO_ESBLK3	NO_ESBLK2	NO_ESBLK1	NO_ESBLK0	NO_EBLK7	NO_EBLK6	NO_EBLK5	NO_EBLK4	NO_EBLK3	NO_EBLK2	NO_EBLK1	NO_EBLK0
Type					RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset					0	0	0	0	0	0	0	0	0	0	0	0

This register identifies the block in which an uncorrectable error has been detected.

NO_EBLKn No errors in the block n.
PE_BLKn The correctable error in parities of the block n.
NO_ESBLKn No errors in the spare block n.
PES_BLKn The correctable error in parities of the spare block n.

NFI+0148h NFI Spare ECC Control register NFI_SCON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SPARE_ECC_STR							SPARE_ECC_NUM			
Type						R/W							R/W			
Reset						0							0			

The register is used to control ECC for spare data.

SPARE_ECC_NUM byte number in spare for ECC. (0-8)
SPARE_ECC_STR start byte number in spare for ECC. (0-7)

NFI+0200h NFI device select register NFI_CSEL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CSEL
Type																R/W
Reset																0

The register is used to select the target device. It decides which CEB pin to be functional. This is useful while using the high-density device.

CSEL Chip select. The value defaults to 0.
- **0** Device 1 is selected.
- **1** Device 2 is selected.

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NFI+0204h NFI IO Control register NFI_IOCON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																NLD_PD
Type																R/W
Reset																0

Data bus pull down when no use.

NLD_PD data bus pull down when no use.

- **0** disable.
- **1** enable.

6.3.3 Control and Timing

6.3.3.1 Device timing control

This section illustrates the timing diagram.

The ideal timing for write access is listed as listed in **Table 57**.

Parameter	Description	Timing specification	Timing at 13MHz (WST, WH) = (0,0)	Timing at 26MHz (WST, WH) = (0,0)	Timing at 52MHz (WST, WH) = (1,0)
T_{WC1}	*Write cycle time*	3T + WST + WH	230.8ns	105.4ns	76.9ns
T_{WC2}	*Write cycle time*	2T + WST + WH	153.9ns	76.9ns	57.7ns
T_{DS}	*Write data setup time*	1T + WST	76.9ns	38.5ns	38.5ns
T_{DH}	*Write data hold time*	1T + WH	76.9ns	38.5ns	19.2ns
T_{WP}	*Write enable time*	1T + WST	76.9ns	38.5ns	38.5ns
T_{WH}	*Write high time*	1T + WH	76.9ns	38.5ns	19.2ns
T_{CLS}	*Command latch enable setup time*	1T	76.9ns	38.5ns	19.2ns
T_{CLH}	*Command latch enable hold time*	1T + WH	76.9ns	38.5ns	19.2ns
T_{ALS}	*Address latch enable setup time*	1T	76.9ns	38.5ns	19.2ns
T_{ALH}	*Address latch enable hold time*	1T + WH	76.9ns	38.5ns	19.23ns
F_{WC}	*Write data rate*	1 / T_{WC2}	6.5Mbytes/s	13Mbytes/s	17.3Mbytes/s

Table 57 Write access timing

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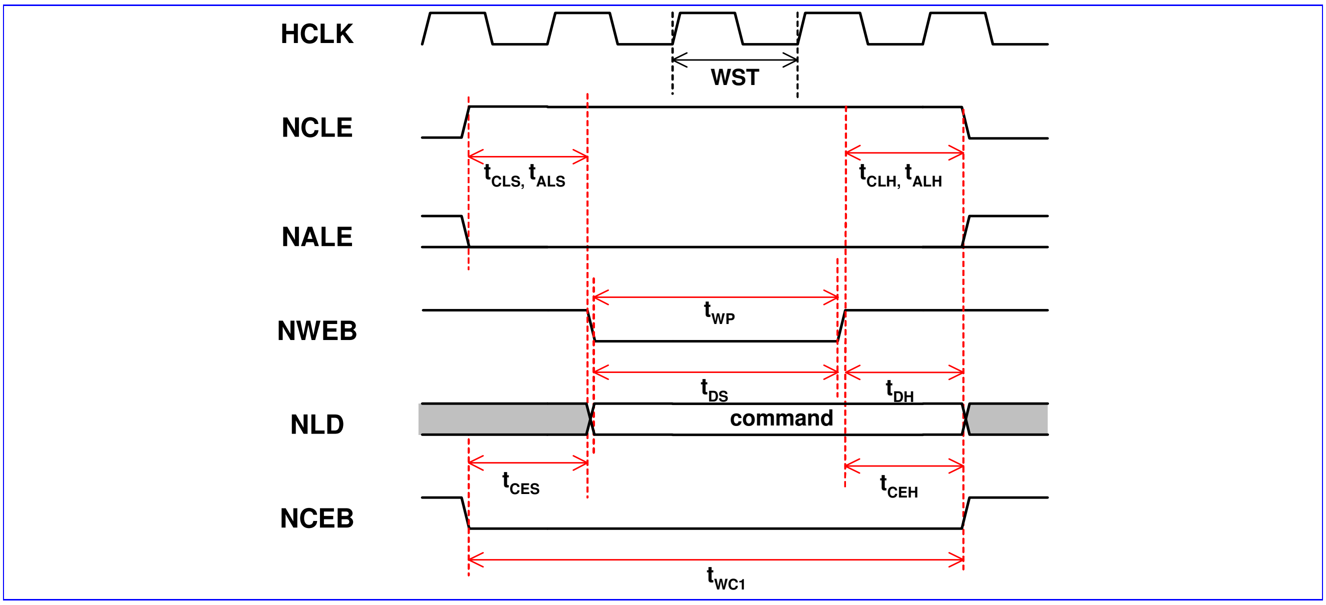

Figure 64 Command input cycle (1 wait state).

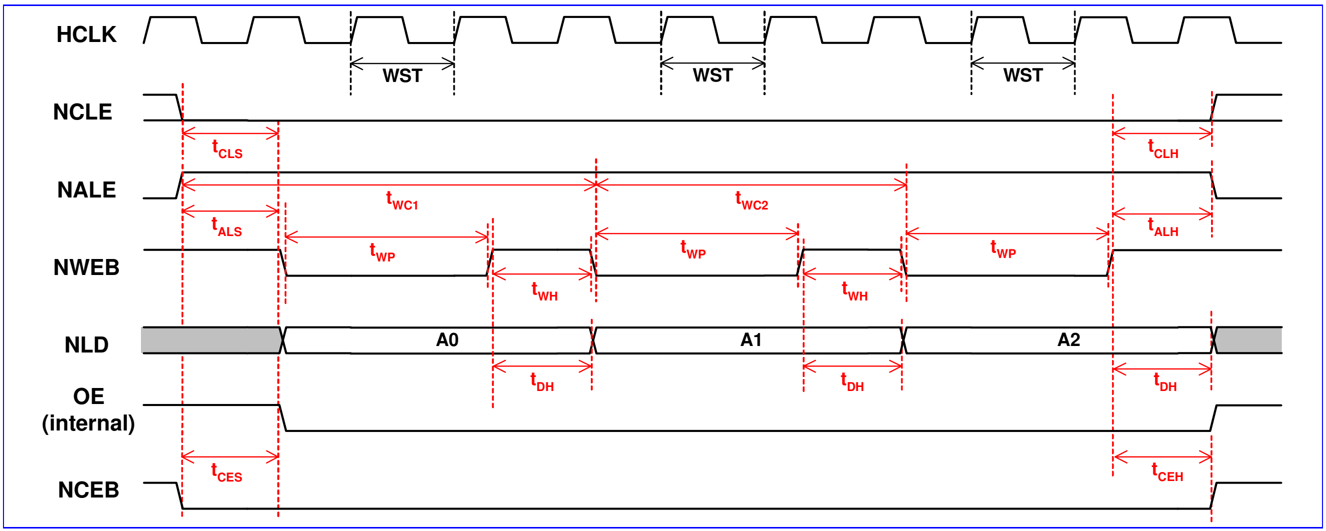

Figure 65 Address input cycle (1 wait state)

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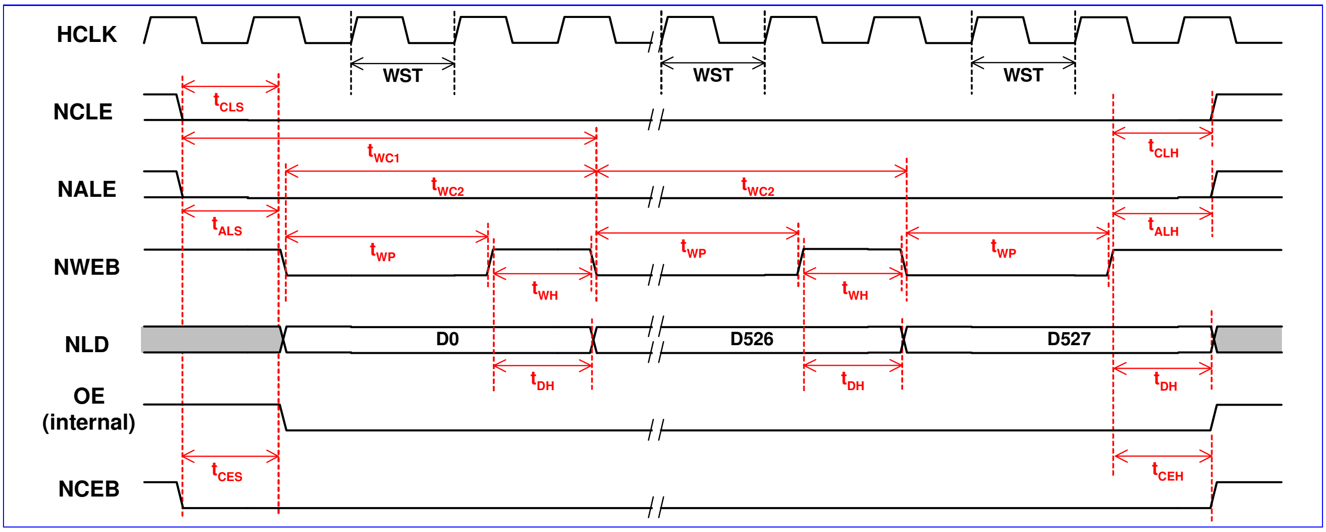

Figure 66 Consecutive data write cycles (1 wait state, 0 hold time extension)

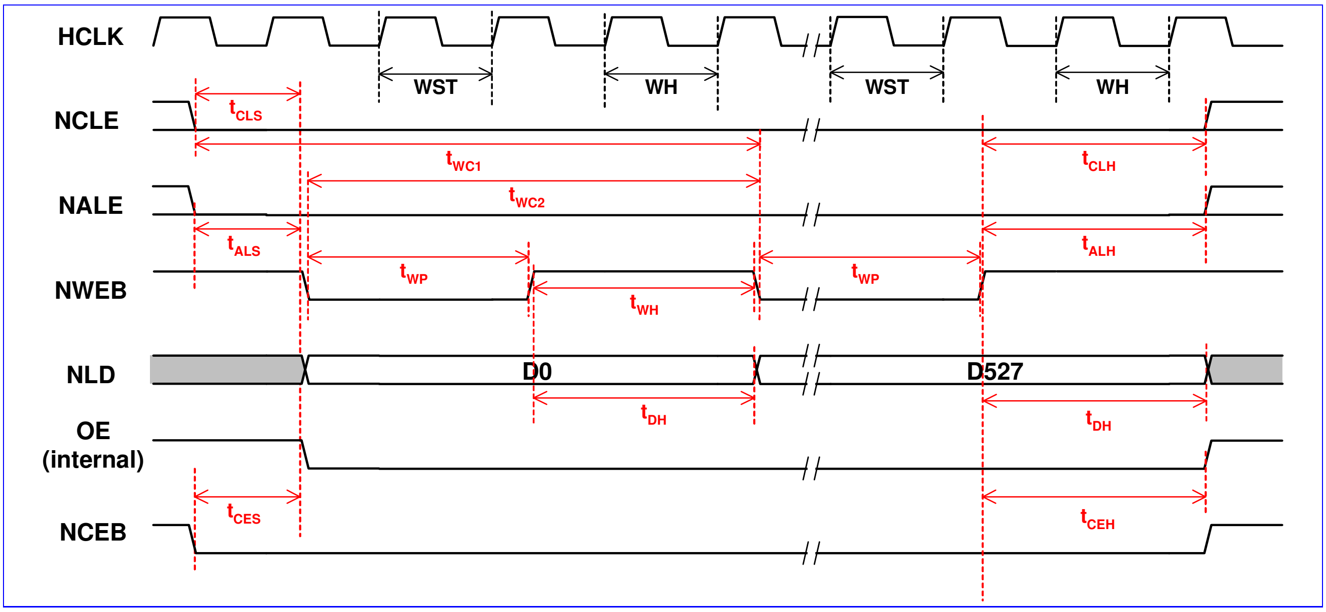

Figure 67 Consecutive data write cycles (1 wait state, 1 hold time extension)

The ideal timing for read access is as listed in **Table 58**.

Parameter	Description	Timing specification	Timing at 13MHz (RLT, WH) = (0,0)	Timing at 26MHz (RLT, WH) = (1,0)	Timing at 52MHz (RLT, WH) = (2,0)
T_{RC1}	*Read cycle time*	3T + RLT + WH	230.8ns	153.8ns	96.2ns
T_{RC2}	*Read cycle time*	2T + RLT + WH	153.9ns	115.4ns	76.9ns

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T_{DS}	*Read data setup time*	1T + RLT	76.9ns	76.9ns	57.7ns
T_{DH}	*Read data hold time*	1T + WH	76.9ns	38.5ns	19.2ns
T_{RP}	*Read enable time*	1T + RLT	76.9ns	76.9ns	57.7ns
T_{RH}	*Read high time*	1T + WH	76.9ns	38.5ns	19.2ns
T_{CLS}	*Command latch enable setup time*	1T	76.9ns	38.5ns	19.2ns
T_{CLH}	*Command latch enable hold time*	1T + WH	76.9ns	38.5ns	19.2ns
T_{ALS}	*Address latch enable setup time*	1T	76.9ns	38.5ns	19.2ns
T_{ALH}	*Address latch enable hold time*	1T + WH	76.9ns	38.5ns	19.2ns
F_{RC}	*Write data rate*	1 / T_{RC2}	6.5Mbytes/s	8.7Mbytes/s	13Mbytes/s

Table 58 Read access timing

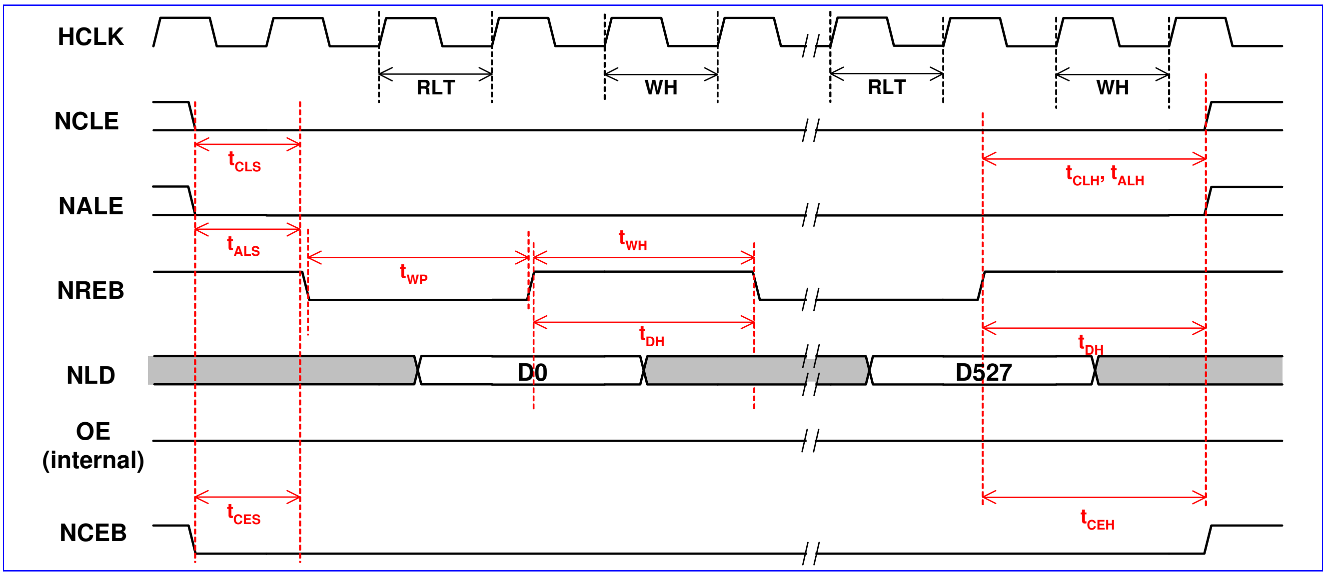

Figure 68 Serial read cycle (1 wait state, 1 hold time extension)

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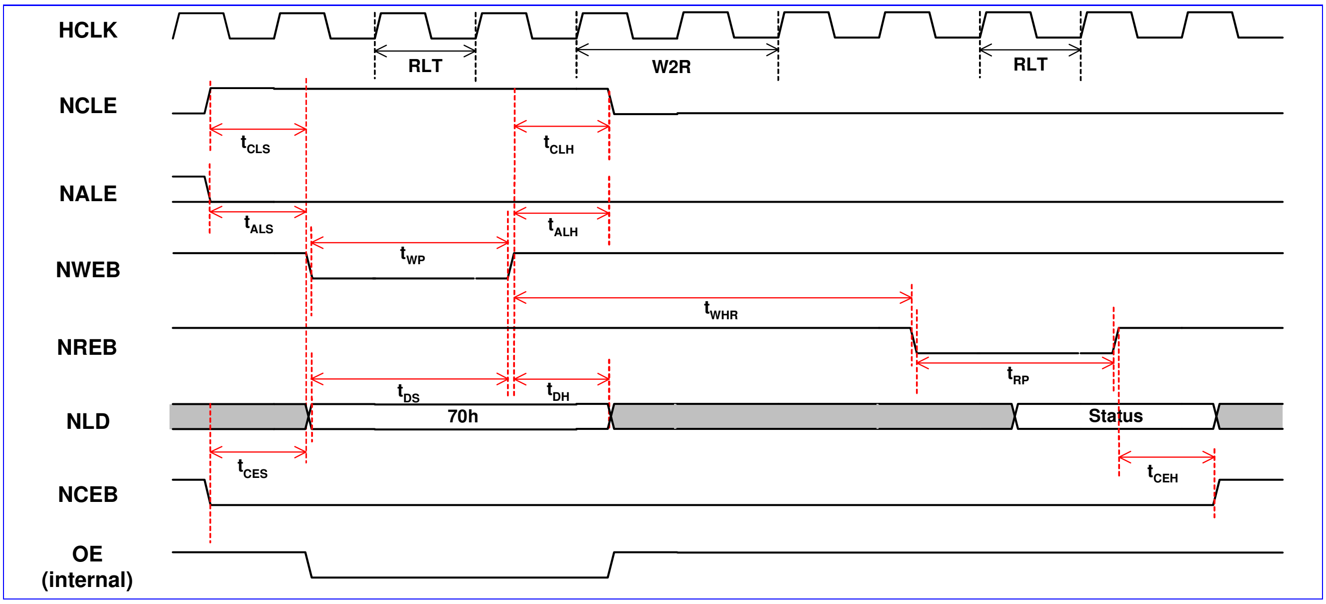

Figure 69 Status read cycle (1 wait state)

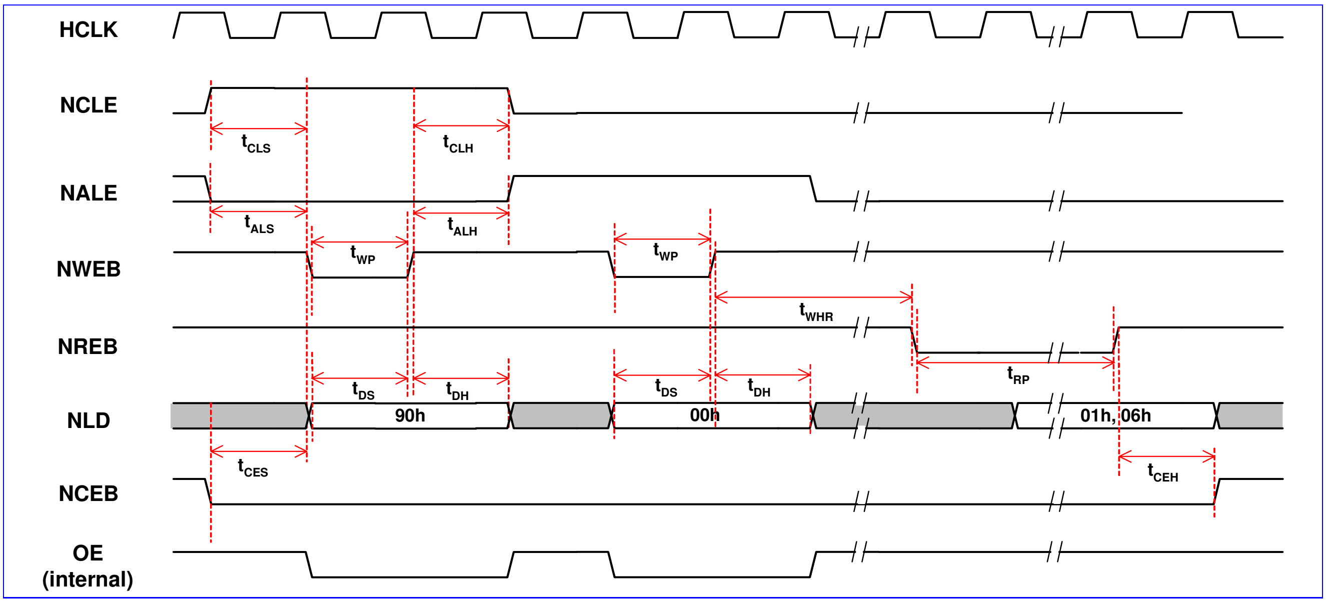

Figure 70 ID and manufacturer read (0 wait state)

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6.4 USB 2.0 High-Speed Dual-Role Controller

6.4.1 General Description

The USB2.0 Controller can support 4 Tx and 2 Rx endpoints(excluding Endpoint 0). These endpoints can be individually configured in software to handle either Bulk transfers, Interrupt transfers or Isochronous transfers. There are 2 DMA channels and the embedded RAM size is 1152bytes. The embedded RAM can be dynamically configured to each endpoint. When acting as the host for point-to-point communications, the controller maintains a frame counter and automatically schedules SOF, Isochronous, Interrupt and Bulk transfers.

Here is provided features.

- Operates either as the host/peripheral in point-to-point communications with another USB function or as a function controller for a USB peripheral
- Supports point-to-point communications with one high-, full-, or low-speed device
- Supports Suspend and Resume signaling
- Supports High-Bandwidth Isochronous & Interrupt transfers
- UTMI+ Level 2 Transceiver Interface
- Synchronous RAM interface for FIFOs
- Support for DMA access to FIFOs
- Software connect/disconnect option
- Supports multi-layer operations on the AHB bus
- Performs all transaction scheduling in hardware

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The USB2.0 Controller Block Diagram is as illustrated.

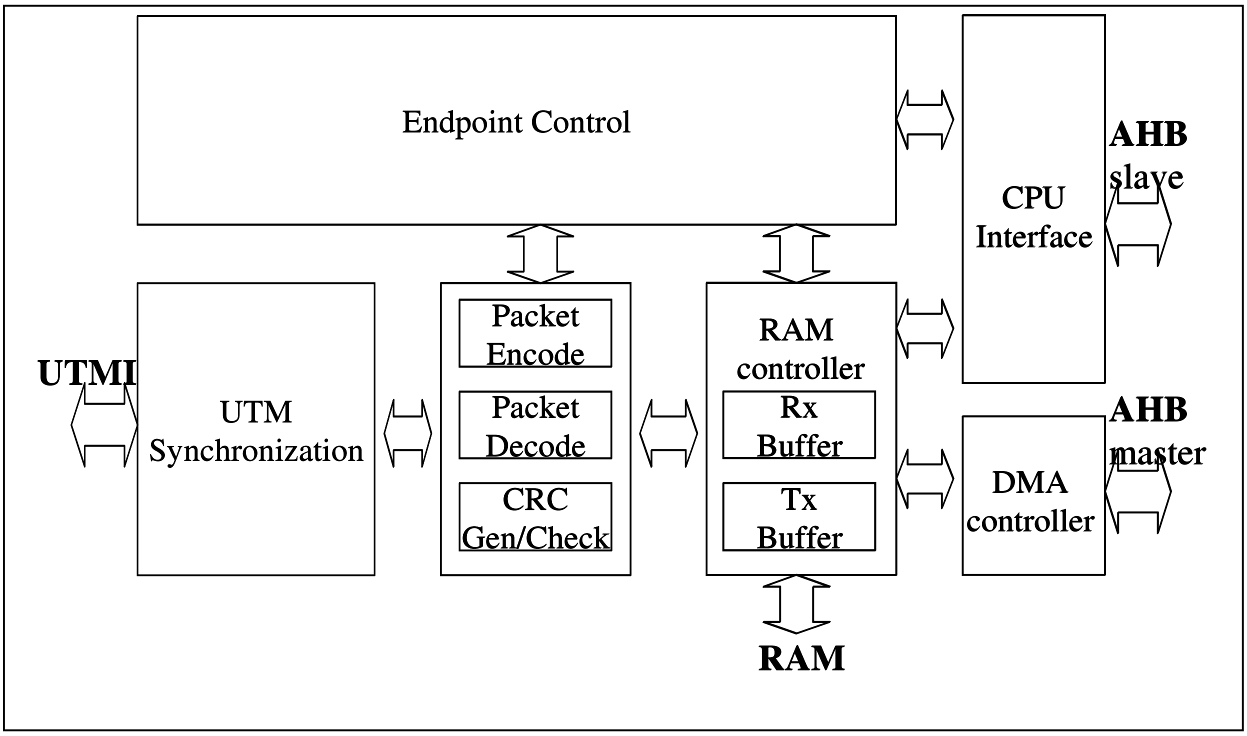

Figure 71 USB Controller Block diagram

6.4.2 Register Definitions

REGISTER ADDRESS	REGISTER NAME	SYNONYM
USB + 0000h	Function Address Register	FADDR
USB + 0001h	Power Management Register	POWER
USB + 0002h	Tx Interrupt Status Register	INTRTX
USB + 0004h	Rx Interrupt Status Register	INTRRX
USB + 0006h	Tx Interrupt Enable Register	INTRTXE
USB + 0008h	Rx Interrupt Enable Register	INTRRXE
USB + 000Ah	Common USB interrupts Register	INTRUSB
USB + 000Bh	Common USB interrupts Enable Register	INTRUSBE
USB + 000Ch	Frame Number Register	FRAME
USB + 000Eh	Endpoint Selecting Index Register	INDEX
USB + 000Fh	Test Mode Enable Register	TESTMODE

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USB + 0010h ~ USB + 001Fh	It maps to CSR EP0 ~ EP5 depends on INDEX	Indexed CSR
USB + 0020h	USB Endpoint 0 FIFO Register	FIFO0
USB + 0024h	USB Endpoint 1 FIFO Register	FIFO1
USB + 0028h	USB Endpoint 2 FIFO Register	FIFO2
USB + 002Ch	USB Endpoint 3 FIFO Register	FIFO3
USB + 0030h	USB Endpoint 4 FIFO Register	FIFO4
USB + 0061h	Power Up Counter Register	PWRUPCNT
USB + 0062h	Tx FIFO Size Register	TXFIFOSZ
USB + 0063h	Rx FIFO Size Register	RXFIFOSZ
USB + 0064h	Tx FIFO Address Register	TXFIFOADD
USB + 0066h	Rx FIFO Address Register	RXFIFOADD
USB + 006Ch	Hardware version Register	HWVERS
USB + 0070h	Software Reset Register	SWRST
USB + 0078h	Info. about number of Tx and Rx Register	EPINFO
USB + 0079h	Info. about the width of RAM and the number of DMA channel Register	RAMINFO
USB + 007Ah	Info. about delay to be applied Register	LINKINFO
USB + 007Bh	VBus Pulsing Charge Register	VPLEN
USB + 007Ch	Time buffer available on HS transactions Register	HS_EOF1
USB + 007Dh	Time buffer available on FS transactions Register	FS_EOF1
USB + 007Eh	Time buffer available on LS transactions Register	LS_EOF1
USB + 007Fh	RESET Information Register	RSTINFO
USB + 0102h	EP0 Control Status Register	CSR0
USB + 0108h	EP0 Received bytes Register	COUNT0
USB + 010Bh	NAK Limit Register	NAKLIMT0
USB + 010Fh	Core Configuration Register	CONFIGDATA
USB + 01n0h	TXMAP Register	TXMAP(n)
USB + 01n2h	Tx CSR Register	TXCSR(n)
USB + 01n4h	RXMAP Register	RXMAP(n)
USB + 01n6h	Rx CSR Register	RXCSR(n)
USB + 01n8h	Rx Count Register	RXCOUNT(n)
USB + 01nAh	TxType Register	TXTYPE(n)
USB + 01nBh	TxInterval Register	TXINTERVAL(n)
USB + 01nCh	RxType Register	RXTYPE(n)

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USB + 01nDh	RxInterval Register	RXINTERVAL(n)
USB + 01nFh	Configured FIFO Size Register	FIFOSIZE(n)
	n stands for endpoint number. For example, endpoint 1's n = 1.	
USB + 0200h	DMA Interrupt Status Register	DMA_INTR
USB + 0204h	DMA Channel 1 Control Register	DMA_CNTL1
USB + 0208h	DMA Channel 1 ADDRESS Register	DMA_ADDR1
USB + 020Ch	DMA Channel 1 BYTE COUNT Register	DMA_COUNT1
USB + 0210h	DMA Channel 1 Limiter Register	DMA_LIMITER1
USB + 0214h	DMA Channel 2 Control Register	DMA_CNTL2
USB + 0218h	DMA Channel 2 ADDRESS Register	DMA_ADDR2
USB + 021Ch	DMA Channel 2 BYTE COUNT Register	DMA_COUNT2
USB + 0284h	DMA Channel 1 PingPong Control Register	DMA_PP_CNTL1
USB + 0288h	DMA Channel 1 PingPong Address Register	DMA_PP_ADDR1
USB + 028Ch	DMA Channel 1 PingPong Count Register	DMA_PP_CNT1
USB + 0294h	DMA Channel 2 PingPong Control Register	DMA_PP_CNTL2
USB + 0298h	DMA Channel 2 PingPong Address Register	DMA_PP_ADDR2
USB + 029Ch	DMA Channel 2 PingPong Count Register	DMA_PP_CNT2
USB + 0300h	EP1 RxPktCount Register	EP1RXPKTCOUNT
USB + 0302h	EP2 RxPktCount Register	EP2RXPKTCOUNT
USB + 0304h	EP3 RxPktCount Register	EP3RXPKTCOUNT
USB + 0308h	EP4 RxPktCount Register	EP4RXPKTCOUNT
USB + 0400h	DMA Channel 1 Real Count Register	DMA_REALCNT1
USB + 0404h	DMA Channel 1 PingPong Real Count Register	DMA_PP_REALCNT1
USB + 0408h	DMA Channel 1 Timer Register	DMA_Timer1
USB + 0410h	DMA Channel 2 Real Count Register	DMA_REALCNT2
USB + 0414h	DMA Channel 2 PingPong Real Count Register	DMA_PP_REALCNT2
USB + 0418h	DMA Channel 2 Timer Register	DMA_Timer2
USB + 0600h	PHY Control Register 1	PHYCR1
USB + 0604h	PHY Control Register 2	PHYCR2
USB + 0608h	PHY Control Register 3	PHYCR3
USB + 060Ch	PHY Control Register 4	PHYCR4
USB + 0610h	PHY Control Register 5	PHYCR5
USB + 0614h	PHY UTMI Interface Register 1	PHYIR1
USB + 0618h	PHY UTMI Interface Register 2	PHYIR2
USB + 061ch	PHY UTMI Interface Register 3	PHYIR3

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Table 59 USB Register Mapping Table

USB COTROL REGISTER

USB+0000h Function Address Register FADDR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										FUNCTION ADDRESS						
Type										R/W						
Reset										0						

FUNCTION ADDRESS FAddr is an 8-bit register that should be written with the 7-bit address of the peripheral part of the transaction. When the USB2.0 controller is being used in Peripheral mode (DevCtl.bit2=0), this register should be written with the address received through a SET_ADDRESS command, which will then be used for decoding the function address in subsequent token packets. When the USB2.0 controller is being used in Host mode (DevCtl.bit2=1), this register should be set to the value sent in a SET_ADDRESS command during device enumeration as the address for the peripheral device.

Peripheral Mode

USB+0001h Power Management Register POWER

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ISOUPDATE	SOFTCONN	HSENAB	HSMODE	RESET	RESUME	SUSPENDMODE	ENABLE_SUSPENDM
Type									R/W	R/W	R/W	R	R	R/W	R	R/W
Reset									0	0	1	0	0	0	0	0

Host Mode

USB+0001h Power Management Register POWER

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												HSENAB	HSMODE	RESUME	SUSPENDMODE	ENABLESUSPENDM
Type												R/W	R	R/W	Set	R/W
Reset												1	0	0	0	0

ENABLE_SUSPENDM Set by the CPU to enable the SUSPENDM output

SUSPENDMODE In Host mode, this bit is set by the CPU to enter Suspend mode. In Peripheral mode, this bit is set on entryo into Suspend mode. It is cleared when the CPU reads the interrupt register, or sets the Resume bit above.

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RESUME Set by the CPU to generate Resume signaling when the function is in Suspend mode. The CPU should clear this bit after 10 ms (a maximum of 15 ms) to end Resume signaling. In Host mode, this bit is also automatically set when Resume signaling from the target is detected while the USB2.0 controller is suspended.

RESET This bit is set when Reset signaling is present on the bus. Note: This bit is Read/Write from the CPU in Host Mode but Read-Only in Peripheral Mode.

HSMODE When set, this read-only bit indicates High-speed mode successfully negotiated during USB reset. In Peripheral Mode, becomes valid when USB reset completes (as indicated by USB reset interrupt). In Host Mode, becomes valid when Reset bit is cleared. Remains valid for the duration of the session.
Note: Allowance is made for Tiny-J signaling in determining the transfer speed to select.

HSENAB When set by the CPU, the USB2.0 controller will negotiate for High-speed mode when the device is reset by the hub. If not set, the device will only operate in Full-speed mode.

SOFTCONN If Soft Connect/Disconnect feature is enabled, then the USB D+/D- lines is enabled when this bit is set by the CPU and tri-stated when this bit is cleared by the CPU. Note: Only valid in Peripheral Mode.

ISOUPDATE When set by the CPU, the USB2.0 controller will wait for an SOF token from the time TxPktRdy is set before sending the packet. If an IN token is received before an SOF token, then a zero length data packet will be sent.Note: Only valid in Peripheral Mode. Also, this bit only affects endpoints performing Isochronous transfers.

USB+0002h Tx Interrupt Status Register INTRTX

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											EP5_TX	EP4_TX	EP3_TX	EP2_TX	EP1_TX	EP0
Type											R	R	R	R	R	R
Reset											0	0	0	0	0	0

EP0 Endpoint0 interrupt event
EP1_TX Tx Endpoint 1 interrupt event
EP2_TX Tx Endpoint 2 interrupt event
EP3_TX Tx Endpoint 3 interrupt event
EP4_TX Tx Endpoint 4 interrupt event
EP5_TX Tx Endpoint 4 interrupt event

USB+0004h Rx Interrupt Status Register INTRRX

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													EP3_RX	EP2_RX	EP1_RX	
Type													R/W	R/W	R/W	
Reset													0	0	0	

INTRRX[15:0] Rx Interrupt Status register is “write 0 clear”
EP1_RX Rx Endpoint 1 interrupt event

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EP2_RX Rx Endpoint 2 interrupt event
EP3_RX Rx Endpoint 3 interrupt event

USB+0006h Tx Interrupt Enable Register INTRTXE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											EP5_TXE	EP4_TXE	EP3_TXE	EP2_TXE	EP1_TXE	EP0_E
Type											R/W	R/W	R/W	R/W	R/W	R/W
Reset											1	1	1	1	1	1

EP0_E
- **0** Endpoint0 interrupt event disable
- **1** Endpoint0 interrupt event enable

EP1_TXE
- **0** Endpoint1 interrupt event disable
- **1** Endpoint1 interrupt event enable

EP2_TXE
- **0** Endpoint2 interrupt event disable
- **1** Endpoint2 interrupt event enable

EP3_TXE
- **0** Endpoint3 interrupt event disable
- **1** Endpoint3 interrupt event enable

EP4_TXE
- **0** Endpoint4 interrupt event disable
- **1** Endpoint4 interrupt event enable

EP5_TXE
- **0** Endpoint5 interrupt event disable
- **1** Endpoint5 interrupt event enable

USB+0008h Rx Interrupt Enable Register INTRRXE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													EP3_RXE	EP2_RXE	EP1_RXE	
Type													R/W	R/W	R/W	
Reset													1	1	1	

EP1_RXE
- **0** Rx Endpoint1 interrupt event disable
- **1** Rx Endpoint1 interrupt event enable

EP2_RXE
- **0** Rx Endpoint1 interrupt event disable
- **1** Rx Endpoint1 interrupt event enable

EP3_RXE

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0 Rx Endpoint1 interrupt event disable
1 Rx Endpoint1 interrupt event enable

USB+000Ah Common USB Interrupt Register INTRUSB

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									VBUSERROR	SESSREQ	DISCON	CONN	SOF	RESET/BABBLE	RESUME	SUSPEND
Type									R	R	R	R	R	R	R	R
Reset									0	0	0	0	0	0	0	0

SUSPEND Set when Suspend signaling is detected on the bus. Only valid in Peripheral mode.
RESUME Set when Resume signaling is detected on the bus while the USB2.0 controller is in Suspend mode.
RESET Set in Peripheral mode when Reset signaling is detected on the bus.
BABBLE Set in Host mode when babble is detected. Note: Only active after first SOF has been sent.
SOF Set when a new frame starts.
CONN Set when a device connection is detected. Only valid in Host mode. Valid at all transaction speeds.
DISCON Set in Host mode when a device disconnect is detected. Set in Peripheral mode when a session ends. Valid at all transaction speeds.
SESSREQ Set when Session Request signaling has been detected. Only valid when USB2.0 controller is 'A' device.
VBUSERROR Set when VBus drops below the VBus Valid threshold during a session. Only valid when USB2.0 controller is 'A' device.

USB+000Bh Common USB Interrupt Enable Register INTRUSBE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									VBUSERROR_E	SESSREQ_E	DISCON_E	CONN_E	SOF_E	RESET/BABBLE_E	RESUM_E	SUSPEND_E
Type									R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset									0	0	0	0	0	0	0	0

SUSPEND_E Suspend interrupt enable.
RESUME_E Resume interrupt enable
RESET/BABBLE_E Reset/Babble interrupt enable
SOF_E SOF interrupt enable
CONN_E Conn interrupt enable
DISCON_E Discon interrupt enable
SESSREQ_E SessReq interrupt enable
VBUSERROR_E VBusError interrupt enable

USB+000Ch Frame Number Register FRAME

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						FRAME NUMBER										
Type						R										
Reset						0										

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FRAME_NUMBER Frame is a 11-bit read-only register that holds the last received frame number.

USB+000Eh Endpoint Selection Index Register INDEX

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SELECTED ENDPOINT			
Type													R/W			
Reset													0			

SELECTED ENDPOINT Each Tx endpoint and each Rx endpoint have their own set of control/status registers located between USB+100h – USB+1FFh. In addition one set of Tx control/status and one set of Rx control/status registers appear at USB+010h – USB+01Fh. Index is a 4-bit register that determines which endpoint control/status registers are accessed. Before accessing an endpoint's control/status registers at USB+010h – USB+01Fh, the endpoint number should be written to the Index register to ensure that the correct control/status registers appear in the memory map.

USB+000Fh Test Mode Enable Register TESTMODE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FORCE_HOST	FIFO_ACCESS	FORCE_FS	FORCE_HS	TEST_PACKET	TEST_K	TEST_J	TEST_SE0_NAK
Type									R/W	SET	R/W	R/W	R/W	R/W	R/W	R/W
Reset									0	0	0	0	0	0	0	0

TEST_SE0_NAK (HIGH-SPEED MODE) The CPU sets this bit to enter the Test_SE0_NAK test mode. In this mode, the USB2.0 controller remains in High-speed mode but responds to any valid IN token with a NAK.

TEST_J (HIGH-SPEED MODE) The CPU sets this bit to enter the Test_J test mode. In this mode, the USB2.0 controller transmits a continuous J on the bus.

TEST_K (HIGH-SPEED MODE) The CPU sets this bit to enter the Test_K test mode. In this mode, the USB2.0 controller transmits a continuous K on the bus.

TEST_PACKET (HIGH-SPEED MODE) The CPU sets this bit to enter the Test_Packet test mode. In this mode, the USB2.0 controller repetitively transmits on the bus a 53-byte test packet, the form of which is defined in the Universal Serial Bus Specification Revision 2.0, Section 7.1.20. Note: The test packet has a fixed format and must be loaded into the Endpoint 0 FIFO before the test mode is entered.

FORCE_HS The CPU sets this bit either in conjunction with bit 7 above or to force the USB2.0 controller into High-speed mode when it receives a USB reset.

FORCE_FS The CPU sets this bit either in conjunction with bit 7 above or to force the USB2.0 controller into Fullspeed mode when it receives a USB reset.

FIFO_ACCESS The CPU sets this bit to transfer the packet in the Endpoint 0 Tx FIFO to the Endpoint 0 Rx FIFO. It is cleared automatically.

FORCE_HOST The CPU sets this bit to instruct the core to enter Host mode when the Session bit is set, regardless of whether it is connected to any peripheral. The state of the CID input, HostDisconnect and LineState signals are ignored. The core will then remain in Host mode until the Session bit is cleared, even if a device is disconnected, and if the Force_Host bit remains set, will re-enter Host mode the next time the Session bit is set.While in this mode, the status of the

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HOSTDISCON signal from the PHY may be read from bit 7 of the ACTLR0.DevCtl register.
The operating speed is determined from the Force_HS and Force_FS bits as follows:

Force_HS	Force_FS	Operating Speed
0	0	Low Speed
0	1	Full Speed
1	0	High Speed
1	1	*Undefined*

Peripheral Mode

USB+0100h EP0 Control Status Register CSR0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								FLUSHFIFO	SERVICESETUPEND	SERVICEDRXPKTRDY	SENDSTALL	SETUPEND	DATAEND	SENDSTALL	TXPKTRDY	RXPKTRDY
Type								SET	SET	SET	SET	R	SET	R/CLEAR	R/SET	R
Reset								0	0	0	0	0	0	0	0	0

RXPKTRDY This bit is set when a data packet has been received. An interrupt is generated when this bit is set. The CPU clears this bit by setting the ServicedRxPktRdy bit.
TXPKTRDY The CPU sets this bit after loading a data packet into the FIFO. It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled).
SENTSTALL This bit is set when a STALL handshake is transmitted. The CPU should clear this bit.
DATAEND The CPU sets this bit: When setting TxPktRdy for the last data packet. When clearing RxPktRdy after unloading the last data packet. When setting TxPktRdy for a zero length data packet.It is cleared automatically.
SETUPEND This bit will be set when a control transaction ends before the DataEnd bit has been set. An interrupt will be generated and the FIFO flushed at this time. The bit is cleared by the CPU writing a 1 to the ServicedSetupEnd bit.
SENDSTALL The CPU writes a 1 to this bit to terminate the current transaction. The STALL handshake will be transmitted and then this bit will be cleared automatically. Note: The FIFO should be flushed before SendStall is set.
SERVICERXPKTRDY The CPU writes a 1 to this bit to clear the RxPktRdy bit. It is cleared automatically.
SERVICESETUPEND The CPU writes a 1 to this bit to clear the SetupEnd bit. It is cleared automatically.
FLUSHFIFO The CPU writes a 1 to this bit to flush the next packet to be transmitted/read from the Endpoint 0 FIFO. It is cleared automatically. The FIFO pointer is reset and the TxPktRdy/RxPktRdy bit (below) is cleared. Note: FlushFIFO should only be used when TxPktRdy/RxPktRdy is set. At other times, it may cause data to be corrupted.

Host Mode

USB+0102h EP0 Control Status Register CSR0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DISPING			FLUSHFIFO	NAKTIMEOUT	STATUSPKT	REQPKT	ERROR	SETUPPKT	RXSTALL	TXPKTRDY	RXPKTRDY

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Type					R/W			SET	R/CLEAR	R/W	R/W	R/CLEAR	R/CLEAR	R/CLEAR	R/SET	R/CLEAR
Reset					0			0	0	0	0	0	0	0	0	0

RXPKTRDY This bit is set when a data packet has been received. An interrupt is generated (if enabled) when this bit is set. The CPU should clear this bit when the packet has been read from the FIFO.
TXPKTRDY The CPU sets this bit after loading a data packet into the FIFO. It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled).
RXSTALL This bit is set when a STALL handshake is received. The CPU should clear this bit.
SETUPPKT The CPU sets this bit, at the same time as the TxPktRdy bit is set, to send a SETUP token instead of an OUT token for the transaction. Note: Setting this bit also clears the DataToggle.
ERROR This bit will be set when three attempts have been made to perform a transaction with no response from the peripheral. The CPU should clear this bit. An interrupt is generated when this bit is set.
REQPKT The CPU sets this bit to request an IN transaction. It is cleared when RxPktRdy is set.
STATUSPKT The CPU sets this bit at the same time as the TxPktRdy or ReqPkt bit is set, to perform a status stage transaction. Setting this bit ensures that the data toggle is set to 1 so that a DATA1 packet is used for the Status Stage transaction.
NAKTIMEOUT This bit will be set when Endpoint 0 is halted following the receipt of NAK responses for longer than the time set by the NAKLimit0 register. The CPU should clear this bit to allow the endpoint to continue.
FLUSHFIFO The CPU writes a 1 to this bit to flush the next packet to be transmitted/read from the Endpoint 0 FIFO. The FIFO pointer is reset and the TxPktRdy/RxPktRdy bit (below) is cleared. Note: FlushFIFO should only be used when TxPktRdy/RxPktRdy is set. At other times, it may cause data to be corrupted.
DISPING The CPU writes a 1 to this bit to instruct the core not to issue PING tokens in data and status phases of a high-speed Control transfer (for use with devices that do not respond to PING)

USB+0108h EP0 Received bytes Register COUNT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										EP0 RX COUNT						
Type										R						
Reset										0						

EP0 RX COUNT0 Count0 is a 7-bit read-only register that indicates the number of received data bytes in the Endpoint 0 FIFO. The value returned changes as the contents of the FIFO change and is only valid while RxPktRdy (IDXEPR0.CSR0.bit0) is set.

Host Mode

USB+010Bh NAK Limit Register NAKLIMT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												NAKLIMIT0				
Type												R/W				
Reset												0				

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NAKLIMIT0 NAKLimit0 is a 5-bit register that sets the number of frames/microframes (High-Speed transfers) after which Endpoint 0 should timeout on receiving a stream of NAK responses. (Equivalent settings for other endpoints can be made through their TxInterval and RxInterval registers.). The number of frames/microframes selected is $2^{(m-1)}$ (where m is the value set in the register, valid values 2 – 16). If the host receives NAK responses from the target for more frames than the number represented by the Limit set in this register, the endpoint will be halted. Note: A value of 0 or 1 disables the NAK timeout function.

USB+010Fh Core Configuration Register CONFIGDATA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MPRXE	MPTXE	BIGENDIAN	HBRXE	HBTXE	DYNFIFOSIZING	SOFTCONE	UTMIDATAWIDTH
Type									R	R	R	R	R	R	R	R
Reset									0	0	0	0	0	0	0	0

UTMIDATAWIDTH Indicates selected UTMI+ data width.

- **0** 8 bits
- **1** 16 bits

SOFTCONE When set to '1' indicates Soft Connect/Disconnect option selected.
DYNFIFOSIZEING When set to '1' indicates Dynamic FIFO Sizing option selected.
HBTXE When set to '1' indicates High-bandwidth Tx ISO Endpoint Support selected.
HBRXE When set to '1' indicates High-bandwidth Rx ISO Endpoint Support selected
BIGENDIAN When set to '1' indicates Big Endian ordering is selected.
MPTXE When set to '1', automatic splitting of bulk packets is selected.
MPRXE When set to '1', automatic amalgamation of bulk packets is selected.

USB+0110h TXMAP Register TXMAP

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	M-1					MAXIMUM PAYLOAD TRANSACTION										
Type	R/W					R/W										
Reset	0					0										

TXMAXP M-1 Maxmum payload size for indexed TX endpoint

M-1 Packet multiplier m

TXMAXP MAXIMUM PAYLOD TRANSACTION REGISTER

The TxMaxP register defines the maximum amount of data that can be transferred through the selected Tx endpoint in asingle operation. There is a TxMaxP register for each Tx endpoint (except Endpoint 0).Bits 10:0 define (in bytes) the maximum payload transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints

placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Fullspeed and High speed operations. Where the option of High-bandwidth Isochronous/Interrupt endpoints or of packet splitting on Bulk endpoints

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has been taken when the core is configured, the register includes either 2 or 5 further bits that define a multiplier m which is equal to one more than the value recorded.

In the case of Bulk endpoints with the packet splitting option enabled, the multiplier m can be up to 32 and defines the maximum number of 'USB' packets (i.e. packets for transmission over the USB) of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. (If the packet splitting option is not enabled, bit15–13 is not implemented and bit12–11(if included) is ignored.) Note: The data packet is required to be an exact multiple of the payload specified by bits 10:0, which is itself required to be either 8, 16, 32, 64 or (in the case of High Speed transfers) 512 bytes.

For Isochronous/Interrupt endpoints operating in High-Speed mode and with the High-bandwidth option enabled, m may only be either 2 or 3 (corresponding to bit 11 set or bit 12 set, respectively) and it specifies the maximum number of such transactions that can take place in a single microframe. If either bit 11 or bit 12 is non-zero, the USB2.0 controller will automatically split any data packet written to the FIFO into up to 2 or 3 'USB' packets, each containing the specified payload (or less). The maximum payload for each transaction is 1024 bytes, so this allows up to 3072 bytes to be transmitted in each microframe. (For Isochronous/Interrupt transfers in Full-speed mod, bits 11 and 12 are ignored.)

The value written to bits 10:0 (multiplied by m in the case of high-bandwidth Isochronous/Interrupt transfers) must match the value given in the wMaxPacketSize field of the Standard Endpoint Descriptor for the associated endpoint (see USB Specification Revision 2.0, Chapter 9). A mismatch could cause unexpected results.The total amount of data represented by the value written to this register (specified payload × m) must not exceed the FIFO size for the Tx endpoint, and should not exceed half the FIFO size if double-buffering is required.If this register is changed after packets have been sent from the endpoint, the Tx endpoint FIFO should be completely flushed (using the FlushFIFO bit in TxCSR) after writing the new value to this register.

Peripheral Mode

USB+0112h Tx CSR Register TXCSR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOSET	ISO	MODE	DMAREQEN	FRCDATATOG	DMAREQMODE	AUTOSETENSPKT		INCOMPTX	CLRDATATOG	SENTSTALL	SENDSTALL	FLUSHFIFO	UNDERRUN	FIFONOTEMPTY	TXPKTRDY
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

TXPKTRDY The CPU sets this bit after loading a data packet into the FIFO. It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled). TxPktRdy is also automatically cleared (but no interrupt is generated) prior to loading a second packet into a double-buffered FIFO.

FIFONOTEMPTY The USB sets this bit when there is at least 1 packet in the TxFIFO.

UNDERRUN The USB sets this bit if an IN token is received when the TxPktRdy bit not set. The CPU should clear this bit (write 0 clear).

FLUSHFIFO The CPU writes a 1 to this bit to flush the latest packet from the endpoint TxFIFO. The FIFO pointer is reset, the TxPktRdy bit is cleared and an interrupt is generated. May be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. Note: FlushFIFO should only be used when TxPktRdy is set. At other times, it may cause data to be corrupted. Also note that, if the FIFO is double-buffered, FlushFIFO may need to be set twice to ompletely

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clear the FIFO.

SENDSTALL The CPU writes a 1 to this bit to issue a STALL handshake to an IN token. The CPU clears this bit to terminate the stall condition. Note: This bit has no effect where the endpoint is being used for Isochronous transfer.

SENTSTALL This bit is set when a STALL handshake is transmitted. The FIFO is flushed and the TxPktRdy bit is cleared. The CPU should clear this bit.

CLRDATATOG The CPU writes a 1 to this bit to reset the endpoint data toggle to 0.

INCOMPTX When the endpoint is being used for high-bandwidth Isochronous/Interrupt transfers, this bit is set to indicate where a large packet has been split into 2 or 3 packets for transmission but insufficient IN tokens have been received to send all the parts. Note: In anything other than a high-bandwidth transfer, this bit will always return 0.

AUTOSETEN_SPKT If the CPU sets this bit, TxPktRdy will be automatically set when the short packet is loaded into the TxFIFO completely. But, this function only works in Tx endpoint 1 and 2. Besides, Tx endpoint 1 has to use DMA channel 1 to move data and Tx endpoint 2 has to use DMA channel 2 to move data.

DMAREQMODE The CPU sets this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0.Note: This bit must not be cleared either before or in the same cycle as the DMAReqEn bit is cleared.

FRCDATATOG The CPU sets this bit to force the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received. This can be used by Interrupt Tx endpoints that are used to communicate rate feedback for Isochronous endpoints.

DMAREQEN The CPU sets this bit to enable the DMA request for the Tx endpoint.

MODE The CPU sets this bit to enable the endpoint direction as Tx, and clears the bit to enable it as Rx. Note: This bit only has any effect where the same endpoint FIFO is used for both Tx and Rx transactions.

ISO The CPU sets this bit to enable the Tx endpoint for Isochronous transfers, and clears it to enable the Tx endpoint for Bulk or Interrupt transfers. Note: This bit only has any effect in Peripheral mode. In Host mode, it always returns zero.

AUTOSET If the CPU sets this bit, TxPktRdy will be automatically set when data of the maximum packet size (value in TxMaxP) is loaded into the TxFIFO. If a packet of less than the maximum packet size is loaded, then TxPktRdy will have to be set manually if AutoSetEn_SPKT is not enabled.

Host Mode

USB+0112h Tx CSR Register TXCSR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOSET		MODE	DMAREQEN	FRCDATATOG	DMAREQMODE			NAKTIMEOUT/INCOMPTX	CLRDATATOG	RXSTALL		FLUSHFIFO	ERROR	FIFONOTEMPTY	TXPKTRDY
Type	R/W		R/W	R/W	R/W	R/W			R/W	R/W	R/W		R/W	R/W	R/W	R/W
Reset	0		0	0	0	0			0	0	0		0	0	0	0

TXPKTRDY The CPU sets this bit after loading a data packet into the FIFO. It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled). TxPktRdy is also automatically cleared prior to loading a second packet into a double-buffered FIFO.

FIFONOTEMPTY The USB sets this bit when there is at least 1 packet in the Tx FIFO.

ERROR The USB sets this bit when 3 attempts have been made to send a packet and no handshake packet has been

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received. When the bit is set, an interrupt is generated, TxPktRdy is cleared and the FIFO is completely flushed. The CPU should clear this bit. Valid only when the endpoint is operating in Bulk or Interrupt mode.

FLUSHFIFO The CPU writes a 1 to this bit to flush the latest packet from the endpoint Tx FIFO. The FIFO pointer isreset, the TxPktRdy bit (below) is cleared and an interrupt is generated. May be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. Note: FlushFIFO should only be used when TxPktRdy is set. At other times, it may cause data to be corrupted. Also note that, if the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.

RXSTALL This bit is set when a STALL handshake is received. When this bit is set, any DMA request that is in progress is stopped, the FIFO is completely flushed and the TxPktRdy bit is cleared (see below). The CPU should clear this bit.

CLRDATATOG The CPU writes a 1 to this bit to reset the endpoint data toggle to 0.

NAKTIMEOUT Bulk endpoints only: This bit will be set when the Tx endpoint is halted following the receipt of NAK responses for longer than the time set as the NAK Limit by the TxInterval register. The CPU should clear this bit to allow the endpoint to continue.

INCOMPTX High-bandwidth Interrupt endpoints only: This bit will be set if no response is received from the device to which the packet is being sent.

DMAREQMODE The CPU sets this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0.Note: This bit must not be cleared either before or in the same cycle as the above DMAReqEnab bit is cleared.

FRCDATATOG The CPU sets this bit to force the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received. This can be used by Interrupt Tx endpoints that are used to communicate rate feedback for Isochronous endpoints.

DMAREQENAB The CPU sets this bit to enable the DMA request for the Tx endpoint.

MODE The CPU sets this bit to enable the endpoint direction as Tx, and clears it to enable the endpoint direction as Rx. Note: This bit only has any effect where the same endpoint FIFO is used for both Tx and Rx transactions.

AUTOSET If the CPU sets this bit, TxPktRdy will be automatically set when a packet of the maximum packet size (TxMaxP) is loaded into the Tx FIFO. If a packet of less than the maximum packet size is loaded, then TxPktRdy will have to be set manually. Note: Should not be set for either high-bandwidth Isochronous endpoints or high-bandwidth Interrupt endpoints.

USB+0114h RXMAP Register RXMAP

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	M-1					MAXIMUM PAYLOAD TRANSACTION										
Type	R/W					R/W										
Reset	0					0										

M-1 Maxmum payload size for indexed RX endpoint , M-1 Packet multiplier m

MAXIMUM PAYLOAD TRANSACTION REGISTER The RxMaxP register defines the maximum amount of data that can be transferred through the selected Rx endpoint in a single operation. There is a RxMaxP register for each Rx endpoint (except Endpoint 0).Bits 10:0 define (in bytes) the maximum payload transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-speed and High-speed operations.

Where the option of High-bandwidth Isochronous/Interrupt endpoints or of combining Bulk packets has been taken when

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the core is configured, the register includes either 2 or 5 further bits that define a multiplier m which is equal to one more than the value recorded.
For Bulk endpoints with the packet combining option enabled, the multiplier m can be up to 32 and defines the number of USB packets of the specified payload which are to be combined into a single data packet within the FIFO. (If the packet splitting option is not enabled, bit15–bit13 is not implemented and bit12–bit11 (if included) is ignored.)
For Isochronous/Interrupt endpoints operating in High-Speed mode and with the High-bandwidth option enabled, m may only be either 2 or 3 (corresponding to bit 11 set or bit 12 set, respectively) and it specifies the maximum number of such transactions that can take place in a single microframe. If either bit 11 or bit 12 is non-zero, the USB2.0 controller will automatically combine the separate USB packets received in any microframe into a single packet within the Rx FIFO. The maximum payload for each transaction is 1024 bytes, so this allows up to 3072 bytes to be received in each microframe. (For Isochronous/Interrupt transfers in Full-speed mode or if High-bandwidth is not enabled, bits 11 and 12 are ignored.)
The value written to bits 10:0 (multiplied by m in the case of high-bandwidth Isochronous/Interrupt transfers) must match the value given in the wMaxPacketSize field of the Standard Endpoint Descriptor for the associated endpoint (see USB Specification Revision 2.0, Chapter 9). A mismatch could cause unexpected results.
The total amount of data represented by the value written to this register (specified payload × m) must not exceed the FIFO size for the OUT endpoint, and should not exceed half the FIFO size if double-buffering is required.

Peripheral Mode

USB+0116h RX CSR Register RXCSR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOCLEAR	ISO	DMAREQEN	DISNYET/PIDERR	DMAREQMODE	AUTOCLRENSPKT	INCOMPRXINTREN	INCOMPRX	CLRDTATOG	SENTSTALL	SENDSTALL	FLUSHFIFO	DATAERR	OVERRUN	FIFOFULL	RXPKTRDY
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RXPKTRDY This bit is set when a data packet has been received (to RxFIFO). The CPU should clear this bit when the packet has been unloaded from the RxFIFO. An interrupt is generated when the bit is set.
FIFOFULL This bit is set when no more packets can be loaded into the RxFIFO.
OVERRUN This bit is set if an OUT packet cannot be loaded into the RxFIFO. The CPU should clear this bit (write 0 clear). Note: This bit is only valid when the endpoint is operating in ISO mode. In Bulk Mode, it always returns zero. The new incoming packet won't be written to RxFIFO. An interrupt is generated when the bit is set and OverRunIntrEn is set.
DATAERROR This bit is set when RxPktRdy is set if the data packet has a CRC or bit-stuff error. The CPU should write 0 to clear this bit. Note: This bit is only valid when the endpoint is operating in ISO mode. In Bulk Mode, it always returns zero. An interrupt is generated when the bit is set and DataErrIntrEn is set.
FLUSHFIFO The CPU writes a 1 to this bit to flush the next packet to be read from the endpoint RxFIFO. The RxFIFO pointer is reset and the RxPktRdy bit is cleared. Note: FlushFIFO should only be used when RxPktRdy is set. At other times, it may cause data to be corrupted. Also note that, if the RxFIFO is double buffered, FlushFIFO may need to be set twice to completely clear the RxFIFO.
SENDSTALL The CPU writes a 1 to this bit to issue a STALL handshake. The CPU clears this bit to terminate the stall condition. Note: This bit has no effect where the endpoint is being used for ISO transfers.

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SENTSTALL This bit is set when a STALL handshake is transmitted. The CPU should clear this bit. An interrupt is generated when the bit is set.

CLRDATATOG The CPU writes a 1 to this bit to reset the endpoint data toggle to 0.

INCOMPRX This bit is set in a high-bandwidth Isochronous/Interrupt transfer if the packet in the RxFIFO is incomplete because parts of the data were not received. It is cleared when RxPktRdy is cleared or write 0 to clear. Note: In anything other than a high-bandwidth transfer, this bit will always return 0. An interrupt is generated when the bit is set and IncompRxIntrEn is set.

INCOMPRXINTREN IncompRx and PidErr interrupt enable.

AUTOCLREN_SPKT The CPU write a 1 to this bit to enable short packets' RxPktRdy to be automatically cleared. Whe this bit is turned on, AutoClear must also be turned on. If ISO and AutoClrEn_SPKT are both set, when short packets are unloaded, RxPktRdy will be cleared automatically. But, these short packets must have no IncompRx, PidErr, DataErr or OverRun status.

DMAREQMODE The CPU sets this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0. DMA Request Mode 1: Rx endpoint interrupt is generated only when DMA Request Mode 1 and received a short packet. RxDMAReq is generated when receiving a Max-Packet-size packet.DMA Request Mode 0: No Rx endpoint interrupt. RxDMAReq is generated when RxPktRdy is set.

DISNYET(BULK/INTERRUPT TRANSACTIONS) The CPU sets this bit to disable the sending of NYET handshakes. When set, all successfully received Rx packets are ACK'd including at the point at which the RxFIFO becomes full. Note: This bit only has any effect in High-speed mode, in which mode it should be set for all interrupt endpoint.

PIDERR(ISO TRANSACTIONS) This bit is set when there is a PID error in the received packet. It is cleared when RxPktRdy is cleared or write 0 to clear. An interrupt is generated when the bit is set and IncompRxIntrEn is set.

DMAREQEN The CPU sets this bit to enable the DMA request for the Rx endpoint.

ISO The CPU sets this bit to enable the Rx endpoint for Isochronous transfers, and clears it to enable the Rx endpoint for Bulk/Interrupt transfers.

AUTOCLEAR If the CPU sets this bit then the RxPktRdy bit will be automatically cleared when a packet of RxMaxP bytes has been unloaded from the RxFIFO. When packets of less than the maximum packet size are unloaded, RxPktRdy will have to be cleared manually if AutoClrEn_SPKT is not enabled.

Host Mode

USB+0116h Rx CSR Register RXCSR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOCLEAR	AUTOREQ	DMAREQENAB	PIDERROR	DMAREQMODE			INCOMPRX	CLRDATATOG	RXSTALL	REQPKT	FLUSHFIFO	DATAERR/NAKTIMER	ERROR	FIFOFULL	RXPKTRDY
Type	R/W	R/W	R/W	R	R/W			R/CLEAR	R/W	R/CLEAR	R/W	SET	R/CLEAR	R/CLEAR	R	R/CLEAR
Reset	0	0	0	0	0			0	0	0	0	0	0	0	0	0

RXPKTRDY This bit is set when a data packet has been received. The CPU should clear this bit when the packet has been unloaded from the Rx FIFO. An interrupt is generated when the bit is set.

FIFOFULL This bit is set when no more packets can be loaded into the Rx FIFO.

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ERROR The USB sets this bit when 3 attempts have been made to receive a packet and no data packet has been received. The CPU should clear this bit. An interrupt is generated when the bit is set. Note: This bit is only valid when the Rx endpoint is operating in Bulk or Interrupt mode. In ISO mode, it always returns zero.

NAKTIMEOUT In Bulk mode, this bit will be set when the Rx endpoint is halted following the receipt of NAK responses for longer than the time set as the NAK Limit by the RxInterval register.

DATAERROR When operating in ISO mode, this bit is set when RxPktRdy is set if the data packet has a CRC or bit-stuff error and cleared when RxPktRdy is cleared.

FLUSHFIFO The CPU writes a 1 to this bit to flush the next packet to be read from the endpoint Rx FIFO. The FIFO pointer is reset and the RxPktRdy bit (below) is cleared. Note: FlushFIFO should only be used when RxPktRdy is set. At other times, it may cause data to be corrupted. Also note that, if the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.

REQPKT The CPU writes a 1 to this bit to request an IN transaction. It is cleared when RxPktRdy is set.

RXSTALL When a STALL handshake is received, this bit is set and an interrupt is generated. The CPU should clear this bit.

CLRDATATOG The CPU writes a 1 to this bit to reset the endpoint data toggle to 0.

INCOMPRX This bit will be set in a high-bandwidth Isochronous/Interrupt transfer if the packet received is incomplete. It will be cleared when RxPktRdy is cleared. Note: If USB protocols are followed correctly, this bit should never be set. The bit becoming set indicates a failure of the associated Peripheral device to behave correctly. (In anything other than a high-bandwidth transfer, this bit will always return 0.)

DMAREQMODE The CPU sets this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0.Note: This bit should not be cleared in the same cycle as RxPktRdy is cleared

PIDERROR ISO Transactions Only: The core sets this bit to indicate a PID error in the received packet. Bulk/Interrupt Transactions: The setting of this bit is ignored.

DMAREQENAB The CPU sets this bit to enable the DMA request for the Rx endpoint.

AUTOREQ If the CPU sets this bit, the ReqPkt bit will be automatically set when the RxPktRdy bit is cleared. Note: This bit is automatically cleared when a short packet is received.

AUTOCLR f the CPU sets this bit then the RxPktRdy bit will be automatically cleared when a packet of RxMaxP bytes has been unloaded from the Rx FIFO. When packets of less than the maximum packet size are unloaded, RxPktRdy will have to be cleared manually. Note: Should not be set for highbandwidth Isochronous endpoints.

USB+0118h Rx Count Register RXCOUNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RXCOUNT													
Type			R													
Reset			0													

RXCOUNT It is a 14-bit read-only register that holds the number of received data bytes in the packet in the RxFIFO. Note: The value returned changes as the FIFO is unloaded and is only valid while RxPktRdy(RxCSR.D0) is set.

Host Mode

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USB+011Ah TxType Register TXTYPE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TX PROTOCOL		TX TARGET EP NUMBER			
Type											R/W		R/W			
Reset											0		0			

TX TARGET EP NUMBER (HOST MODE ONLY) The CPU should set this value to the endpoint number contained in the Tx endpoint descriptor returned to the USB2.0 Controller during device enumeration.

TX PROTOCOL (HOST MODE ONLY) The CPU should set this to select the required protocol for the Tx endpoint:

- **00** Illegal
- **01** Isochronous
- **10** Bulk
- **11** Interrupt

USB+011Bh TxInterval Register TXINTERVAL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TX POLLING INTERVAL/NAK LIMIT M							
Type									R/W							
Reset									0							

TxInterval Register TxInterval is an 8-bit register that, for Interrupt and Isochronous transfers, defines the polling interval for the currently-selected Tx endpoint. For Bulk endpoints, this register sets the number of frames/microframes after which the endpoint should timeout on receiving a stream of NAK responses. There is a TxInterval register for each configured Tx endpoint (except Endpoint 0).

TX POLLING INTERVAL / NAK LIMIT (M), (HOST MODE ONLY)
In each case the value that is set defines a number of frames/microframes (High Speed transfers), as follows:

Transfer Type	Speed	Valid values (*m*)	Interpretation
Interrupt	Low Speed or Full Speed	1 – 255	Polling interval is *m* frames.
	High Speed	1 – 16	Polling interval is $2^{(m-1)}$ microframes
Isochronous	Full Speed or High Speed	1 – 16	Polling interval is $2^{(m-1)}$ frames/microframes
Bulk	Full Speed or High Speed	2 – 16	NAK Limit is $2^{(m-1)}$ frames/microframes. *Note:* A value of 0 or 1 disables the NAK timeout function.

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USB+011Ch RxType Register RXTYPE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RX PROTOCOL		RX TARGET EP NUMBER			
Type											R/W		R/W			
Reset											0		0			

RX TARGET EP NUMBER (HOST MODE ONLY) The CPU should set this value to the endpoint number contained in the Tx endpoint descriptor returned to the USB2.0 Controller during device enumeration.

RX PROTOCOL (HOST MODE ONLY) The CPU should set this to select the required protocol for the Tx endpoint:

- **00** Illegal
- **01** Isochronous
- **10** Bulk
- **11** Interrupt

USB+011Dh RxInterval Register RXINTERVAL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX POLLING INTERVAL/NAK LIMIT M							
Type									R/W							
Reset									0							

RxInterval Register RxInterval is an 8-bit register that, for Interrupt and Isochronous transfers, defines the polling interval for the currently-selected Rx endpoint. For Bulk endpoints, this register sets the number of frames/microframes after which the endpoint should timeout on receiving a stream of NAK responses. There is a RxInterval register for each configured Rx endpoint (except Endpoint 0).

RX POLLING INTERVAL / NAK LIMIT (M), (HOST MODE ONLY)
In each case the value that is set defines a number of frames/microframes (High Speed transfers), as follows:

Transfer Type	Speed	Valid values (*m*)	Interpretation
Interrupt	Low Speed or Full Speed	1 – 255	Polling interval is *m* frames.
	High Speed	1 – 16	Polling interval is $2^{(m-1)}$ microframes
Isochronous	Full Speed or High Speed	1 – 16	Polling interval is $2^{(m-1)}$ frames/microframes
Bulk	Full Speed or High Speed	2 – 16	NAK Limit is $2^{(m-1)}$ frames/microframes. *Note:* A value of 0 or 1 disables the NAK timeout function.

Peripheral Mode

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USB+011Fh Configured FIFO Size Register FIFOSIZE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RXFIFOSIZE				TXFIFOSIZE			
Type									R				R			
Reset									0				0			

TXFIFOSIZE Indicate the TxFIFO size of 2n bytes, (ex: value 10 means 210 = 1024 bytes.)

RXFIFOSIZE Indicate the RxFIFO size of 2n bytes, (ex: value 10 means 210 = 1024 bytes.)

USB+0120h ~ USB+012Fh stands for Endpoint 2 Registers and their behaviors are the same as Endpoint 1.
USB+0130h ~ USB+013Fh stands for Endpoint 3 Registers and their behaviors are the same as Endpoint 1.
USB+0140h ~ USB+014Fh stands for Endpoint 4 Registers and their behaviors are the same as Endpoint 1.

USB+0020h USB Endpoint 0 FIFO Register FIFO0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO DATA[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO DATA[15:0]															
Type	R/W															
Reset	0															

USB+0024h USB Endpoint 1 FIFO Register FIFO1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO DATA[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO DATA[15:0]															
Type	R/W															
Reset	0															

USB+0028h USB Endpoint 2 FIFO Register FIFO2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO DATA[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO DATA[15:0]															
Type	R/W															
Reset	0															

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USB+002Ch USB Endpoint 3 FIFO Register FIFO3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO DATA[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO DATA[15:0]															
Type	R/W															
Reset	0															

FIFOData 32-bits FIFO data access window

The Endpoint FIFO Registers provides 6 addresses for CPU access to the FIFOs for each endpoint. Writing to these addresses loads data into the TxFIFO for the corresponding endpoint. Reading from these addresses unloads data from the RxFIFO for the corresponding endpoint.

Note: (i) Transfers to and from FIFOs may be 8-bit, 16-bit or 32-bit as required, and any combination of access is allowed provided the data accessed is contiguous. However, all the transfers associated with one packet must be of the ame width so that the data is consistently byte-, word- or double-word-aligned. The last transfer may however contain fewer bytes than the previous transfers in order to complete an odd-byte or odd-word transfer.

(ii) Depending on the size of the FIFO and the expected maximum packet size, the FIFOs support either single-packet or double-packet buffering. However, burst writing of multiple packets is not supported as flags need to be set after each packet is written.

(iii) Following a STALL response or a Tx Strike Out error on Endpoint 0 – 4, the associated FIFO is completely flushed

USB+0061h Power Up Counter Register PWRUPCNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													PWRUPCNT			
Type													R/W			
Reset													4'hf			

PWRUPCNT[3:0] Power Up Counter Limit. Power Up Counter is used to count the K state duration during suspend and when it is timeout, the resume interrupt will be issued. The register should be configured according to AHB clock speed.

USB+0062h Tx FIFO Size Register TXFIFOSZ

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TXDPB	TXSZ			
Type												R/W	R/W			
Reset												0	0			

TXDPB Defines whether double-packet buffering supported for TxFIFO. When '1', double-packet buffering is supported. When '0', only single-packet buffering is supported.

TXSZ Maximum packet size to be allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission). If TxDPB = 0, the FIFO will also be this size; if TxDPB = 1, the FIFO will be twice this size

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TxSZ[3:0]				Packet Size (Bytes)
0	0	0	0	8
0	0	0	1	16
0	0	1	0	32
0	0	1	1	64
0	1	0	0	128
0	1	0	1	256
0	1	1	0	512
0	1	1	1	1024
1	0	0	0	2048 (Single-packet buffering only)
1	0	0	1	4096 (Single-packet buffering only)
1	1	1	1	3072 (Single-packet buffering only)

USB+0063h Rx FIFO Size Register RXFIFOSZ

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RXDPB	RXSZ			
Type												R/W	R/W			
Reset												0	0			

RXDPB Defines whether double-packet buffering supported for TxFIFO. When '1', double-packet buffering is supported. When '0', only single-packet buffering is supported.

RXSZ Maximum packet size to be allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission). If TxDPB = 0, the FIFO will also be this size; if TxDPB = 1, the FIFO will be twice this size

RxSZ[3:0]				Packet Size (Bytes)
0	0	0	0	8
0	0	0	1	16
0	0	1	0	32
0	0	1	1	64
0	1	0	0	128
0	1	0	1	256
0	1	1	0	512
0	1	1	1	1024
1	0	0	0	2048 (Single-packet buffering only)

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RxSZ[3:0]				Packet Size (Bytes)
1	0	0	1	4096 (Single-packet buffering only)
1	1	1	1	3072 (Single-packet buffering only)

USB+0064h Tx FIFO Address Register TXFIFOADD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			TXFIFOADD													
Type			R/W													
Reset			0													

TXFIFOADD TxFIFOadd is a 13-bit register which controls the start address of the selected Rx endpoint FIFO.

TxFIFOadd[12:0]				Start Address
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
		...		...
1	F	F	F	FFF8

USB+0066h Rx FIFO Address Register RXFIFOADD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATAERRINTRE	OVERRUNITREN		RXFIFOADD												
Type	R/W	R/W		R/W												
Reset	0	0		0												

RXFIFOADD RxFIFOadd is a 13-bit register which controls the start address of the selected Rx endpoint FIFO.

RxFIFOadd[12:0]				Start Address
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
		...		...
1	F	F	F	FFF8

OVERRUNINTREN OverRun interrupt enable. The OverRun status bit is in RxCSR[2] and it should be write 0 to clear.

DATAERRINTREN DataErr interrupt enable. The DataErr status bit is in RxCSR[3] and it should be write 0 to clear.

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USB+006Ch Version Register HWVERS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RC	XX					YYY									
Type	R	R					R									
Reset	0	0					0									

RC Set to '1' if RTL used from a Release Candidate rather than from a full release of the core.

XX Major Version Number (Range 0 – 31).

YYY Minor Version Number (Range 0 – 999).
HWVers register is a 16-bit read-only register that returns information about the version of the RTL from which the core hardware was generated, in particular the RTL version number (vxx.yyy).

USB+0070h Software Reset Register SWRST

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			OPSTATE									REDUCEDLY	UNDOSRPFIX	FRCVBUSVALID	SWRST	DISUSBRESET
Type			RO									R/W	R/W	R/W	R/W	R/W
Reset			0									0	0	0	0	0

DISUSBRESET The CPU sets this bit to Disable USBReset function. And, then the CPU can reset the hardware bySwRst. USBReset will be asserted when doing High Speed Detection Handshake. (This bit will only be reset when hardware reset.)
SWRST The CPU sets this bit to reset the endpoint and RAM interface hardware.
FRC_VBUSVALID The CPU sets this bit to force VBusVal = 1, VBusSess = 1 and VBusLo = 0.
UNDO_SRPFIX The CPU sets this bit to recover to the original circuit of USB2.0 IP about SRP.
REDUCEDLY The CPU can set this bit to reduce inter-pkt delay.
OPSTATE This register indicates the USB controller state information.

USB+0078h Info. about number of Tx and Rx Register EPINFO

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RXENDPOINTS				TXENDPOINTS			
Type									R				R			
Reset									0				0			

TXENDPOINTS The number of Tx endpoints implemented in the design.

RXENDPOINTS The number of Rx endpoints implemented in the design.
This 8-bit read-only register allows read-back of the number of Tx and Rx endpoints included in the design.

USB+0079h Info. about the width of RAM and the number of DMA channel Register RAMINFO

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name									DMACHANS				RAMBITS			
Type									R				R			
Reset									0				0			

RAMBITS The width of the RAM address bus – 1.

DMA CHANNELS The number of DMA channels implemented in the design.
This 8-bit read-only register provides information about the width of the RAM and the number of DMA channels.

USB+007Ah Info. about delay to be applied Register LINKINFO

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									WTCON				WTID			
Type									R/W				R/W			
Reset									4'h5				4'hc			

WTID Sets the delay to be applied from IDPULLUP being asserted to IDDIG being considered valid in units of 4.369ms. (The default setting corresponds to 52.43ms.)
WTCON Sets the wait to be applied to allow for the user's connect/disconnect filter in units of 533.3ns. (The default setting corresponds to 2.667µs.) This 8-bit register allows some delays to be specified.

USB+007Bh Vbus Pulsing Charge Register VPLEN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									VPLEN							
Type									R/W							
Reset									8'h3C							

VPLEN Sets the duration of the VBus pulsing charge in units of 136.5 us. (The default setting corresponds to 8.19ms)
This 8-bit register sets the duration of the VBus pulsing charge.

USB+007Ch Time buffer available on HS transaction Register HS_EOF1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									HS_EOF1							
Type									R/W							
Reset									8'h80							

HS_EOF1 Sets for High-speed transactions the time before EOF to stop beginning new transactions, in units of 133.3ns. (The default setting corresponds to 17.07µs.)

USB+007Dh Time buffer available on FS transaction Register FS_EOF1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FS_EOF1							
Type									R/W							
Reset									8'h77							

FS_EOF1 Sets for Full-speed transactions the time before EOF to stop beginning new transactions, in units of 533.3ns. (The default setting corresponds to 63.46µs.)

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USB+007Eh Time buffer available on LS transaction Register LS_EOF1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LS_EOF1							
Type									R/W							
Reset									8'h72							

LS_EOF1 Sets for Low-speed transactions the time before EOF to stop beginning new transactions, in units of 1.067μs. (The default setting corresponds to 121.6μs.).

USB+007Fh Reset Information Register RSTINFO

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									WTFSSE0				WTCHRP			
Type									R/W				R/W			
Reset									0				0			

WTCHRP Sets the delay to be applied from detecting Reset to sending chirp K (for Device only). The duration = 272.8 x WTChrp + 0.1 usec. (This register will only be reset when hardware reset.)

WTFSSE0 The field signifies the SE0 signal duration before issue the reset signal(for Device only). The duration = 272.8 x WTFSSE0 + 2.5 usec. (This register will only be reset when hardware reset.)

USB+0300h EP1 RxPktCount Register EP1RXPKTCOUNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EP1RXPKTCOUNT															
Type	R/W															
Reset	0															

EP1RQPKTCOUNT (HOST MODE ONLY) Sets the number of packets of Rx Endpoint 1 size MaxP that are to be transferred in a block transfer. Only used in Host mode when AutoReq is set. Has no effect in Peripheral mode or when AutoReq is not set.

USB+0302h EP2 RxPktCount Register EP2RXPKTCOUNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EP2RXPKTCOUNT															
Type	R/W															
Reset	0															

EP2RQPKTCOUNT (HOST MODE ONLY) Sets the number of packets of Rx Endpoint 2 size MaxP that are to be transferred in a block transfer. Only used in Host mode when AutoReq is set. Has no effect in Peripheral mode or when AutoReq is not set.

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USB+0304h EP3 RxPktCount Register EP3RXPKTCOUNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EP3RXPKTCOUNT															
Type	R/W															
Reset	0															

EP3RQPKTCOUNT (HOST MODE ONLY) Sets the number of packets of Rx Endpoint 3 size MaxP that are to be transferred in a block transfer. Only used in Host mode when AutoReq is set. Has no effect in Peripheral mode or when AutoReq is not set.

USB+0308h EP4 RxPktCount Register EP4RXPKTCOUNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EP4RXPKTCOUNT															
Type	R/W															
Reset	0															

EP4RQPKTCOUNT (HOST MODE ONLY) Sets the number of packets of Rx Endpoint 3 size MaxP that are to be transferred in a block transfer. Only used in Host mode when AutoReq is set. Has no effect in Peripheral mode or when AutoReq is not set.

RqPktCount (Host Mode Only) For each Rx Endpoint 1 – 8, the USB2.0 controller provides a 16-bit RqPktCount register. This read/write register is used in Host mode to specify the number of packets that are to be transferred in a block transfer of one or more Bulk packets of length MaxP to Rx Endpoint n. The core uses the value recorded in this register to etermine the number of requests to issue where the AutoReq option (included in the RxCSR register) has been set.Note: Multiple packets combined into a single bulk packet within the FIFO count as one packet.

USB+0200h DMA Interrupt Status Register DMA_INTR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													PPB_FINISH2	PPA_FINISH2	PPB_FINISH1	PPA_FINISH1
Type													R/W	R/W	R/W	R/W
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_LIMITER												DMA_INTR			
Type	R												R/W			
Reset	0												0			

DMA_INTR Indicates pending DMA interrupts, one bit per DMA channel implemented. Bit 0 is used for DMA channel 1, Bit 1 is used for DMA channel 2 etc. Write 0 clear.

PPA_FINISH1 Indicates dma channel 1 PingPongA finish status. Write 0 clear.

PPB_FINISH1 Indicates dma channel 1 PingPongB finish status. Write 0 clear.

PPA_FINISH2 Indicates dma channel 2 PingPongA finish status. Write 0 clear.

PPB_FINISH2 Indicates dma channel 2 PingPongB finish status. Write 0 clear.

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DMA_LIMITER Please refer to USB+210 register .The DMA_LIMITER can be read in this address,too.

USB+0204h DMA Channel 1 Control Register DMA_CNTL1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ENDMAMODE2	PP_RST	PP_EN	BURSTMODE		BUSERR	ENDPNT				INTEN	DMAMODE	DMADIR	DMAEN
Type			R/W	R/W	R/W	R/W		R/W	R/W				R/W	R/W	R/W	R/W
Reset			0	0	0	0		0	0				0	0	0	0

DMA_EN Enable DMA. The bit will be cleared when the DMA transfer is completed.
DMA_DIR Direction. 0 : DMA Write(Rx endpoint), 1 : DMA Read(Tx endpoint).
DMA_MODE DMA Mode.
INT_EN Interrupt Enable.
EndPnt[3 :0] Endpoint number.
BUS_ERR Bus Error.
BURST_MODE Burst Mode.

- **00** Burst Mode 0 : Bursts of unspecified length.
- **01** Burst Mode 1 : INCR4 or unspecified length
- **10** Burst Mode 2 : INCR8, INCR4 or unspecified length.
- **11** Burst Mode 3 : INCR16, INCR8, INCR4 or unspecified length

PP_EN PingPong Buffer Enable.
PP_RST The CPU writes 1 to this bit to reset PingPong Buffer Sequence. The bit stands for current PingPong Buffer Sequence when read.
ENDMAMODE2 Enable DMA mode 2 function. DMA mode 2: The short packets will be moved by DMA even the short packets are not the last transfer of this DMA Count. The DMA mode 2 function can't be turned on when AutoReq = 1
DMA_CNTL2, DMA_CNTL3, DMA_CNTL4, DMA_CNTL5 and DMA_CNTL6 have the same modification.

USB+0208h DMA Channel 1 ADDRESS Register DMA_ADDR1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_ADDR1[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_ADDR1[15:0]															
Type	R/W															
Reset	0															

DMA_ADDR1 32bits DMA start address, updated (increase) by USB2.0 controller automatically while multiple packet DMA (DMA Mode = 1) is used
DMA_ADDR2, DMA_ADDR3, DMA_ADDR4, DMA_ADDR5 and DMA_ADDR6 have the same modification.

USB+020Ch DMA Channel1 BYTE COUNT Register DMA_COUNT1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA COUNT1[31:16]															

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Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_COUNT1[15:0]															
Type	R/W															
Reset	0															

DMA_COUNT1 32bits DMA transfer count with byte unit, updated (decrease) by USB2.0 controller automatically while each packet is transferred. DMA_COUNT 2, DMA_COUNT3, DMA_COUNT4, DMA_COUNT5 and DMA_COUNT6 have the same modification.

USB+0214h ~ USB+021ch stands for DMA Channel 2 Registers and their behaviors are the same as DMA channel 1.

USB+0210h DMA Channel Limiter Register DMA_LIMITER

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_LIMITER															
Type	R/W															
Reset	0															

DMA_LIMITER This register is to suppress the Bus utilization of the DMA channel. The value is from 0 to 255. 0 means no limitation, and 255 means totally banned. The value between 0 and 255 means certain DMA can have permission to use AHB every (4 X n) AHB clock cycles.Note that it is not recommended to limit the Bus utilization of the DMA channels because this increases the latency of response to the masters, and the transfer rate decreases as well. Before using it, programmer must make sure that the bus masters have some protective mechanism to avoid entering the wrong states.

USB+0284h DMA Channel PingPong Control Register DMA_PP_CNTL1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DMAEN
Type																R/W
Reset																0

DMA_EN Enable DMA(PingPong Buffer DMA). The bit will be cleared when the DMA transfer is completed.

USB+0288h DMA Channel 1 PingPong Address Register DMA_PP_ADDR1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_PP_ADDR1[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_PP_ADDR1[15:0]															
Type	R/W															

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Reset	0

DMA_PP_ADDR1[31:0] DMA(PingPong Buffer DMA) Channel 1 AHB Memory Address.

USB+028Ch DMA Channel 1 PingPong Count Register DMA_PP_CNT1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_PP_CNT1[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_PP_CNT1[15:0]															
Type	R/W															
Reset	0															

DMA_PP_CNT1[31:0] DMA(PingPong Buffer DMA) Channel 1 Byte Count.

USB+0294h ~ USB+029Ch stands for DMA Channel 2 PingPong Registers and their behaviors are the same as DMA channel 1.

USB+0400h DMA Channel Real Count Register DMA_REALCNT1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA REALCNT[31:16]															
Type	R															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA REALCNT[15:0]															
Type	R															
Reset	0															

DMA_REALCNT[31:0] Indicate current transferred bytes of DMA channel 1.

USB+0404h DMA Channel 1 PingPong Real Count Register DMA_PP_REALCNT1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA PP REALCNT[31:16]															
Type	R															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA PP REALCNT[15:0]															
Type	R															
Reset	0															

DMA_PP_REALCNT[31:0] Indicate current transferred bytes of DMA channel 1 PingPong.

USB+0408h DMA Channel 1 Timer Register DMA_TIMER1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name								TIMEOUTSTATUS	ENTIMER	REG TIMEOUT
Type								R/W	R/W	R/W
Reset								0	0	0

ENTIMER Enable timer. When the timer is enabled and there is no this DMA transaction during the reg_timeout duration, then DMA interrupt will be issued. The timer will be reset whenever EnTimer = 0 or (DMA_EN = 0 and DAM_EN_PP = 0).

REG_TIMEOUT To config timeout duration. Timeout duration = 1280 * reg_timeout + 2.5 us.

TIMEOUT_STATUS Indicates the DMA channel has timeout situation. Write 0 clear.

USB+0410h ~ USB+0418h stands for DMA Channel 2 Registers and their behaviors are the same as DMA channel 1.

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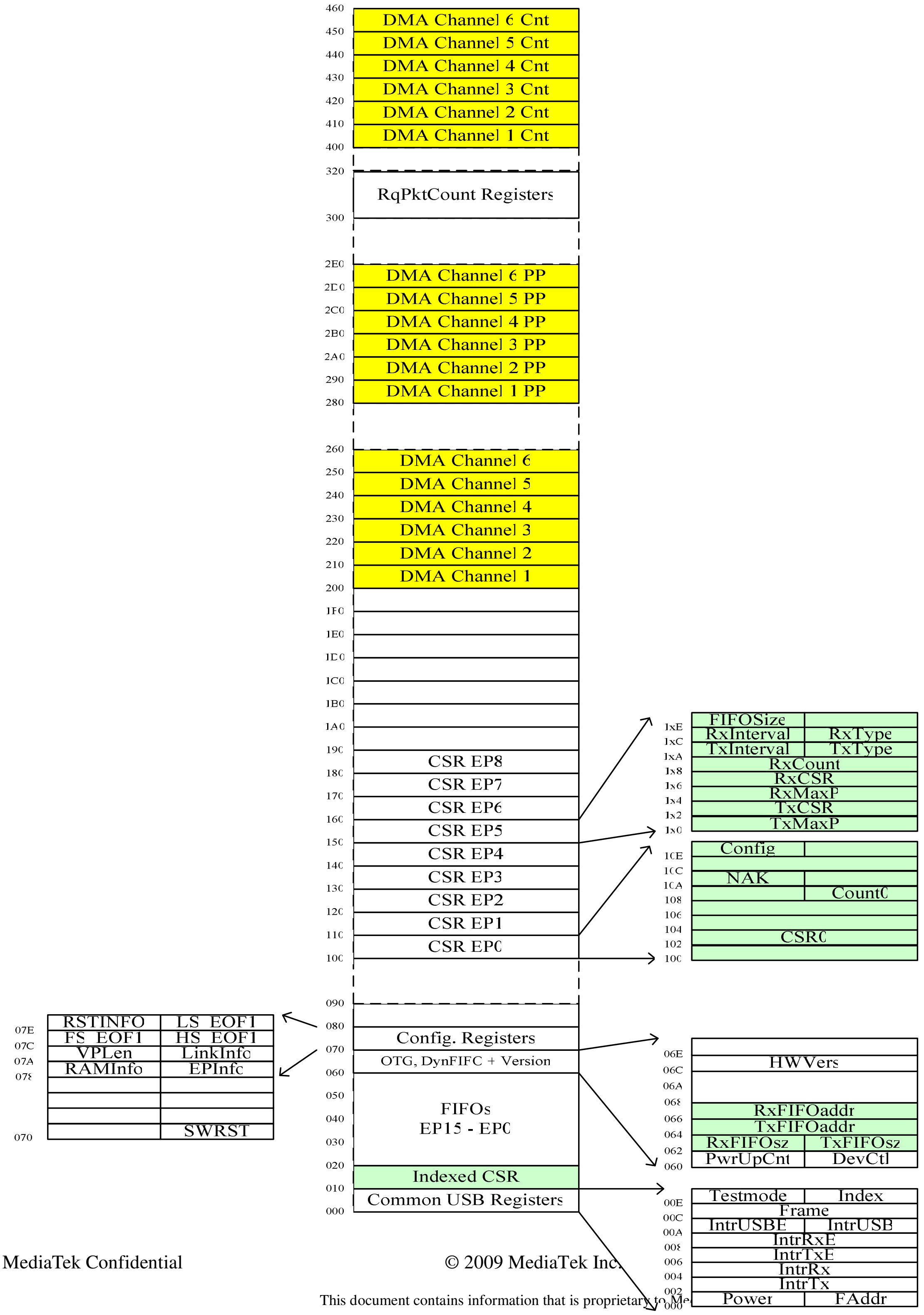

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Figure 72 USB Control Register Mapping

USB+0600h PHY Control Register 1 PHYCR1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HS_TX_IEN_MODE	HS_TX_SPSEL	HS_SQ_INIT_EN_DG[1:0]		HS_SQ_ENDG	HS_SQ_EN_MODE	HS_SQS	HS_RCV_EN_MODE	HS_ RCVB[3:0]				PLL_VCOG[1:0]		PLL_VCOB[1:0]	
Type	R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W				R/W		R/W	
Reset	1	0	2'b01		1	1	0	1	4'b0100				2'b01		0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PLL_CCP[3:0]						PLL_CLF	EN_LS_CMPSAT	PLL_EN		NEG_TRI_EN_B	USB20_TX_TST	BIDI_MODE	CDR_TST[1:0]		GATE_EN_B
Type	R/W						R/W	R/W	R/W		R/W	R/W	R/W	R/W		R/W
Reset	4'b0110						0	0	0		0	0	0	0		0

GATED_EN_B High level clock gating enable

- **0** enable
- **1** disable

CDR_TST CDR function option ，CDR_TST[1]: phase accumulation option，

- **0** accumulation disable
- **1** accumulation

enable CDR_TST[0]: reference phase number option，0: 4 phases，1: 6 phases

BIDI_MODE UTMI data bus bi-directional mode

- **0** enable
- **1** disable

USB20_TX_TST TX macro test option, debug usage，

- **0** enable
- **1** disable

NEG_TRI_EN_B UTMI output signal aligned to negative edge for hold time issue

- **0** negative edge triggered output
- **1** positive edge triggered output

PLL_EN USB2.0 PHY PLL enable，

- **0** enable
- **1** disable

EN_LS_CMPSAT LS Tx mode DM RPU compensation enable when in client mode，

- **0** disable
- **1** enable

PLL_CLF PLL loop filter control，

- **0** disable
- **1** enable

PLL_CPP PLL CP bias current selection，charge pump current = 3.125uA * n，0001 : 3.125uA * 1，0010 : 3.125uA *

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2…1111 : 3.125uA * 15 PLL_CCP should be set to 0x03 for better performance.

PLL_VCOB PLL VCO bias current selection，

- **00** 0uA
- **01** 25uA * 1.5
- **10** 25uA * 2.5
- **11** 25uA * 3.5

PLL_VCOG[0] PLL VCO gain selection ，

- **0** normal Kvco gain.
- **1** decrease Kvco gain

PLL_VCOG[1] This bit is used to gated internal clock source.

HS_RCVB HS RCV bias selection, HS RCV 1st stage bias current，

- **xxx0** 600u
- **xxx1** 675u

HS_RCV_EN_MODE HS RCV enable mode selection，

- **0** HS RCV enable by HS RCV
- **1** HS RCV always enabled

while USB operating in HS mode

HS_SQS HS SQ hystress mode Reserved

HS_SQ_EN_MODE HS SQ enable mode selection，

- **0** SQ enable by HS RCV
- **1** SQ always enabled while USB operating

HS_SQ_EN_DG HS SQ de-glitch time after HS RCV enabled，

- **0** SQ output de-glitch 4T 480M CLK
- **1** SQ output de-glitch 5T 480M CLK

HS_SQ_INIT_EN_DG HS SQ first time initializing de-glitch:gated by

- **00** 1T ref CLK
- **01** 1.5T ref CLK
- **10** 2T ref CLK
- **11** 2.5T ref CLK

HS_TX_SP_SEL HS TX LOAD sampling point selection，

- **0** sampling the HS TX data at rising edge
- **1** sampling the HS TX data at falling edge

HS_TX_I_EN_MODE HS TX I enable mode selection，

- **0** HS TX current always enabled while HS TERM enabled
- **1** HS_TX current enabled when HS TX module enabled

USB+0604h PHY Control Register 2 PHYCR2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	FORCE_DRV_VBUS	FORCE_DM_PULLDOWN	FROCE_DP_PULLDOWN	HS_TERMC[4:0]					FIX_SONYBUG	FROCE_DATA_IN	FROCE_TX VALID	HS_TERM_SEL	HS_DISCTH[1:0]		HS_DISCB[1:0]	
Type	R/W	R/W	R/W	R/W						R/W	R/W	R/W	R/W		R/W	
Reset	0	0	0	5'b01000						0	0	0	0		0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		HS_SQTL[2:0]				HS_SQTH[2:0]			HS_SQD[3:0]				HS_SQB[3:0]			
Type		R/W				R/W			R/W				R/W			
Reset		3'b011				3'b100			4'b0010				4'b0010			

HS_SQB HS SQ bias selection，HS_SQB[0]: HS SQ 1st stage bias current，

xxx0 600uA
xxx1 675uA

HS_SQD HS SQ de-glitch control

xx00 16u (min current, max de-glitch)
xx01 32u
xx10 61u
xx11 122u (max current de-glitch)

HS_SQTH HS SQ threshold high selection

000 165mV
001 155mV
010 145mV
011 135mV
100 125mV
110 105mV
111 95mV

HS_SQTL HS SQ threshold low selection，Reserved

HS_DISCB HS_DISCP[0] : see HS_DISCN[1:0] ，HS_DISCP[1]: disconnect 1st stage bias current，

0 420uA
1 490uA

HS_DISCTH HS DISC threshold selection

000 615mV
001 605mV
010 595mV
011 585mV
100 575mV
101 565mV

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110 555mV
111 545mV

HS_TERM_SEL HS TERM module selection (see HS_TERMC)，0: analog termination，1: digital termination

FORCE_TAVALID It is used to force PHY input signal TXVALID to a specific value. 1: enable. 0: disable.

FORCE_TAVALIDH It is used to force PHY input signal TXVALIDH to a specific value. 1: enable. 0: disable.

FORCE_DATAIN It is used to force PHY input signal DATAIN to a specific value. 1: enable. 0: disable.

FIX_SONYBUG When this bit is set , then TXFIFO write pointer will be reset when FlushFIFO. When this bit is not set, then TxFIFO write pointer won't be reset when FlushFIFO.

HS_TERMC HS TERM impedence control code (see HS_TERM_SEL)，In analog termination mode HS_TERM_SEL: 0 internal reference voltage:

x0000 480mV
x0001 470mV
x0010 460mV
x0011 450mV
x0100 440mV
x0101 430mV
x0110 420mV
x0111 410mV
x1000 400mV
x1001 390mV
x1010 380mV
x1011 370mV

the final output swing is about (the termnation voltage + 400mv)/2.
In digital termination mode HS_TERM_SEL: 1

00000 for max swing
...
11111 for min swing

FORCE_DP_PULLDOWN It is used to force PHY input signal DP_PULLDOWN to a specific value.

0 disable
1 enable

FORCE_DM_PULLDOWN It is used to force PHY input signal DM_PULLDOWN to a specific value.

0 disable
1 enable.

FORCE_DRV_VBUS It is used to force PHY input signal DRVVBUS to a specific value.

0 disable
1 enable

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USB+0608h PHY Control Register 3 PHYCR3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		AIOI_SEL[2:0]			GHX_SEL[3:0]				CLKMODE[0]	XTAL_BIAS[2:0]			TEST_CTRL[3:0]			
Type		R/W			R/W				R/W	R/W			R/W			
Reset		0			0				0	0			0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			PLL_DR[5:0]						FEN_HS_TX_I	FEN_FS_LS_RCV	FEN_FS_LS_TX	IREF_MODE_SEL	FEN_HS_RCV	IADJ[2:0]		
Type			R/W						R/W	R/W	R/W	R/W	R/W	R/W		
Reset			6'b001010						0	0	0	0	0	3'b100		

IADJ HS TX bias current selection

- **000** 840mV(Rext + 300)
- **001** 830mV(Rext + 300)
- **010** 820mV(Rext + 300)
- **011** 810mV(Rext + 300)
- **100** 800mV(Rext + 300)
- **101** 790mV(Rext + 300)
- **110** 780mV(Rext + 300)
- **111** 770mV(Rext + 300)

Rext = 5.1k (typ.)

FEN_HS_RCV Forced HS RCV and Squelch enable for test purpose

- **0** disable
- **1** enable

IREF_MODE_SEL HS SQ reference current mode selection ，0: HS SQ current always enabled while USB operating ，1: HS SQ current enabled while HS RX module enabled

FEN_FS_LS_TX Forced FS/LS output enable for test purpose

- **0** disable
- **1** enable

FEN_FS_LS_RCV Forced FS/LS RCV enable for test purpose，

- **0** disable
- **1** enable

FEN_HS_TX_I Forced HS TX current source enable for test purpose，

- **0** disable
- **1** enable

PLL_DR PLL div ratio 480/reference CLK=PLL_DR ex: 30MHz xtal case, PLL_DR = 480/30 = 16 = 0x10

TEST_CTRL Test mode control TEST_CTRL[3]:0: normal UTMI operation

1: 240MHz clock ouput, with while TEST_CTRL[0]=1 and FEN_HS_TX_I=11

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TEST_CTRL[3]:

- **0** normal UTMI operation
- **1** 240Mhz clock output ,with while TEST_CTRL[0]=1 and FEN_HS_TX_I=11

TEST_CTRL[2]:

- **0** no tx early
- **1** tx_early

TEST_CTRL[1]:

- **0** turn off 100K ohm register pull up DM signal
- 1 turn on 100K ohm register pull up DM signal

TEST_CTRL[0]:

- **0** normal UTMI operation
- **1** TX controlled by FEN_HS_TX_I/FEN_FS_LS_TX

XTAL_BIAS XTAL bias selection Reserved

CLKMODE External/Internal input CLK source selection

- **x00** internal clk source USB_INTA1_CK
- **x01** internal clk source USB_INTA2_CK
- **x10** internal clk source USB_INTD_CK

GHX_SEL GHX Digital output selection

- **xx00** none
- **xx01** HS DISC output for USB 2.0 RXDC test(set DOUT1_SEL)
- **xx10** HS SQ output for USB 2.0 RXDC test(set DOUT1_SEL)
- **xx11** HS RX output for USB 2.0 RXDC test(set DOUT1_SEL)

AIO1_SEL Analog IO1 selection for test (IO via XTALI pin)

- **0xxx** disable AIO1
- **100** external bgr input
- **101** monitor internal bgr voltage
- **110** monitor internal pll loop filter voltage
- **111** monitor internal hs termination control voltage

AIO ouput only valid for XTALI_GPIO_EN=1 & XTALI_GPIO_OE=0

USB+060Ch PHY Control Register 4 PHYCR4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CLKMODE[1]	HS_DISCTH[2]		TX_FLUSH_EN	XTALI_GPIO_OE	XTALO_GPIO_ES	XTALO_GPIO_EN	XTALI_GPIO_I	XTALI_GPIO_OE	XTALI_GPIO_ES	XTALI_GPIO_EN	XTALI_GPIO_I
Type					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BGR_DIV[1:0]			BGR_SELPH	BGR_CHIP_EN	BGR_ISRC_EN	BGR_CLK_EN	BGR_BGR_EN		DOUT2_SEL[2:0]				DOUT1_SEL[2:0]		
Type	R/W			R/W	R/W	R/W	R/W	R/W		R/W				R/W		
Reset	2'b01			0	1	0	0	0		3'b100				3'b100		

DOUT1_SEL Digital output 1 selection for test (output via VRT pin)

- **000** normal function
- **001** bgr ph1
- **010** bgr ph1s
- **011** bgr pheq
- **100** USB 2.0 RX DC test (see GHX_SEL)
- **101** USB 1.1 RXM
- **110** USB 1.1 RXP
- **111** USB 1.1 RXD

DOUT1 ouput only valid for XTALI_GPIO_EN=1 & XTALI_GPIO_OE=1

DOUT2_SEL Digital output 2 selection for test (output via VRT pin)

- **000** normal function
- **x01** bgr ph2
- **x10** bgr ph2s_
- **x11** bgr pho_

DOUT2 ouput only valid for XTALO_GPIO_EN=1 & XTALO_GPIO_OE=1

BGR_BGR_EN Force BGR enable 0: disable 1: enableBGRCLKEN

BGR_CLK_EN Force BGR chop clock enable 0: disable 1: enable

BGR_ISRC_EN Force BGR current source generator enable 0: disable 1: enable

BGR_CHP_EN BGR chop enable 0: disable 1: enable

BGR_DIV BGR chop clk rate

- **00** 836k
- **11** 836k/2
- **10** 836k/4
- **11** 836k/8

XTALI_GPIO_I It's used to control GPIO output data when XTALI pin GPIO function is enabled.
XTALI_GPIO_EN Enable XTALI pin GPIO function.
XTALI_GPIO_ES It's used to control GPIO output driving strength when XTALI pin GPIO function is enabled.
XTALI_GPIO_OE It's used to enable GPIO output function when XTALI pin GPIO function is enabled.
XTALO_GPIO_I It's used to control GPIO output data when XTALO pin GPIO function is enabled.

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XTALO_GPIO_EN Enable XTALO pin GPIO function.
XTALO_GPIO_ES It's used to control GPIO output driving strength when XTALO pin GPIO function is enabled.
XTALO_GPIO_OE It's used to enable GPIO output function when XTALI pin GPIO function is enabled.
TX_FLUSH_EN When this bit is set , then TxFIFO write pointer will be reset when FlushFIFO. When this bit is not set, then TxFIFO write pointer won't be reset when FlushFIFO.

USB+0610h PHY Control Register 5 PHYCR5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DM_PULL_DOWN	DP_PULL_DOWN	XCVR_SELECT[1:0]		SUSPNDM	TERM_SELECT	OP_MODE[1:0]		FROCE_IDPULLUP	UTMIMUXSEL	USB_MODE[1:0]		FROCE_XVER_SELECT	FROCE_SUSPENDM	FROCE_TERM_SELECT	FORCE_OP_MODE
Type	R/W	R/W	R/W		R/W	R/W	R/W		R/W	R/W	R/W		R/W	R/W	R/W	R/W
Reset	0	0	0		0	0	0		0	0	0		0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PROBE_SEL[7:0]								VBUS_CMP_EN	CLK_DIV_CNT[2:0]			CDR_FILT[3:0]			
Type	R/W								R/W	R/W			R/W			
Reset	0								1	0			4'b0010			

CDR_FILT CDR low pass filter selection, debug usage
CLK_DIVC_CNT The divide ratio of div_ck
PROBE_SEL Debug signal selection
FORCE_OPMODE It is used to force PHY input signal OPMODE to a specific value. 1: enable. 0: disable.
FORCE_TERM_SELECT It is used to force PHY input signal TERM_SELECT to a specific value. 1: enable. 0: disable.
FORCE_SUSPENDM It is used to force PHY input signal SUSPENDM to a specific value. 1: enable. 0: disable.
FORCE_XCVR_SELECT It is used to force PHY input signal XCVR_SELECT to a specific value. 1: enable. 0: disable.
USB_MODE Test mode selection (for testing)

00 normal operation
01 loop-back mode1 enable, the pseudo random number will be generated inside USB2.0 PHY macro and transmit onto USB bus. The data will be received by receiver and then be compared. The compared result is muxed on line_state[1] and should be always be 1.
10 loop-back mode2 enable, the packet is longer.

UTMI_MUXSEL It is used to force all PHY UTMI input signals to specific values
0 disable
1 enable
.
FORCE_IDPULLUP It is used to force PHY input signal IDPULLUP to a specific value.
0 disable
1 enable

OPMODE It is used to control PHY input signal OPMODE when force_opmode = 1 or utmi_muxsel = 1.
TERMSEL It is used to control PHY input signal TERMSEL when force_termsel = 1 or utmi_muxsel = 1.

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SUSPENDM It is used to control PHY input signal SUSPENDM when force_suspendm = 1 or utmi_muxsel = 1.

XCVRSEL It is used to control PHY input signal XCVRSEL when force_xcvrsel = 1 or utmi_muxsel = 1.

DPPULLDOWN It is used to control PHY input signal DPPULLDOWN when force_dppulldown = 1 or utmi_muxsel = 1.

DMPULLDOWN It is used to control PHY input signal DMPULLDOWN when force_dmpulldown = 1 or utmi_muxsel = 1.

USB+0614h PHY UTMI Interface Register 1 PHYIR1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LINESTATE[1:0]		HOSTDISC_ON	TXREADY	RXERROR	RXACTIVE	RXVALIDH	RXVALID	XDATA_OUT[15:8]							
Type	R		R	R	R	R	R	R	R							
Reset	0		0	0	0	0	0	0	0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XDATA_OUT[7:0]								XDATA_IN[3:0]				TX_VALIDH	TX_VALID	DRVVBUS	IDPULLUP
Type	R								R/W				R/W	R/W	R/W	R/W
Reset	0								0				0	0	0	0

IDPULLUP It is used to control PHY input signal IDPULLUP when force_idpullup = 1 or utmi_muxsel = 1.

DRVVBUS It is used to control PHY input signal DRVVBUS when force_drvvbus = 1 or utmi_muxsel = 1.

TX_VALID It is used to control PHY input signal TX_VALID when force_txvalid = 1 or utmi_muxsel = 1.

TX_VALIDH It is used to control PHY input signal TX_VALIDH when force_txvalidh = 1 or utmi_muxsel = 1.

XDATA_IN It is used to control PHY input signal XDATA_IN when force_datain = 1 or utmi_muxsel = 1.

XDATA_OUT It is used to control PHY input signal IDPULLUP when force_idpullup = 1 or utmi_muxsel = 1.

RXVALID It indicates the PHY output signal RXVALID status.

RXVALIDH It indicates the PHY output signal RXVALIDH status.

RXACTIVE It indicates the PHY output signal RXACTIVE status.

RXERROR It indicates the PHY output signal RXERROR status.

TXREADY It indicates the PHY output signal TXREADY status.

HOSTDISCON It indicates the PHY output signal HOSTDISCON status.

LINE_STATE It indicates the PHY output signal LINE_STATE status.

USB+0618h PHY UTMI Interface Register 2 PHYIR2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	FORCE_AUX_EN	FORCE_OTG_PROBE	FORCE_USB_CLKON	FORCE_BVALID	FORCE_IDDIG	FORCE_VBUSVALID	FORCE_SESSEND	FORCE_AVALID	USB_RESERVED[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W							
Reset	0	0	0	0	0	0	0	0	0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	USB_RESERVED[7:0]												IDDIG	VBUSVALID	SESSEND	AVALID
Type	R/W												R	R	R	R
Reset	0												0	0	0	0

FORCE_AVALID It is used to force PHY input signal AVALID to a specific value. 1: enable. 0: disable.
FORCE_SESSEND It is used to force PHY input signal SESSEND to a specific value. 1: enable. 0: disable.
FORCE_VBUSVALID It is used to force PHY input signal VBUSVALID to a specific value. 1: enable. 0: disable.
FORCE_IDDIG It is used to force PHY input signal IDIG to a specific value. 1: enable. 0: disable.
FORCE_BVALID It is used to force PHY input signal BVALID to a specific value. 1: enable. 0: disable.
FORCE_USB_CLKON It is used to force PHY input signal USB_CLKOFF to a specific value. 1: enable. 0: disable.
FORCE_OTG_PROBE It is used to force PHY input signal OTG_PROBE to a specific value. 1: enable. 0: disable.
FORCE_AUX_EN It is used to force PHY input signal AUX_EN to a specific value. 1: enable. 0: disable.
AVALID It indicates the OTG AVALID Comparator result.
- **0** avalid< 0.8v
- **1** avalid > 2v

SESSEND It indicates the OTG SESSEND Comparator result.
- **0** sessend< 0.2v
- **1** sessend > 0.8v

VBUSVALID It indicates the OTG VBUS Comparator result.
- **0** Vbus< 4.4v
- **1** Vbus > 4.75v

IDDIG It indicates the ID pin comparator result when IDPULLUP = 1.
- **0** A-plug is plugged in.
- **1** B-plug is plugged in

USB+061Ch PHY UTMI Interface Register 3 PHYIR3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AUX_EN	OTG_PROBE	USB_CLKON	BVALID_W	IDDIG_W	VBUSVALID_W	SESSEND_W	AVALID_W
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1

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AVALID_W It is used to control PHY input signal avalid when force_avalid = 1 or utmi_muxsel = 1
SESSEND_W It is used to control PHY input signal sessend when force_sessend = 1 or utmi_muxsel = 1.
VBUSVALID_W It is used to control PHY input signal vbusvalid when force_vbusvalid = 1 or utmi_muxsel = 1.
IDDIG_W It is used to control PHY input signal iddig when force_iddig = 1 or utmi_muxsel = 1.
BVALID_W It is used to control PHY input signal bvalid when force_bvalid = 1 or utmi_muxsel = 1.
USB_CLKON USB PHY input 48Mhz clock source signal enable 0: disable 1: enable

OTG_PROBE OTG debug signal enable 0: disable 1: enable

AUX_EN UART USB share pad function enable 0: disable 1: enable

6.4.3 Power on/off USB PHY and Controller Sequence

1 Power on sequence after plug-in.

1.1 Turn on Vusb(PHY 3.3v power) – the control register is in PMIC document.

1.2 Turn on USB AHB clock(52MHz) – the control register is in config document.

1.3 Turn on internal 48MHz PLL – the control register is in clock document.

1.4 Wait 50 usec. (PHY 3.3v power stable time)

1.5 It should set force_aux_en= 0 and force_usb_clkon = 1 to enable 48MHz PLL and switch to USB function. → reg[USB+061Bh] = 0x20.

1.6 Turn on Bandgap → reg[USB+060Dh] bit0 = 1. (bgr_bgr_en).

1.7 Wait 10 usec.

1.8 Release force suspendm. → reg[USB+0612h] bit2 = 0. (force_suspendm)

1.9 Wait 20 usec.

1.10 pll_en = 1. → reg[USB+0600h] bit7 = 1.

2 Power off sequence after plug-out.

2.1 Force suspendm = 0. → reg[USB+0613h] bit3 = 0.(suspendm) and reg[USB+0612h] bit2 = 1.(force_suspendm)

2.2 Wait 6 * 33.33ns

2.3 Pll_en = 0. → reg[USB+0600h] bit7 = 0

2.4 Turn off Bandgap → reg[USB+060Dh] bit0 = 0. (bgr_bgr_en).

2.5 Turn off Vusb(PHY 3.3v power) – the control register is in PMIC document

3 Suspend sequence after get suspend interrupt

3.1 Wait 6 * 33.33ns

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3.2 Pll_en = 0. → reg[USB+0600h] bit7 = 0

3.3 It should set force_aux_en= 0 and force_usb_clkon = 1 to enable 48MHz PLL and switch to USB function. → reg[USB+061Bh] = 0x20.

3.4 Turn off internal 48Mhz PLL if there is no other hardware module is using the 48Mhz clock -the control register is in clock document

4 Resume sequence after get resume interrupt

4.1 Turn on internal 48MHz PLL – the control register is in clock document.

4.2 Turn on pll_vcog[1] = 1 to disable gated 48MHz PLL. → reg[USB+0602h] bit3 = 1.

4.3 It should set force_aux_en= 0 and force_usb_clkon = 1 to enable 48MHz PLL and switch to USB function. → reg[USB+061Bh] = 0x20.

4.4 Wait 20 usec.

4.5 pll_en = 1. → reg[USB+0600h] bit7 = 1.

5 Initialzation Sequence

5.1 PLL_CCP[3:0]=0x3; (for better jitter performance).

5.2 TEST_CTRL[2] = 1; (for better jitter performance. Turn on tx earrlier).

6.5 Memory Stick and SD Memory Card Controller

6.5.1 Introduction

The controller fully supports the Memory Stick bus protocol as defined in Format Specification version 2.0 of Memory Stick Standard (Memory Stick PRO) and the SD Memory Card bus protocol as defined in SD Memory Card Specification Part 1 Physical Layer Specification version 2.0 as well as the MultiMediaCard (MMC) bus protocol as defined in MMC system specification version 4.1. Since SD Memory Card bus protocol is backward compatible to MMC bus protocol, the controller is capable of working well as the host on MMC bus under control of proper firmware. Furthermore, the controller also support SDIO card specification version 1.0 partially. However, the controller can only be configured as either the host of Memory Stick or the host of SD/MMC Memory Card at one time. Hereafter, the controller is also abbreviated as MS/SD controller. The following are the main features of the controller.

- Interface with MCU by APB bus
- 16/32-bit access on APB bus
- 16/32-bit access for control registers
- 32-bit access for FIFO

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- Shared pins for Memory Stick and SD/MMC Memory Card
- Built-in 32 bytes FIFO buffers for transmit and receive, FIFO is shared for transmit and receive
- Built-in CRC circuit
- CRC generation can be disabled
- DMA supported
- Interrupt capabilities
- Automatic command execution capability when an interrupt from Memory Stick
- Data rate up to 26 Mbps in serial mode, 26x4 Mbps (26x8 Mbps if 8-bit data line for SD/MMC card is configured) in parallel model, the module is targeted at 26 MHz operating clock
- Serial clock rate on MS/SD/MMC bus is programmable
- Card detection capabilities during sleep mode
- Controllability of power for memory card
- Not support SPI mode for MS/SD/MMC Memory Card
- Not support multiple SD Memory Cards

6.5.2 Overview

6.5.2.1 Pin Assignment

Since the controller can only be configured as either the host of Memory Stick or the host of SD/MMC Memory Card at one time, pins for Memory Stick and SD/MMC Memory Card are shared in order to save pin counts. The following lists pins required for Memory Stick and SD/MMC Memory Card. **Table 60** shows how they are shared. In **Table 60**, all I/O pads have embedded both pull up and pull down resistor because they are shared by both the Memory Stick and SD/MMC Memory Card. Pins 2,4,5,8 are only useful for SD/MMC Memory Card. Pull down resistor for these pins can be used for power saving. All embedded pull-up and pull-down resistors can be disabled by programming the corresponding control registers if optimal pull-up or pull-down resistors are required on the system board. The pin VDDPD is used for power saving. Power for Memory Stick or SD/MMC Memory Card can be shut down by programming the corresponding control register. The pin WP (Write Protection) is only valid when the controller is configured for SD/MMC Memory Card. It is used to detect the status of Write Protection Switch on SD/MMC Memory Card.

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No.	Name	Type	MMC	SD	MS	MSPRO	Description
1	SD_CLK	O	CLK	CLK	SCLK	SCLK	Clock
2	SD_DAT3	I/O/PP		CD/DAT3		DAT3	Data Line [Bit 3]
3	SD_DAT0	I/O/PP	DAT0	DAT0	SDIO	DAT0	Data Line [Bit 0]
4	SD_DAT1	I/O/PP		DAT1		DAT1	Data Line [Bit 1]
5	SD_DAT2	I/O/PP		DAT2		DAT2	Data Line [Bit 2]
6	SD_CMD	I/O/PP	CMD	CMD	BS	BS	Command Or Bus State
7	SD_PWRON	O					VDD ON/OFF
8	SD_WP	I					Write Protection Switch in SD
9	SD_INS	I	VSS2	VSS2	INS	INS	Card Detection

Table 60 Sharing of pins for Memory Stick and SD/MMC Memory Card Controller

6.5.2.2 Card Detection

For Memory Stick, the host or connector should provide a pull up resistor on the signal INS. Therefore, the signal INS will be logic high if no Memory Stick is on line. The scenario of card detection for Memory Stick is shown in **Figure 73**. Before Memory Stick is inserted or powered on, on host side SW1 shall be closed and SW2 shall be opened for card detection. It is the default setting when the controller is powered on. Upon insertion of Memory Stick, the signal INS will have a transition from high to low. Hereafter, if Memory Stick is removed then the signal INS will return to logic high. If card insertion is intended to not be supported, SW1 shall be opened and SW2 closed always.

For SD/MMC Memory Card, detection of card insertion/removal by hardware is also supported. Because a pull down resistor with about 470 KΩ resistance which is impractical to embed in an I/O pad is needed on the signal CD/DAT3, and it has to be capable of being connected or disconnected dynamically onto the signal CD during initialization period, an additional I/O pad is needed to switch on/off the pull down resistor on the system board. The scenario of card detection for SD/MMC Memory Card is shown in **Figure 74**. Before SD/MMC Memory Card is inserted or powered on, SW1 and SW2 shall be opened for card detection on the host side. Meanwhile, pull down resistor R_{CD} on system board shall attach onto the signal CD/DAT3 by the output signal RCDEN. In addition, SW3 on the card is default to be closed. Upon insertion of SD/MMC Memory Card, the signal CD/DAT3 will have a transition from low to high. If SD/MMC Memory Card is removed then the signal CD/DAT3 will return to logic low. After the card identification process, pull down resistor R_{CD} on system board shall disconnect with the signal CD/DAT3 and SW3 on the card shall be opened for normal operation.

Since the scheme above needs a mechanical switch such as a relay on system board, it is not ideal enough. Thus, a dedicated pin “INS” is used to perform card insertion and removal for SD/MMC. The pin “INS” will connect to the pin “VSS2” of a SD/MMC connector. Then the scheme of card detection is the same as that for MS. It is shown in **Figure 73**.

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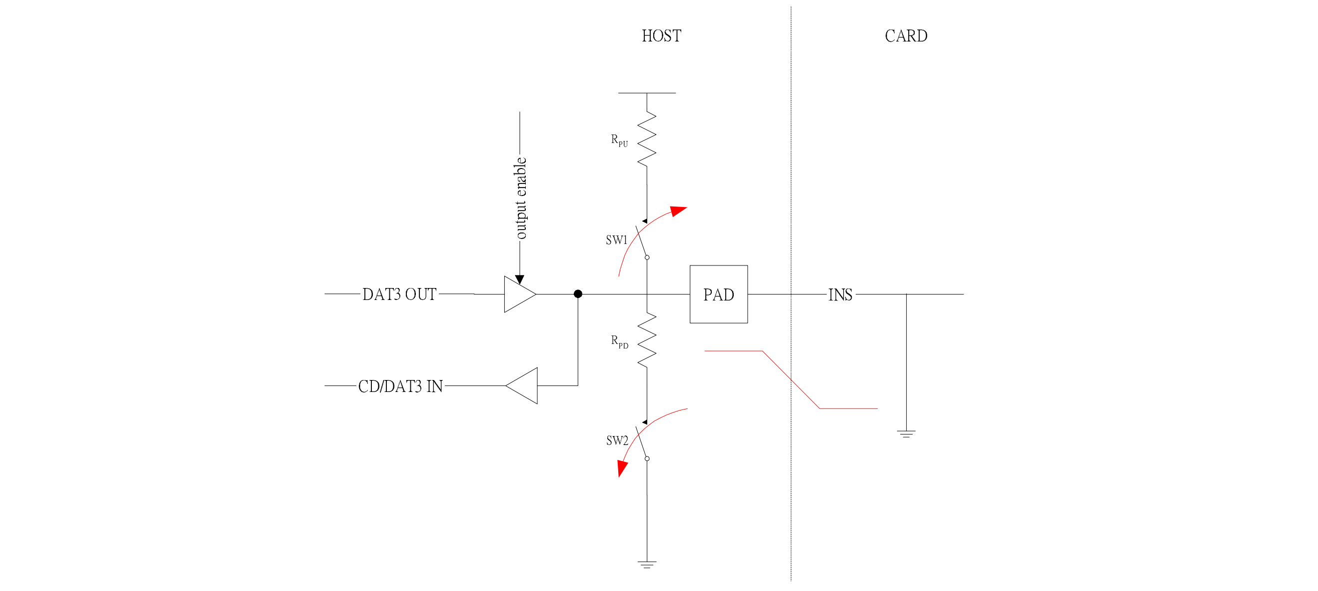

Figure 73 Card detection for Memory Stick

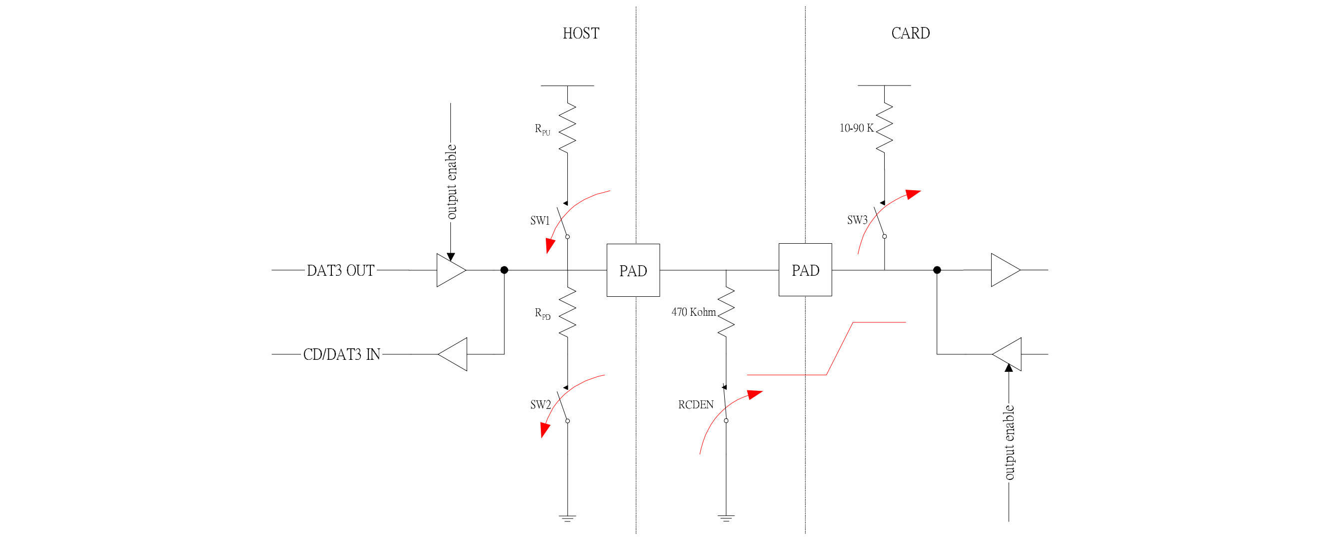

Figure 74 Card detection for SD/MMC Memory Card

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6.5.3 Register Definitions

For MT6253, MSDC base address is 0x81110000.

REGISTER ADDRESS	REGISTER NAME	SYNONYM
MSDC + 0000h	MS/SD Memory Card Controller Configuration Register	MSDC_CFG
MSDC + 0004h	MS/SD Memory Card Controller Status Register	MSDC_STA
MSDC + 0008h	MS/SD Memory Card Controller Interrupt Register	MSDC_INT
MSDC + 000Ch	MS/SD Memory Card Controller Data Register	MSDC_DAT
MSDC + 00010h	MS/SD Memory Card Pin Status Register	MSDC_PS
MSDC + 00014h	MS/SD Memory Card Controller IO Control Register	MSDC_IOCON
MSDC + 0020h	SD Memory Card Controller Configuration Register	SDC_CFG
MSDC + 0024h	SD Memory Card Controller Command Register	SDC_CMD
MSDC + 0028h	SD Memory Card Controller Argument Register	SDC_ARG
MSDC + 002Ch	SD Memory Card Controller Status Register	SDC_STA
MSDC + 0030h	SD Memory Card Controller Response Register 0	SDC_RESP0
MSDC + 0034h	SD Memory Card Controller Response Register 1	SDC_RESP1
MSDC + 0038h	SD Memory Card Controller Response Register 2	SDC_RESP2
MSDC + 003Ch	SD Memory Card Controller Response Register 3	SDC_RESP3
MSDC + 0040h	SD Memory Card Controller Command Status Register	SDC_CMDSTA
MSDC + 0044h	SD Memory Card Controller Data Status Register	SDC_DATSTA
MSDC + 0048h	SD Memory Card Status Register	SDC_CSTA
MSDC + 004Ch	SD Memory Card IRQ Mask Register 0	SDC_IRQMASK0
MSDC + 0050h	SD Memory Card IRQ Mask Register 1	SDC_IRQMASK1
MSDC + 0054h	SDIO Configuration Register	SDIO_CFG
MSDC + 0058h	SDIO Status Register	SDIO_STA
MSDC + 0060h	Memory Stick Controller Configuration Register	MSC_CFG
MSDC + 0064h	Memory Stick Controller Command Register	MSC_CMD
MSDC + 0068h	Memory Stick Controller Auto Command Register	MSC_ACMD
MSDC + 006Ch	Memory Stick Controller Status Register	MSC_STA

Table 61 MS/SD Controller Register Map

6.5.3.1 Global Register Definitions

MSDC+0000h MS/SD Memory Card Controller Configuration Register MSDC_CFG

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	FIFOTHD				PRCFG2		PRCFG1		PRCFG0		VDDPD	RCDEN	DIRQEN	PINEN	DMAEN	INTEN
Type	R/W				R/W		R/W		R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0001				01		01		10		0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCLKF								SCLKON	CRED	STDBY	CLKSRC	RST	NOCRC		MSDC
Type	R/W								R/W	R/W	R/W	R/W	W	R/W		R/W
Reset	00000000								0	0	1	0	0	0		0

The register is for general configuration of the MS/SD controller. Note that MSDC_CFG[31:16] can be accessed by 16-bit APB bus access.

MSDC The register bit is used to configure the controller as the host of Memory Stick or as the host of SD/MMC Memory card. The default value is to configure the controller as the host of Memory Stick.

- **0** Configure the controller as the host of Memory Stick
- **1** Configure the controller as the host of SD/MMC Memory card

NOCRC CRC Disable. A ‘1’ indicates that data transfer without CRC is desired. For write data block, data will be transmitted without CRC. For read data block, CRC will not be checked. It is for testing purpose.

- **0** Data transfer with CRC is desired.
- **1** Data transfer without CRC is desired.

RST Software Reset. Writing a ‘1’ to the register bit will cause internal synchronous reset of MS/SD controller, but does not reset register settings.

- **0** Otherwise
- **1** Reset MS/SD controller

CLKSRC The register bit specifies which clock is used as source clock of memory card. If MUC clock is used, the fastest clock rate for memory card is 52/2=26MHz. If MCPLL clock is used, the fastest clock rate for memory card is 91/4 =22.75MHz.

- **0** Use MCU clock as source clock of memory card.
- **1** Use MCPLL clock as source clock of memory card.

STDBY Standby Mode. If the module is powered down, operating clock to the module will be stopped. At the same time, clock to card detection circuitry will also be stopped. If detection of memory card insertion and removal is desired, write ‘1’ to the register bit. If interrupt for detection of memory card insertion and removal is enabled, interrupt will take place whenever memory is inserted or removed.

- **0** Standby mode is disabled.
- **1** Standby mode is enabled.

RED Rise Edge Data. The register bit is used to determine that serial data input is latched at the falling edge or the rising edge of serial clock. The default setting is at the rising edge. If serial data has worse timing, set the register bit to ‘1’. **When memory card has worse timing on return read data, set the register bit to ‘1’.**

- **0** Serial data input is latched at the rising edge of serial clock.
- **1** Serial data input is latched at the falling edge of serial clock.

SCLKON Serial Clock Always On. It is for debugging purpose.

- **0** Not to have serial clock always on.

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1 To have serial clock always on.

SCLKF The register field controls clock frequency of serial clock on MS/SD bus. Denote clock frequency of MS/SD bus serial clock as f_{slave} and clock frequency of the MS/SD controller as f_{host} which is 104 or 52 MHz. Then the value of the register field is as follows. **Note that the allowable maximum frequency of f_{slave} is 26MHz. While changing clock rate, it needs " 1T clock period before change + 1T clock period after change" for HW signal to re-synchronize.**

00000000b f_{slave} =(1/2) * f_{host}

00000001b f_{slave} = (1/(4*1)) * f_{host}

00000010b f_{slave} = (1/(4*2)) * f_{host}

00000011b f_{slave} = (1/(4*3))* f_{host}

…

00010000b f_{slave} = (1/(4*16))* f_{host}

…

11111111b f_{slave} = (1/(4*255)) * f_{host}

INTEN Interrupt Enable. Note that if interrupt capability is disabled then application software must poll the status of the register MSDC_STA to check for any interrupt request.

0 Interrupt induced by various conditions is disabled, no matter the controller is configured as the host of either SD/MMC Memory Card or Memory Stick.

1 Interrupt induced by various conditions is enabled, no matter the controller is configured as the host of either SD/MMC Memory Card or Memory Stick.

DMAEN DMA Enable. Note that if DMA capability is disabled then application software must poll the status of the register MSDC_STA for checking any data transfer request. If DMA is desired, the register bit must be set before command register is written.

0 DMA request induced by various conditions is disabled, no matter the controller is configured as the host of either SD/MMC Memory Card or Memory Stick.

1 DMA request induced by various conditions is enabled, no matter the controller is configured as the host of either SD/MMC Memory Card or Memory Stick.

PINEN Pin Interrupt Enable. The register bit is used to control if the pin for card detection is used as an interrupt source.

0 The pin for card detection is not used as an interrupt source.

1 The pin for card detection is used as an interrupt source.

DIRQEN Data Request Interrupt Enable. The register bit is used to control if data request is used as an interrupt source.

0 Data request is not used as an interrupt source.

1 Data request is used as an interrupt source.

RCDEN The register bit controls the output pin RCDEN that is used for card identification process when the controller is for SD/MMC Memory Card. Its output will control the pull down resistor on the system board to connect or disconnect with the signal CD/DAT3.

0 The output pin RCDEN will output logic low.

1 The output pin RCDEN will output logic high.

VDDPD The register bit controls the output pin VDDPD that is used for power saving. The output pin VDDPD will control power for memory card.

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0 The output pin VDDPD will output logic low. The power for memory card will be turned off.

1 The output pin VDDPD will output logic high. The power for memory card will be turned on.

PRCFG0 Pull Up/Down Register Configuration for the pin WP. The default value is 10.

00 Pull up resistor and pull down resistor in the I/O pad of the pin WP are all disabled.

01 Pull down resistor in the I/O pad of the pin WP is enabled.

10 Pull up resistor in the I/O pad of the pin WP is enabled.

11 Use keeper of IO pad.

PRCFG1 Pull Up/Down Register Value for the pins CMD/BS. The default value is 0b01. **Note that pull up configuration for the pins CMD/BS with the register bit MCCPUPD in ACIF_CON3 setting to 1. Pull down configuration for the pins CMD/BS with the register bit MCCPUPD in ACIF_CON3(0x8001070c) setting to 0.**

00 Pull up resistor and pull down resistor in the I/O pad of the pin CMD/BS are all disabled.

01 Pull up/down resistor in the I/O pad of the pin CMD/BS value is 47k.

10 Pull up/down resistor in the I/O pad of the pin CMD/BS value is 47k.

11 Pull up/down resistor in the I/O pad of the pin CMD/BS value is 23.5k.

PRCFG2 Pull Up/Down Register Value for the pins DAT0, DAT1, DAT2, DAT3. The default value is 0b01. **Note that pull up configuration for the pins DAT0, DAT1, DAT2, DAT3 with the register bit MCDPUPD in ACIF_CON3 setting to 1. Pull down configuration for the pins DAT0, DAT1, DAT2, DAT3 with the register bit MCDPUPD in ACIF_CON3(0x8001070c) setting to 0. And DAT pin enable configuration from DAT0 to DAT3 is the register bit from GPIO71 to GPIO68 in GPIO_PULLSEL5(0x80020090)**.

00 Pull up resistor and pull down resistor in the I/O pad of the pin DAT are all disabled.

01 Pull up/down resistor in the I/O pad of the pin DAT value is 47k.

10 Pull up/down resistor in the I/O pad of the pin DAT value is 47k.

11 Pull up/down resistor in the I/O pad of the pin DAT value is 23.5k.

FIFOTHD FIFO Threshold. The register field determines when to issue a DMA request. For write transactions, DMA requests will be asserted if the number of free entries in FIFO are larger than or equal to the value in the register field. For read transactions, DMA requests will be asserted if the number of valid entries in FIFO are larger than or equal to the value in the register field. The register field must be set according to the setting of data transfer count in DMA burst mode. If single mode for DMA transfer is used, the register field shall be set to 0b0001.

0000 Invalid.

0001 Threshold value is 1.

0010 Threshold value is 2.

…

1000 Threshold value is 8.

others Invalid

MSDC+0004h MS/SD Memory Card Controller Status Register MSDC_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUSY	FIFOCLR							FIFOCNT				INT	DRQ	BE	BF
Type	R	W							RO				RO	RO	RO	RO

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Reset	0	-							0000	0	0	0	0

The register contains the status of FIFO, interrupts and data requests.

BF The register bit indicates if FIFO in MS/SD controller is full.

- **0** FIFO in MS/SD controller is not full.
- **1** FIFO in MS/SD controller is full.

BE The register bit indicates if FIFO in MS/SD controller is empty.

- **0** FIFO in MS/SD controller is not empty.
- **1** FIFO in MS/SD controller is empty.

DRQ The register bit indicates if any data transfer is required. While any data transfer is required, the register bit still will be active even if the register bit DIRQEN in the register MSDC_CFG is disabled. Data transfer can be achieved by DMA channel alleviating MCU loading, or by polling the register bit to check if any data transfer is requested. While the register bit DIRQEN in the register MSDC_CFG is disabled, the second method is used.

- **0** No DMA request exists.
- **1** DMA request exists.

INT The register bit indicates if any interrupt exists. While any interrupt exists, the register bit still will be active even if the register bit INTEN in the register MSDC_CFG is disabled. MS/SD controller can interrupt MCU by issuing interrupt request to Interrupt Controller, or software/application polls the register endlessly to check if any interrupt request exists in MS/SD controller. While the register bit INTEN in the register MSDC_CFG is disabled, the second method is used. For read commands, it is possible that timeout error takes place. Software can read the status register to check if timeout error takes place without OS time tick support or data request is asserted. Note that the register bit will be cleared when reading the register MSDC_INT.

- **0** No interrupt request exists.
- **1** Interrupt request exists.

FIFOCNT FIFO Count. The register field shows how many valid entries are in FIFO.

- **0000** There is 0 valid entry in FIFO.
- **0001** There is 1 valid entry in FIFO.
- **0010** There are 2 valid entries in FIFO.
- **...**
- **1000** There are 8 valid entries in FIFO.
- **others** Invalid

FIFOCLR Clear FIFO. Writing '1' to the register bit will cause the content of FIFO clear and reset the status of FIFO controller.

- **0** No effect on FIFO.
- **1** Clear the content of FIFO clear and reset the status of FIFO controller.

BUSY Status of the controller. If the controller is in busy state, the register bit will be '1'. Otherwise '0'.

- **0** The controller is in busy state.
- **1** The controller is in idle state.

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MSDC+0008h MS/SD Memory Card Controller Interrupt Register MSDC_INT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SDIOIRQ	SDR1BIRQ	MSIFIRQ	SDMCIRQ	SDDATIRQ	SDCMDIRQ	PINIRQ	DIRQ
Type									RC	RC	RC	RC	RC	RC	RC	RC
Reset									0	0	0	0	0	0	0	0

The register contains the status of interrupts. Note that the register still show status of interrupt even though interrupt is disabled, that is, the register bit INTEN of the register MSDC_CFG is set to '0. It implies that software interrupt can be implemented by polling the register bit INT of the register MSDC_STA and this register. **However, if hardware interrupt is desired, remember to clear the register before setting the register bit INTEN of the register MSDC_CFG to '1'. Or undesired hardware interrupt arisen from previous interrupt status may take place.**

DIRQ Data Request Interrupt. The register bit indicates if any interrupt for data request exists. Whenever data request exists and data request as an interrupt source is enabled, i.e., the register bit DIRQEN in the register MSDC_CFG is set to '1', the register bit will be active. It will be reset when reading it. For software, data requests can be recognized by polling the register bit DRQ or by data request interrupt. Data request interrupts will be generated every FIFOTHD data transfers.

- **0** No Data Request Interrupt.
- **1** Data Request Interrupt occurs.

PINIRQ Pin Change Interrupt. The register bit indicates if any interrupt for memory card insertion/removal exists. Whenever memory card is inserted or removed and card detection interrupt is enabled, i.e., the register bit PINEN in the register MSDC_CFG is set to '1', the register bit will be set to '1'. It will be reset when the register is read.

- **0** Otherwise.
- **1** Card is inserted or removed.

SDCMDIRQ SD Bus CMD Interrupt. The register bit indicates if any interrupt for SD CMD line exists. Whenever interrupt for SD CMD line exists, i.e., any bit in the register SDC_CMDSTA is active, the register bit will be set to '1' if interrupt is enabled. It will be reset when the register is read.

- **0** No SD CMD line interrupt.
- **1** SD CMD line interrupt exists.

SDDATIRQ SD Bus DAT Interrupt. The register bit indicates if any interrupt for SD DAT line exists. Whenever interrupt for SD DAT line exists, i.e., any bit in the register SDC_ DATSTA is active, the register bit will be set to '1' if interrupt is enabled. It will be reset when the register is read.

- **0** No SD DAT line interrupt.
- **1** SD DAT line interrupt exists.

SDMCIRQ SD Memory Card Interrupt. The register bit indicates if any interrupt for SD Memory Card exists. Whenever interrupt for SD Memory Card exists, i.e., any bit in the register SDC_CSTA is active, the register bit will be set to '1' if interrupt is enabled. It will be reset when the register is read.

- **0** No SD Memory Card interrupt.
- **1** SD Memory Card interrupt exists.

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MSIFIRQ MS Bus Interface Interrupt. The register bit indicates if any interrupt for MS Bus Interface exists. Whenever interrupt for MS Bus Interface exists, i.e., any bit in the register MSC_STA is active, the register bit will be set to '1' if interrupt is enabled. It will be reset when the register MSDC_STA or MSC_STA is read.

0 No MS Bus Interface interrupt.

1 MS Bus Interface interrupt exists.

SDR1BIRQ SD/MMC R1b Response Interrupt. The register bit will be active when a SD/MMC command with R1b response finishes and the DAT0 line has transition from busy to idle state. **Single block write commands with R1b response will cause the interrupt when the command completes no matter successfully or with CRC error. However, multi-block write commands with R1b response do not cause the interrupt because multi-block write commands are always stopped by STOP_TRANS commands. STOP_TRANS commands (with R1b response) behind multi-block write commands will cause the interrupt. Single block read command with R1b response will cause the interrupt when the command completes but multi-block read commands do not. Note that STOP_TRANS commands (with R1b response) behind multi-block read commands will cause the interrupt.**

0 No interrupt for SD/MMC R1b response.

1 Interrupt for SD/MMC R1b response exists.

MSDC+000Ch MS/SD Memory Card Controller Data Register MSDC_DAT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA[31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA[15:0]															
Type	R/W															

The register is used to read/write data from/to FIFO inside MS/SD controller. Data access is in unit of 32 bits.

MSDC+0010h MS/SD Memory Card Pin Status Register MSDC_PS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								CMD	DAT							
Type								RO	RO							
Reset								-	-							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDDEBOUNCE											PINCHG	PIN0	POEN0	PIEN0	CDEN
Type	RW											RC	RO	R/W	R/W	R/W
Reset	0000											0	1	0	0	0

The register is used for card detection. When the memory card controller is powered on, and the system is powered on, the power for the memory card is still off unless power has been supplied by the PMIC. Meanwhile, pad for card detection defaults to pull down when the system is powered on. The scheme of card detection for MS is the same as that for SD/MMC.

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For detecting card insertion, first pull up INS pin, and then enable card detection and input pin at the same time. After 32 cycles of controller clock, status of pin changes will emerge. For detecting card removal, just keep enabling card detection and input pin.

CDEN Card Detection Enable. The register bit is used to enable or disable card detection.
- **0** Card detection is disabled.
- **1** Card detection is enabled.

PIEN0 The register bit is used to control input pin for card detection.
- **0** Input pin for card detection is disabled.
- **1** Input pin for card detection is enabled.

POEN0 The register bit is used to control output of input pin for card detection.
- **0** Output of input pin for card detection is disabled.
- **1** Output of input pin for card detection is enabled.

PIN0 The register shows the value of input pin for card detection.
- **0** The value of input pin for card detection is logic low.
- **1** The value of input pin for card detection is logic high.

PINCHG Pin Change. The register bit indicates the status of card insertion/removal. If memory card is inserted or removed, the register bit will be set to '1' no matter pin change interrupt is enabled or not. It will be cleared when the register is read.
- **0** Otherwise.
- **1** Card is inserted or removed.

CDDEBOUNCE The register field specifies the time interval for card detection de-bounce. Its default value is 0. It means that de-bounce interval is 32 cycle time of 32KHz. The interval will extend one cycle time of 32KHz by increasing the counter by 1.

DAT Memory Card Data Lines.

CMD Memory Card Command Lines.

MSDC+0014h MS/SD Memory Card Controller IO Control Register MSDC_IOCON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DLT											CRCDIS	CMDSEL	INTLH		DSW
Type	R/W											R/W	R/W	R/W		R/W
Reset	00000010											0	0	0		0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CMDRE						PRCFG3		SRCFG1	SRCFG0	ODCCFG1			ODCCFG0		
Type	R/W						R/W		R/W	R/W	R/W			R/W		
Reset	0						10		1	1	000			011		

The register specifies **Output Driving Capability** and **Slew Rate** of IO pads for MSDC. The reset value is suggestion setting. If output driving capability of the pins DAT0, DAT1, DAT2 and DAT3 is too large, it's possible to arise ground bounce and thus result in glitch on SCLK. The actual driving current will depend on the PAD type selected for the chip.

ODCCFG0 Output driving capability the pins CMD/BS and SCLK

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000 4mA
010 12mA
100 8mA
110 16mA

ODCCFG1 Output driving capability the pins DAT0, DAT1, DAT2 and DAT3
000 4mA
010 12mA
100 8mA
110 16mA

SRCFG0 Output driving capability the pins CMD/BS and SCLK
0 Fast Slew Rate
1 Slow Slew Rate

SRCFG1 Output driving capability the pins DAT0, DAT1, DAT2 and DAT3
0 Fast Slew Rate
1 Slow Slew Rate

PRCFG3 Pull Up/Down Register Configuration for the pin INS. The default value is 10.
00 Pull up resistor and pull down resistor in the I/O pad of the pin INS are all disabled.
01 Pull down resistor in the I/O pad of the pin INS is enabled.
10 Pull up resistor in the I/O pad of the pin INS is enabled.
11 Use keeper of IO pad.

CMDRE The register bit is used to determine whether the host should latch response token (which is sent from card on CMD line) at rising edge or falling edge of serial clock.
0 Host latches response at rising edge of serial clock
1 Host latches response at falling edge of serial clock

DSW The register bit is used to determine whether the host should latch data with 1-T delay or not. For SD card, this bit is suggest to be 0. for MS/MSPRO cards, it is suggested to be 1. **Note that this field is added after MT6268 and MT6516. (TK6516 not support yet)**
0 Host latches the data with 1-T delay
1 Host latches the data without 1-T delay

INTLH This field is used to select the latch timing for SDIO multi-block read interrupt. **Note that this field is added after MT6268 and MT6516. (TK6516 not support yet)**
00 Host latches INT at the second backend clock after the end bit of current data block from card is received. (This is the default setting)
01 Host latches INT at the first backend clock after the end bit of current data block from card is received.
10 Host latches INT at the second backend clock after the end bit of current data block from card is received.
11 Host latches INT at the third backend clock after the end bit of current data block from card is received.

CMDSEL The register bit is used to determine whether the host should delay 1-T to latch response from card. **Note that this field is added after MT6268 and MT6516. (TK6516 not support yet)**
0 Host latches response without 1-T delay.
1 Host latches response with 1-T delay.

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CRCDIS The register bit is used to switch-off the data CRC check for SD/MMC read data. **Note that this field is added after MT6268 and MT6516. (TK6516 not support yet)**

- **0** CRC Check is on.
- **1** CRC Check is off.

DLT Data Latch Timing. The register is used for SW to select the latch timing on data line. **Figure 75** illustrates the data line latch timing. sclk_out is the serial clock output to card. div_clk is the internal clock used for generating divided clock. The number "1 2 1 2" means the current sclk_out is divided from div_clk by a ratio of 2. data_in is the output data from card, and latched_data(r)/(f) is the rising/falling edge latched data inside the host (configured by RED in MSDC_CFG). In this example, SCLKF(in MSDC_CFG) is set to 8'b0 which means the division ratio is 2, and DLT is set to 1. Note that the value of DLT CANNOT be set as 0 and its value should not exceed the division ratio (in the example, the division ratio is 2). Also note that, the latching time will be one div_clk later than the indicated DLT value and the falling edge is always half div_clk ahead from rising edge. The default value of DLT is set to 8'b2.

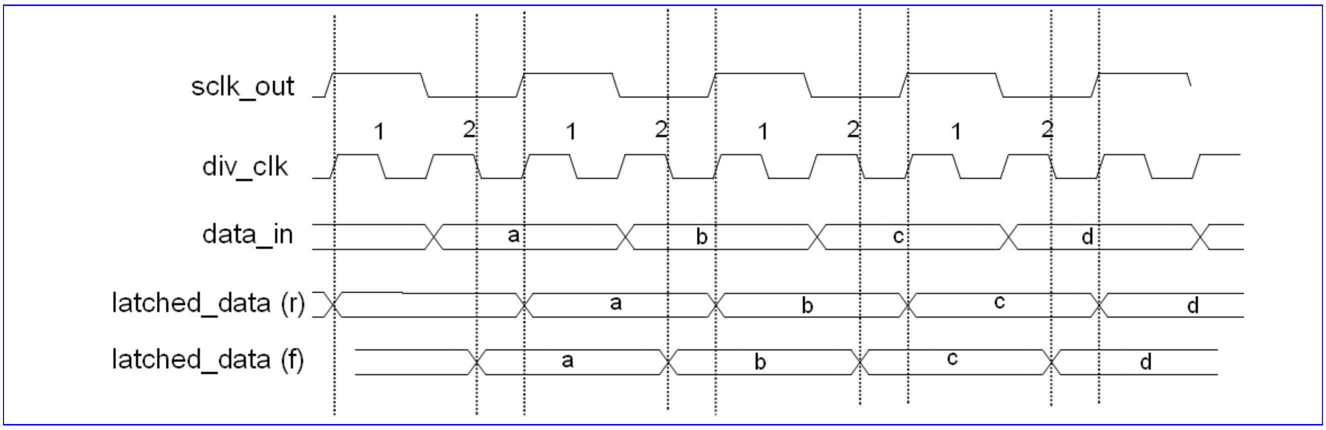

Figure 75 Illustration of data line latch timing

6.5.3.2 SD Memory Card Controller Register Definitions

MSDC+0020h SD Memory Card Controller Configuration Register SDC_CFG

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DTOC								WDOD				SDIO	MDLW8	MDLEN	SIEN
Type	R/W								R/W				R/W	R/W	R/W	R/W
Reset	00000000								0000				0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSYDLY				BLKLEN											
Type	R/W				R/W											
Reset	1000				00000000000											

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The register is used for configuring the MS/SD Memory Card Controller when it is configured as the host of SD Memory Card. If the controller is configured as the host of Memory Stick, the contents of the register have no impact on the operation of the controller. Note that SDC_CFG[31:16] can be accessed by 16-bit APB bus access.

BLKLEN It refers to Block Length. The register field is used to define the length of one block in unit of byte in a data transaction. The maximal value of block length is 2048 bytes.

000000000000 Reserved.
000000000001 Block length is 1 byte.
000000000010 Block length is 2 bytes.
…
011111111111 Block length is 2047 bytes.
100000000000 Block length is 2048 bytes.

BSYDLY The register field is only valid for the commands with R1b response. If the command has a response of R1b type, MS/SD controller must monitor the data line 0 for card busy status from the bit time that is two serial clock cycles after the command end bit to check if operations in SD/MMC Memory Card have finished. The register field is used to expand the time between the command end bit and end of detection period to detect card busy status. If time is up and there is no card busy status on data line 0, then the controller will abandon the detection.

0000 No extend.
0001 Extend one more serial clock cycle.
0010 Extend two more serial clock cycles.
…
1111 Extend fifteen more serial clock cycle.

SIEN Serial Interface Enable. It should be enabled as soon as possible before any command.

0 Serial interface for SD/MMC is disabled.
1 Serial interface for SD/MMC is enabled.

MDLW8 Eight Data Line Enable. The register works when MDLEN is enabled. The register can be enabled only when MultiMediaCard 4.0 is applied and detected by software application.

0 4-bit Data line is enabled.
1 8-bit Data line is enabled.

SDIO SDIO Enable.

0 SDIO mode is disabled
1 SDIO mode is enabled

MDLEN Multiple Data Line Enable. The register can be enabled only when SD Memory Card is applied and detected by software application. It is the responsibility of the application to program the bit correctly when an MultiMediaCard is applied. If an MultiMediaCard is applied and 4-bit data line is enabled, then 4 bits will be output every serial clock. Therefore, data integrity will fail.

0 4-bit Data line is disabled.
1 4-bit Data line is enabled.

WDOD Write Data Output Delay. The period from finish of the response for the initial host write command or the last write data block in a multiple block write operation to the start bit of the next write data block requires at least two

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serial clock cycles. The register field is used to extend the period (Write Data Output Delay) in unit of one serial clock.

0000 No extend.
0001 Extend one more serial clock cycle.
0010 Extend two more serial clock cycles.
…
1111 Extend fifteen more serial clock cycle.

DTOC Data Timeout Counter. The period from finish of the initial host read command or the last read data block in a multiple block read operation to the start bit of the next read data block requires at least two serial clock cycles. The counter is used to extend the period (Read Data Access Time) in unit of 65,536 serial clock. See the register field description of the register bit RDINT for reference.

00000000 Extend 65,536 more serial clock cycle.
00000001 Extend 65,536x2 more serial clock cycle.
00000010 Extend 65,536x3 more serial clock cycle.
…
11111111 Extend 65,536x 256 more serial clock cycle.

MSDC+0024h SD Memory Card Controller Command Register SDC_CMD

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																CMDFAIL
Type																R/W
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INTC	STOP	RW	DTYPE		IDRT	RSPTYP			BREAK	CMD					
Type	R/W	R/W	R/W	R/W		R/W	R/W			R/W	R/W					
Reset	0	0	0	00		0	000			0	000000					

The register defines a SD Memory Card command and its attribute. Before MS/SD controller issues a transaction onto SD bus, application shall specify other relative setting such as argument for command. After application writes the register, MS/SD controller will issue the corresponding transaction onto SD serial bus. If the command is GO_IDLE_STATE, the controller will have serial clock on SD/MMC bus run 128 cycles before issuing the command.

CMD SD Memory Card command. It is totally 6 bits.

BREAK Abort a pending MMC GO_IRQ_MODE command. It is only valid for a pending GO_IRQ_MODE command waiting for MMC interrupt response.

0 Other fields are valid.
1 Break a pending MMC GO_IRQ_MODE command in the controller. Other fields are invalid.

RSPTYP The register field defines response type for the command. For commands with R1 and R1b response, the register SDC_CSTA (not SDC_STA) will update after response token is received. This register SDC_CSTA contains the status of the SD/MMC and it will be used as response interrupt sources. Note that if CMD7 is used with all 0's RCA then RSPTYP must be "000". And the command "GO_TO_IDLE" also have RSPTYP='000'.

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000 There is no response for the command. For instance, broadcast command without response and GO_INACTIVE_STATE command.

001 The command has R1 response. R1 response token is 48-bit.

010 The command has R2 response. R2 response token is 136-bit.

011 The command has R3 response. Even though R3 is 48-bit response, but it does not contain CRC checksum.

100 The command has R4 response. R4 response token is 48-bit. (Only for MMC)

101 The command has R5 response. R5 response token is 48-bit. (Only for MMC)

110 The command has R6 response. R6 response token is 48-bit.

111 The command has R1b response. If the command has a response of R1b type, MS/SD controller must monitor the data line 0 for card busy status from the bit time that is two or four serial clock cycles after the command end bit to check if operations in SD/MMC Memory Card have finished. There are two cases for detection of card busy status. The first case is that the host stops the data transmission during an active write data transfer. The card will assert busy signal after the stop transmission command end bit followed by four serial clock cycles. The second case is that the card is in idle state or under a scenario of receiving a stop transmission command between data blocks when multiple block write command is in progress. The register bit is valid only when the command has a response token.

IDRT Identification Response Time. The register bit indicates if the command has a response with N_{ID} (that is, 5 serial clock cycles as defined in SD Memory Card Specification Part 1 Physical Layer Specification version 1.0) response time. The register bit is valid only when the command has a response token. Thus the register bit must be set to '1' for CMD2 (ALL_SEND_CID) and ACMD41 (SD_APP_OP_CMD).

0 Otherwise.

1 The command has a response with N_{ID} response time.

DTYPE The register field defines data token type for the command.

00 No data token for the command

01 Single block transaction

10 Multiple block transaction. That is, the command is a multiple block read or write command.

11 Stream operation. It only shall be used when an MultiMediaCard is applied.

RW The register bit defines the command is a read command or write command. The register bit is valid only when the command will cause a transaction with data token.

0 The command is a read command.

1 The command is a write command.

STOP The register bit indicates if the command is a stop transmission command.

0 The command is not a stop transmission command.

1 The command is a stop transmission command.

INTC The register bit indicates if the command is GO_IRQ_STATE. If the command is GO_IRQ_STATE, the period between command token and response token will not be limited.

0 The command is not GO_IRQ_STATE.

1 The command is GO_IRQ_STATE.

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MSDC+0028h SD Memory Card Controller Argument Register SDC_ARG

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARG [31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARG [15:0]															
Type	R/W															

The register contains the argument of the SD/MMC Memory Card command.

MSDC+002Ch SD Memory Card Controller Status Register SDC_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WP											FEDATBUSY	FECMDBUSY	BEDATBUSY	BECMDBUSY	BESDCBUSY
Type	R											RO	RO	RO	RO	RO
Reset	-											0	0	0	0	0

The register contains various status of MS/SD controller as the controller is configured as the host of SD Memory Card.

BESDCBUSY The register field indicates if MS/SD controller is busy, that is, any transmission is going on CMD or DAT line on SD bus. This bit shows backend controller's SDC busy state. The busy state is sync from card clock domain to bus clock domain.

- **0** Backend MS/SD controller is idle.
- **1** Backend MS/SD controller is busy.

BECMDBUSY The register field indicates if any transmission is going on CMD line on SD bus. This bit shows backend controller's CMD busy state. The busy state is sync from card clock domain to bus clock domain.

- **0** Backend MS/SDC Controller gets the info that no transmission is going on CMD line on SD bus.
- **1** Backend MS/SDC Controller gets the info that there exists transmission going on CMD line on SD bus.

BEDATBUSY The register field indicates if any transmission is going on DAT line on SD bus.

- **0** Backend MS/SDC Controller gets the info that no transmission is going on DAT line on SD bus.
- **1** Backend MS/SDC Controller gets the info that there exists transmission going on DAT line on SD bus.

FECCMDBUSY The register field indicates if any transmission is going on CMD line on SD bus. This bit indicates directly the CMD line at card clock domain.

- **0** No transmission is going on CMD line on SD bus.
- **1** There exists transmission going on CMD line on SD bus.

FEDATBUSY The register field indicates if any transmission is going on DAT line on SD bus. This bit indicates directly the CMD line at card clock domain. **For those commands without data but still involving DAT line, the register bit is useless. For example, if an Erase command is issued, then checking if the register bit is '0' before issuing next command with data would not guarantee that the controller is idle. In this situation, use the register bit BESDCBUSY.**

- **0** No transmission is going on DAT line on SD bus.
- **1** There exists transmission going on DAT line on SD bus.

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WP It is used to detect the status of Write Protection Switch on SD Memory Card. The register bit shows the status of Write Protection Switch on SD Memory Card. There is no default reset value. The pin WP (Write Protection) is also only useful while the controller is configured for SD Memory Card.

1 Write Protection Switch ON. It means that memory card is desired to be write-protected.

0 Write Protection Switch OFF. It means that memory card is writable.

MSDC+0030h SD Memory Card Controller Response Register 0 SDC_RESP0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP [31:16]															
Type	RO															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP [15:0]															
Type	RO															

The register contains parts of the last SD/MMC Memory Card bus response. See description for the register field SDC_RESP3.

MSDC+0034h SD Memory Card Controller Response Register 1 SDC_RESP1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP [63:48]															
Type	RO															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP [47:32]															
Type	RO															

The register contains parts of the last SD/MMC Memory Card bus response. See description for the register field SDC_RESP3.

MSDC+0038h SD Memory Card Controller Response Register 2 SDC_RESP2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP [95:80]															
Type	RO															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP [79:64]															
Type	RO															

The register contains parts of the last SD/MMC Memory Card bus response. See description for the register field SDC_RESP3.

MSDC+003Ch SD Memory Card Controller Response Register 3 SDC_RESP3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP [127:112]															
Type	RO															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP [111:96]															
Type	RO															

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The register contains parts of the last SD/MMC Memory Card bus response. The register fields SDC_RESP0, SDC_RESP1, SDC_RESP2 and SDC_RESP3 compose the last SD/MMC Memory card bus response. For response of type R2, that is, response of the command ALL_SEND_CID, SEND_CSD and SEND_CID, only bit 127 to 0 of response token is stored in the register field SDC_RESP0, SDC_RESP1, SDC_RESP2 and SDC_RESP3. For response of other types, only bit 39 to 8 of response token is stored in the register field SDC_RESP0.

MSDC+0040h SD Memory Card Controller Command Status Register SDC_CMDSTA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MMCIRQ	RSPCRCERR	CMDTO	CMDRDY
Type													RC	RC	RC	RC
Reset													0	0	0	0

The register contains the status of MS/SD controller during command execution and that of MS/SD bus protocol after command execution when MS/SD controller is configured as the host of SD/MMC Memory Card. The register will also be used as interrupt sources. The register will be cleared when reading the register. Meanwhile, if interrupt is enabled and thus interrupt caused by the register is generated, reading the register will deassert the interrupt.

CMDRDY For command without response, the register bit will be '1' once the command completes on SD/MMC bus. For command with response, the register bit will be '1' whenever the command is issued onto SD/MMC bus and its corresponding response is received **without CRC error**.

0 Otherwise.

1 Command with/without response finish successfully without CRC error.

CMDTO Timeout on CMD detected. A '1' indicates that MS/SD controller detected a timeout condition while waiting for a response on the CMD line.

0 Otherwise.

1 MS/SD controller detected a timeout condition while waiting for a response on the CMD line.

RSPCRCERR CRC error on CMD detected. A '1' indicates that MS/SD controller detected a CRC error **after reading a response from the CMD line.**

0 Otherwise.

1 MS/SD controller detected a CRC error after reading a response from the CMD line.

MMCIRQ MMC requests an interrupt. A '1' indicates that a MMC supporting command class 9 issued an interrupt request.

0 Otherwise.

1 A '1' indicates that a MMC supporting command class 9 issued an interrupt request.

MSDC+0044h SD Memory Card Controller Data Status Register SDC_DATSTA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DATCRCERR	DATTO	BLKDONE
Type														RC	RC	RC

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Reset														0	0	0

The register contains the status of MS/SD controller during data transfer on DAT line(s) when MS/SD controller is configured as the host of SD/MMC Memory Card. The register also will be used as interrupt sources. The register will be cleared when reading the register. Meanwhile, if interrupt is enabled and thus interrupt caused by the register is generated, reading the register will deassert the interrupt.

BLKDONE The register bit indicates the status of data block transfer.

0 Otherwise.

1 A data block was successfully transferred.

DATTO Timeout on DAT detected. A ‘1’ indicates that MS/SD controller detected a timeout condition while waiting for data token on the DAT line.

0 Otherwise.

1 MS/SD controller detected a timeout condition while waiting for data token on the DAT line.

DATCRCERR CRC error on DAT detected. A ‘1’ indicates that MS/SD controller detected a CRC error after reading a block of data from the DAT line or SD/MMC signaled a CRC error after writing a block of data to the DAT line.

0 Otherwise.

1 MS/SD controller detected a CRC error after reading a block of data from the DAT line or SD/MMC signaled a CRC error after writing a block of data to the DAT line.

MSDC+0048h SD Memory Card Status Register SDC_CSTA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTA [31:16]															
Type	RC															
Reset	0000000000000000															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTA [15:0]															
Type	RC															
Reset	0000000000000000															

After commands with R1 and R1b response this register contains the status of the SD/MMC card and it will be used as response interrupt sources. In all register fields, logic high indicates error and logic low indicates no error. The register will be cleared when reading the register. Meanwhile, if interrupt is enabled and thus interrupt caused by the register is generated, reading the register will deassert the interrupt.

CSTA31 **OUT_OF_RANGE**. The command’s argument was out of the allowed range for this card.

CSTA30 **ADDRESS_ERROR**. A misaligned address that did not match the block length was used in the command.

CSTA29 **BLOCK_LEN_ERROR**. The transferred block length is not allowed for this card, or the number of transferred bytes does not match the block length.

CSTA28 **ERASE_SEQ_ERROR**. An error in the sequence of erase commands occurred.

CSTA27 **ERASE_PARAM**. An invalid selection of write-blocks for erase occurred.

CSTA26 **WP_VIOLATION**. Attempt to program a write-protected block.

CSTA25 Reserved. Return zero.

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CSTA24 **LOCK_UNLOCK_FAILED**. Set when a sequence or password error has been detected in lock/unlock card command or if there was an attempt to access a locked card.
CSTA23 **COM_CRC_ERROR**. The CRC check of the previous command failed.
CSTA22 **ILLEGAL_COMMAND**. Command not legal for the card state.
CSTA21 **CARD_ECC_FAILED**. Card internal ECC was applied but failed to correct the data.
CSTA20 **CC_ERROR**. Internal card controller error.
CSTA19 **ERROR**. A general or an unknown error occurred during the operation.
CSTA18 **UNDERRUN**. The card could not sustain data transfer in stream read mode.
CSTA17 **OVERRUN**. The card could not sustain data programming in stream write mode.
CSTA16 **CID/CSD_OVERWRITE**. It can be either one of the following errors: 1. The CID register has been already written and cannot be overwritten 2. The read only section of the CSD does not match the card. 3. An attempt to reverse the copy (set as original) or permanent WP (unprotected) bits was made.
CSTA[15:4] Reserved. Return zero.
CSTA3 **AKE_SEQ_ERROR**. Error in the sequence of authentication process
CSTA[2:0] Reserved. Return zero.

MSDC+004Ch SD Memory Card IRQ Mask Register 0 SDC_IRQMASK0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQMASK [31:16]															
Type	R/W															
Reset	0000000000000000															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQMASK [15:0]															
Type	R/W															
Reset	0000000000000000															

The register contains parts of SD Memory Card Interrupt Mask Register. See the register description of the register SDC_IRQMASK1 for reference. The register will mask interrupt sources from the register SDC_CMDSTA and SDC_DATSTA. IRQMASK[15:0] is for SDC_CMDSTA and IRQMASK[31:16] for SDC_DATSTA. A ‘1’ in some bit of the register will mask the corresponding interrupt source with the same bit position. For example, if IRQMASK[0] is ‘1’ then interrupt source from the register field CMDRDY of the register SDC_ CMDSTA will be masked. A ‘0’ in some bit will not cause interrupt mask on the corresponding interrupt source from the register SDC_CMDSTA and SDC_DATSTA.

MSDC+0050h SD Memory Card IRQ Mask Register 1 SDC_IRQMASK1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQMASK [63:48]															
Type	R/W															
Reset	0000000000000000															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQMASK [47:32]															
Type	R/W															
Reset	0000000000000000															

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The register contains parts of SD Memory Card Interrupt Mask Register. The registers SDC_IRQMASK1 and SDC_IRQMASK0 compose the SD Memory Card Interrupt Mask Register. The register will mask interrupt sources from the register SDC_CSTA. A '1' in some bit of the register will mask the corresponding interrupt source with the same bit position. For example, if IRQMASK[63] is '1' then interrupt source from the register field OUT_OF_RANGE of the register SDC_ CSTA will be masked. A '0' in some bit will not cause interrupt mask on the corresponding interrupt source from the register SDC_ CSTA.

MSDC+0054h SDIO Configuration Register SDIO_CFG

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DSBSEL	INTSEL	INTEN
Type														R/W	R/W	R/W
Reset														0	0	0

The register is used to configure functionality for SDIO.

INTEN Interrupt enable for SDIO.

- **0** Disable
- **1** Enable

INTSEL Interrupt Signal Selection

- **0** Use data line 1 as interrupt signal
- **1** Use data line 5 as interrupt signal

DSBSEL Data Block Start Bit Selection.

- **0** Use data line 0 as start bit of data block and other data lines are ignored.
- **1** Start bit of a data block is received only when data line 0-3 all become low.

MSDC+0058h SDIO Status Register SDIO_STA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQ
Type																RO
Reset																0

6.5.3.3 Memory Stick Controller Register Definitions

MSDC+0060h Memory Stick Controller Configuration Register MSC_CFG

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	PMODE	PRED											BUSYCNT			SIEN
Type	R/W	R/W											R/W			R/W
Reset	0	0											101			0

The register is used for Memory Stick Controller Configuration when MS/SD controller is configured as the host of Memory Stick.

SIEN Serial Interface Enable. It should be enabled as soon as possible before any command.
- **0** Serial interface for Memory Stick is disabled.
- **1** Serial interface for Memory Stick is enabled.

BUSYCNT RDY timeout setting in unit of serial clock cycle. The register field is set to the maximum BUSY timeout time (set value x 4 +2) to wait until the RDY signal is output from the card. RDY timeout error detection is not performed when BUSYCNT is set to 0. The initial value is 0x5. That is, BUSY signal exceeding 5x4+2=22 serial clock cycles causes a RDY timeout error.
- **000** Not detect RDY timeout
- **001** BUSY signal exceeding 1x4+2=6 serial clock cycles causes a RDY timeout error.
- **010** BUSY signal exceeding 2x4+2=10 serial clock cycles causes a RDY timeout error.
- **…**
- **111** BUSY signal exceeding 7x4+2=30 serial clock cycles causes a RDY timeout error.

PRED Parallel Mode Rising Edge Data. The register field is only valid in parallel mode, that is, MSPRO mode. In parallel mode, data must be driven and latched at the falling edge of serial clock on MS bus. In order to mitigate hold time issue, the register can be set to '1' such that write data is driven by MSDC at the rising edge of serial clock on MS bus.
- **0** Write data is driven by MSDC at the falling edge of serial clock on MS bus.
- **1** Write data is driven by MSDC at the rising edge of serial clock on MS bus.

PMODE Memory Stick PRO Mode.
- **0** Use Memory Stick serial mode.
- **1** Use Memory Stick parallel mode.

MSDC+0064h Memory Stick Controller Command Register MSC_CMD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PID						DATASIZE									
Type	R/W						R/W									
Reset	0000						0000000000									

The register is used for issuing a transaction onto MS bus. Transaction on MS bus is started by writing to the register MSC_CMD. The direction of data transfer, that is, read or write transaction, is extracted from the register field PID. 16-bit CRC will be transferred for a write transaction even if the register field DATASIZE is programmed as zero under the condition where the register field NOCRC in the register MSDC_CFG is '0'. If the register field NOCRC in the register MSDC_CFG is '1' and the register field DATASIZE is programmed as zero, then writing to the register MSC_CMD will not induce transaction on MS bus. The same applies for when the register field RDY in the register MSC_STA is '0'.

DATASIZE Data size in unit of byte for the current transaction.

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0000000000 Data size is 0 byte.
0000000001 Data size is one byte.
0000000010 Data size is two bytes.
…
0111111111 Data size is 511 bytes.
1000000000 Data size is 512 bytes.

PID Protocol ID. It is used to derive Transfer Protocol Code (TPC). The TPC can be derived by cascading PID and its reverse version. For example, if PID is 0x1, then TPC is 0x1e, that is, 0b0001 cascades 0b1110. In addition, the direction of the bus transaction can be determined from the register bit 15, that is, PID[3].

MSDC+0068h Memory Stick Controller Auto Command Register MSC_ACMD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	APID					ADATASIZE										ACEN
Type	R/W					R/W										R/W
Reset	0111					0000000001										0

The register is used for issuing a transaction onto MS bus automatically after the MS command defined in MSC_CMD completed on MS bus. Auto Command is a function used to automatically execute a command like GET_INT or READ_REG for checking status after SET_CMD ends. If auto command is enabled, the command set in the register will be executed once the INT signal on MS bus is detected. After auto command is issued onto MS bus, the register bit ACEN will become disabled automatically. Note that if auto command is enabled then the register bit RDY in the register MSC_STA caused by the command defined in MSC_CMD will be suppressed until auto command completes. Note that the register field ADATASIZE cannot be set to zero, or the result will be unpredictable.

ACEN Auto Command Enable.
0 Auto Command is disabled.
1 Auto Command is enabled.

ADATASIZE Data size in unit of byte for Auto Command. Initial value is 0x01.
0000000000 Data size is 0 byte.
0000000001 Data size is one byte.
0000000010 Data size is two bytes.
…
0111111111 Data size is 511 bytes.
1000000000 Data size is 512 bytes.

APID Auto Command Protocol ID. It is used to derive Transfer Protocol Code (TPC). Initial value is GSET_INT(0x7).

MSDC+006Ch Memory Stick Controller Status Register MSC_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMDNK	BREQ	ERR	CED								HSRDY	CRCER	TOER	SIF	RDY
Type	R	R	R	R								RO	RO	RO	RO	RO
Reset	0	0	0	0								0	0	0	0	1

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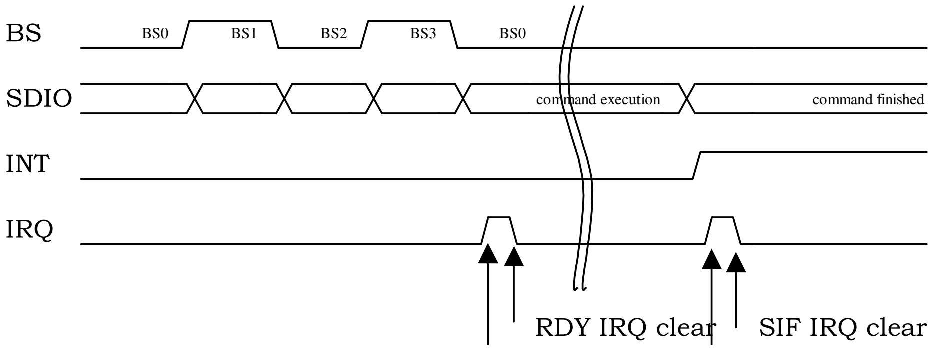
The register contains various status of Memory Stick Controller, that is, MS/SD controller is configured as Memory Stick Controller. These statuses can be used as interrupt sources. Reading the register will NOT clear it. The register will be cleared whenever a new command is written to the register MSC_CMD.

RDY The register bit indicates the status of transaction on MS bus. The register bit will be cleared when writing to the command register MSC_CMD.

- **0** Otherwise.
- **1** A transaction on MS bus is ended.

SIF The register bit indicates the status of serial interface. If an interrupt is active on MS bus, the register bit will be active. Note the difference between the signal RDY and SIF. When parallel mode is enabled, the signal SIF will be active whenever any of the signal CED, ERR, BREQ and CMDNK is active. **In order to separate interrupts caused by the signals RDY and SIF, the register bit SIF will not become active until the register MSDC_INT is read once. That is, the sequence for detecting the register bit SIF by polling is as follows:**

1. Detect the register bit RDY of the register MSC_STA
2. Read the register MSDC_INT
3. Detect the register bit SIF of the register MSC_STA



- **0** Otherwise.
- **1** An interrupt is active on MS bus

TOER The register bit indicates if a BUSY signal timeout error takes place. When timeout error occurs, the signal BS will become logic low '0'. The register bit will be cleared when writing to the command register MSC_CMD.

- **0** No timeout error.
- **1** A BUSY signal timeout error takes place. The register bit RDY will also be active.

CRCER The register bit indicates if a CRC error occurs while receiving read data. The register bit will be cleared when writing to the command register MSC_CMD.

- **0** Otherwise.
- **1** A CRC error occurs while receiving read data. The register bit RDY will also be active.

HSRDY The register bit indicates the status of handshaking on MS bus. The register bit will be cleared when writing to the command register MSC_CMD.

- **0** Otherwise.
- **1** A Memory Stick card responds to a TPC by RDY.

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CED The register bit is only valid when parallel mode is enabled. In fact, it's value is from DAT[0] when serial interface interrupt takes place. See Format Specification version 2.0 of Memory Stick Standard (Memory Stick PRO) for more details.

- **0** Command does not terminate.
- **1** Command terminates normally or abnormally.

ERR The register bit is only valid when parallel mode is enabled. In fact, it's value is from DAT[1] when serial interface interrupt takes place. See Format Specification version 2.0 of Memory Stick Standard (Memory Stick PRO) for more details.

- **0** Otherwise.
- **1** Indicate memory access error during memory access command.

BREQ The register bit is only valid when parallel mode is enabled. In fact, it's value is from DAT[2] when serial interface interrupt takes place. See Format Specification version 2.0 of Memory Stick Standard (Memory Stick PRO) for more details.

- **0** Otherwise.
- **1** Indicate request for data.

CMDNK The register bit is only valid when parallel mode is enabled. In fact, it's value is from DAT[3] when serial interface interrupt takes place. See Format Specification version 2.0 of Memory Stick Standard (Memory Stick PRO) for more details.

- **0** Otherwise
- **1** Indicate non-recognized command.

6.5.4 Application Notes

6.5.4.1 Initialization Procedures After Power On

```
Disable power down control for MSDC module
```

Remember to power on MSDC module before starting any operation to it.

6.5.4.2 Card Detection Procedures

The pseudo code is as follows:

```
MSDC_CFG.PRCFG0 = 2'b10
MSDC_PS = 2'b11
MSDC_CFG.VDDPD = 1
if(MSDC_PS.PINCHG) { // card is inserted
     . . .
}
```

The pseudo code segment perform the following tasks:

1. First pull up CD/DAT3 (INS) pin.
2. Enable card detection and input pin at the same time.
3. Turn on power for memory card.

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4. Detect insertion of memory card.

6.5.4.3 Notes on Commands

For MS, check if MSC_STA.RDY is ‘1’ before issuing any command.

For SD/MMC, if the command desired to be issued involves data line, for example, commands with data transfer or R1b response, check if SDC_STA.SDCBUSY is ‘0’ before issuing. If the command desired to be issued does not involve data line, only check if SDC_STA.CMDBUSY is ‘0’ before issuing.

6.5.4.4 Notes on Data Transfer

- For SD/MMC, if multiple-block-write command is issued then only issue STOP_TRANS command inter-blocks instead of intra-blocks.
- Once SW decides to issue STOP_TRANS commands, no more data transfer from or to the controller.

6.5.4.5 Notes on Frequency Change

Before changing the frequency of serial clock on MS/SD/MMC bus, it is necessary to disable serial interface of the controller. That is, set the register bit SIEN of the register SDC_CFG to ‘0’ for SD/MMC controller, and set the register bit SIEN of the register MSC_CFG to ‘0’ for Memory Stick controller. Serial interface of the controller needs to be enabled again before starting any operation to the memory card.

6.5.4.6 Notes on Response Timeout

If a read command doest not receive response, that is, it terminates with a timeout, then register SDC_DATSTA needs to be cleared by reading it. The register bit “DATTO” should be active. However, it may take a while before the register bit becomes active. The alternative is to send the STOP_TRANS command. However, this method will receive response with illegal-command information. Also, remember to check if the register bit SDC_STA.CMDBUSY is active before issuing the STOP_TRANS command. The procedure is as follows:

1. Read command => response time out
2. Issue STOP_TRANS command => Get Response
3. Read register SDC_DATSTA to clear it

6.5.4.7 Source or Destination Address is not word-aligned

It is possible that the source address is not word-aligned when data move from memory to MSDC. Similarly, destination address may be not word-aligned when data move from MSDC to memory. This can be solved by setting DMA byte-to-word functionality.

1. DMAn_CON.SIZE=0
2. DMAn_CON.BTW=1
3. DMAn_CON.BURST=2 (or 4)

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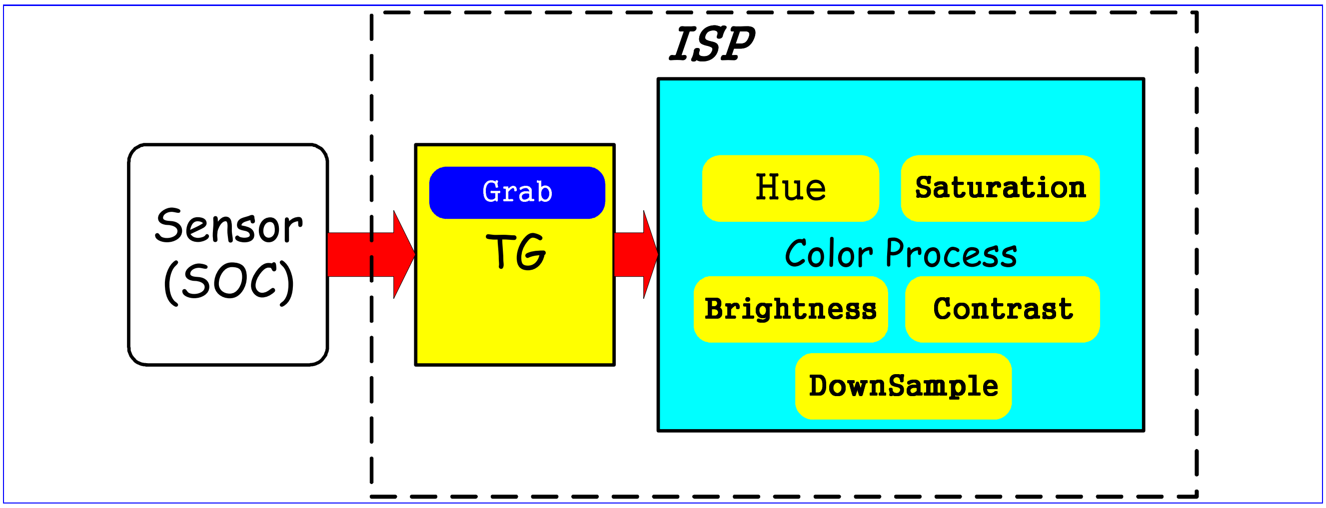
4. DMAn_COUNT=byte number instead of word number
5. fifo threshold setting must be 1 (or 2), depending on DMAn_CON.BURST

Note n=4 ~ 11

6.5.4.8 Miscellaneous notes

- Siemens MMC card: When a write command is issued and followed by a STOP_TRANS command, Siemens MMC card will de-assert busy status even though flash programming has not yet finished. Software must use "Get Status" command to make sure that flash programming finishes.

6.6 Camera Interface



MT6253 ISP support VGA Sensor YUV422/RGB565 interface. Included Functions are Brightness、Contrast、Saturation、Hue Tuning and Input Image Grab Window. Down Sample Function can be used before image output from ISP.

6.6.1 Register Table

CAM = 0x8402_0000

REGISTER ADDRESS	REGISTER NAME	SYNONYM
CAM + 0000h	TG Phase Counter Register	CAM_PHSCNT
CAM + 0004h	Sensor Size Configuration Register	CAM_CAMWIN
CAM + 0008h	TG Grab Range Start/End Pixel Configuration Register	CAM_GRABCOL
CAM + 000Ch	TG Grab Range Start/End Line Configuration Register	CAM_GRABROW
CAM + 0010h	Sensor Mode Configuration Register	CAM_CSMODE
CAM + 0018h	View Finder Mode Control Register	CAM_VFCON

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CAM + 001Ch	Camera Module Interrupt Enable Register	CAM_INTEN
CAM + 0020h	Camera Module Interrupt Status Register	CAM_INTSTA
CAM + 0024h	Camera Module Path Config Register	CAM_PATH
CAM + 0028h	Camera Module Input Address Register	CAM_INADDR
CAM + 002Ch	Camera Module Output Address Register	CAM_OUTADDR
CAM + 0030h	Preprocessing Control Register 1	CAM_CTRL1
CAM + 00B8h	Y Channel Configuration Register	CAM_YCHAN
CAM + 00BCh	UV Channel Configuration Register	CAM_UVCHAN
CAM + 00C0h	Space Convert YUV Register 1	CAM_SCONV1
CAM + 00C4h	Space Convert YUV Register 2	CAM_SCONV2
CAM + 0128h	Vertical Subsample Control Register	CAM_VSUB
CAM + 012Ch	Horizontal Subsample Control Register	CAM_HSUB
CAM + 0174h	Result Window Vertical Size Register	RWINV_SEL
CAM + 0178h	Result Window Horizontal Size Register	RWINH_SEL
CAM + 0180h	Camera Interface Debug Mode Control Register	CAM_DEBUG
CAM + 0184h	Camera Module Debug Information Write Out Destination Address	CAM_DSTADDR
CAM + 0188h	Camera Module Debug Information Last Transfer Destination Address	CAM_LSTADDR
CAM + 018Ch	Camera Module Frame Buffer Transfer Out Count Register	CAM_XFERCNT
CAM + 0190h	Sensor Test Module Configuration Register 1	CAM_MDLCFG1
CAM + 0194h	Sensor Test Module Configuration Register 2	CAM_MDLCFG2
CAM + 01D8h	Cam Reset Register	CAM_RESET
CAM + 01DCh	TG Status Register	TG_STATUS
CAM + 0248h	GMC Debug Register	CAM_GMCDEBUG
CAM + 0274h	Cam Version Register	CAM_VERSION

Table 62 Camera Interface Register Map

6.6.1.1 TG Register Definitions

0x8402_0000 TG Phase Counter Register CAM_PHSCNT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCEN		CLKEN	CLKPOL	CLKCNT				CLKRS				CLKFL			
Type	R/W		R/W	R/W	R/W				R/W				R/W			
Reset	0		0	0	1				0				1			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HVALID_EN	PXCLK_EN	PXCLK_INV	PXCLK_IN	CLKFL_POL			TGCLK_SEL	PIXCNT				DLATCH			
Type	R/W	R/W	R/W	R/W	R/W			R/W	R/W				R/W			

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Reset	0	0	0	0	0			0	1	1

PCEN TG phase counter enable control

CLKEN Enable sensor master clock (mclk) output to sensor. Driving current setting can be set from 0x80010700, there are two control bit, 0x80010700[8] : + 8mA, 0x80010700[9] : + 4mA. Fast slew rate can be set when 0x80010700[10] = 1.

CLKPOL Sensor master clock polarity control

CLKCNT Sensor master clock frequency divider control.
Sensor master clock will be 52Mhz/CLKCNT, where CLKCNT >=1.

CLKRS Sensor master clock rising edge control

CLKFL Sensor master clock falling edge control

HVALID_EN Sensor hvalid or href enable

PXCLK_EN Sensor clock input monitor.

PXCLK_INV Pixel clock inverse

PXCLK_IN Pixel clock sync enable. If sensor master based clock is 48 Mhz, PXCLK_IN must be enabled. Note that for frequency hopping mode,48Mhz PXCLK is selection, thus PXCLK_IN must be set.

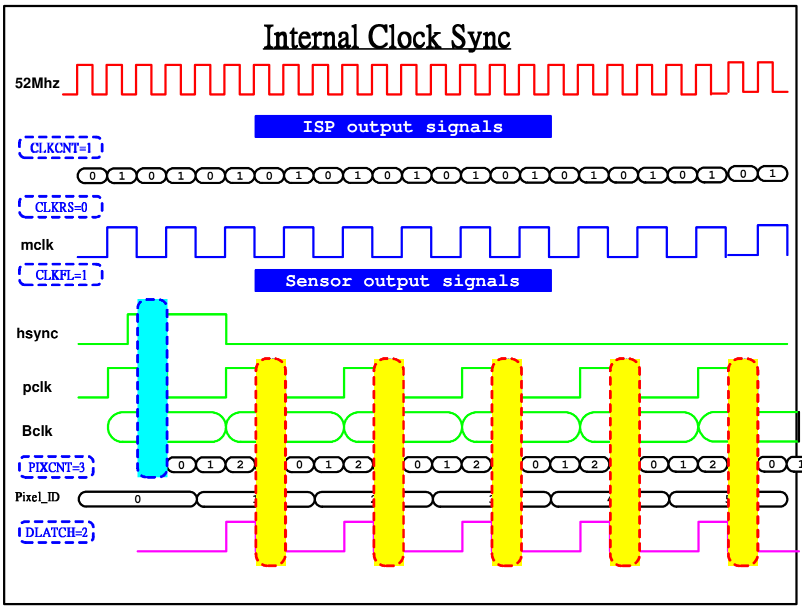
CLKFL_POL Sensor clock falling edge polarity

TGCLK_SEL Sensor master based clock selection (0: 52 Mhz, 1: 48 Mhz)

PIXCNT Sensor data latch frequency control

DLATCH Sensor data latch position control

Example waveform(CLKCNT=1,CLKRS=0,CLKFL=1,PIXCNT=3,DLATCH=2**)**



0x8402_0004 Sensor Size Configuration Register CAM_CAMWIN

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					PIXELS											

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Type					R/W											
Reset					fffh											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LINES											
Type					R/W											
Reset					fffh											

PIXEL Total input pixel number

LINE Total input line number

0x8402_0008 TG Grab Range Start/End Pixel Configuration Register CAM_GRABCOL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					START											
Type					R/W											
Reset					0											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					END											
Type					R/W											
Reset					0											

START Grab start pixel number

END Grab end pixel number

0x8402_000C TG Grab Range Start/End Line Configuration Register CAM_GRABROW

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					START											
Type					R/W											
Reset					0											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					END											
Type					R/W											
Reset					0											

START Grab start line number

END Grab end line number

0x8402_0010 Sensor Mode Configuration Register CAM_CSMODE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									VSPOL	HSPOL	PWRON	RST	AUTO			EN
Type									R/W	R/W	R/W	R/W	R/W			R/W
Reset									0	0	0	0	0			0

VSPOL Sensor Vsync input polarity

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HSPOL Sensor Hsync input polarity
AUTO Auto lock sensor input horizontal pixel numbers enable
EN Sensor process counter enable

0x8402_0018 View Finder Mode Control Register CAM_VFCON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AV_SYNC_SEL				AV_SYNC_LINENO[11:0]											
Type	R/W				R/W											
Reset	0				0											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SP_DELAY			SP_MODE	TAKE_PIC				FR_CON		
Type						R/W			R/W	R/W				R/W		
Reset						0			0	0				0		

AV_SYNC_SEL Av_sync start point selection
0 Start from AV_SYNC_LINENO
1 Start from vsync
AV_SYNC_LINENO Av_sync start point line counts
SP_DELAY Still Picture Mode delay
SP_MODE Still Picture Mode
TAKE_PIC Take Picture Request
FR_CON Frame Sampling Rate Control
000 Every frame is sampled
001 One frame is sampled every 2 frames
010 One frame is sampled every 3 frames
011 One frame is sampled every 4 frames
100 One frame is sampled every 5 frames
101 One frame is sampled every 6 frames
110 One frame is sampled every 7 frames
111 One frame is sampled every 8 frames

0x8402_001C Camera Module Interrupt Enable Register CAM_INTEN

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VSYNC_INT_SEL															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								AV_SYNC_INT	VSYNC_INT			ISPDONE	IDLE	GMCOVRUN	REZOVRUN	EXPDO
Type								R/W	R/W			R/W	R/W	R/W	R/W	R/W

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Reset								0	0			0	0	0	0	0

VSYNC_SEL Vsync interrupt selection

- **0** From Vsync Falling Edge
- **1** From Vsync Rising Edge

AV_SYNC_INT AV sync interrupt

VSYNC_INT Vsync interrupt

ISPDONE ISP done interrupt enable control

IDLE Returning idle state interrupt enable control

GMCOVRUN GMC port over run interrupt enable control

REZOVRUN Resizer over run interrupt enable control

EXPDO Exposure done interrupt enable control

0x8402_0020 Camera Module Interrupt Status Register CAM_INTSTA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								AV_SYNC_INT	VSYNC_INT			ISPDONE	IDLE	GMCOVRUN	REZOVRUN	EXPDO
Type								R/W	R			R	R	R	R	R
Reset								0	0			0	0	0	0	0

0x8402_0024h Camera Module Path Config Register CAM_PATH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTON	CNTMODE		WRITE_LEVEL				BAYER10_OUT	REZ_DISCONN	REZ_LPF_OFF	OUTPATH_TYPE					OUTPATH_EN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				R/W
Reset	0	0	0	0	0	0	1	0	0	0	0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			SWAP_Y	SWAP_CBCR	INDATA_FORMAT	INTYPE_SEL			INPATH_RATE							INPATH_SEL
Type			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				R/W
Reset			0	0	0	0	0	1	0	0	1	1				0

CNTON Enable Debug Mode Data Transfer Counter

CNTMODE Data Transfer Count Selection

- **00** sRGB count
- **01** YCbCr count

REZ_DISCONN Resizer disconnect enable

REZ_LPF_OFF Resizer low-Pass disable

WRITE_LEVEL Write FIFO threshold level

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BAYER10_OUT 10-bit Bayer Format output.
Outpath type should be set to 00.

OUTPATH_TYPE Outpath Type Select
- **00** Bayer Format
- **01** ISP output
- **02** RGB888 Format
- **03** RGB565 Format

OUTPATH_EN Enable Output to Memory

SWAP_Y YCbCr in Swap Y

SWAP_CBCR YCbCr in Swap Cb Cr

INDATA_FORMAT Sensor Input Data connection

INTYPE_SEL Input type selection
- **000** Reserved
- **001** YUV422 Format
  Default Input Format : **UYVY**
- **101** YCbCr422 Format
- **010** RGB

INPATH_RATE Input type rate control. Single word access is used when config to memory input mode. This setting config duration between two consecutive single access.

INPATH_SEL Input path selection
- **0** Sensor input
- **1** From memory

0x8402_0028 Camera Module Input Address Register CAM_INADDR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CAM_INADDR[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAM_INADDR[15:0]															
Type	R/W															
Reset	0															

CAM_INADDR Input memory address

0x8402_002C Camera Module Output Address Register CAM_OUTADDR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CAM_OUTADDR[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAM_OUTADDR[15:0]															
Type	R/W															
Reset	0															

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CAM_OUTADDR Output memory address

6.6.1.2 Color Process Register Definition

0x8402_00B8 Y Channel Configuration Register CAM_YCHAN

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										CONTRAST_GAIN						
Type										R/W						
Reset										40h						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIGN_BRIGHT_OFFSET	BRIGHT_OFFSET							VSUP_EN		UV_LP_EN	CSUP_EDGE_GAIN				
Type	R/W	R/W							R/W		R/W	R/W				
Reset	1	0							0		0	10h				

CONTRAST_GAIN Y channel contrast gain value
SIGN_BRIGHT_OFFSET Sign bit of Y channel brightness offset value
BRIGHT_OFFSET Y channel brightness offset value
VSUP_EN Vertical Edge color suppression enable
UV_LP_EN UV channel low pass enable
CSUP_EDGE_GAIN Chroma suppression edge gain value(1.3)

0x8402_00BC UV Channel Configuration Register CAM_UVCHAN

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	U11								V22							
Type	R/W								R/W							
Reset	20h								20h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIGN_U_OFFSET	U_OFFSET							SIGN_V_OFFSET	V_OFFSET						
Type	R/W	R/W							R/W	R/W						
Reset	0	0							0	0						

U11 Hue U channel operating value
V11 Hue V channel operating value
SIGN_U_OFFSET Sign bit of Hue U channel offset value
U_OFFSET Hue U channel offset value
SIGN_V_OFFSET Sign bit of Hue V channel offset value
V_OFFSET Hue V channel offset value

0x8402_00C0 Space Convert YUV Register 1 CAM_SCONV1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									Y_GAIN							
Type									R/W							
Reset									FFh							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	U_GAIN								V_GAIN							
Type	R/W								R/W							
Reset	91h								B8h							

Y_GAIN Space Convert Y channel gain value
U_GAIN Space Convert U channel gain value
V_GAIN Space Convert V channel gain value

0x8402_00C4 Space Convert YUV Register 2 CAM_SCONV2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									Y_OFFSET							
Type									R/W							
Reset									01h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	U_OFFSET								V_OFFSET							
Type	R/W								R/W							
Reset	80h								80h							

Y_OFFSET Space Convert Y channel offset value
U_OFFSET Space Convert U channel offset value
V_OFFSET Space Convert V channel offset value

0x8402_0128 Vertical Subsample Control Register CAM_VSUB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				V_SUB_EN	V_SUB_IN											
Type				R/W	R/W											
Reset				0	0											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					V_SUB_OUT											
Type					R/W											
Reset					0											

V_SUB_EN Vertical sub-sample enable
V_SUB_IN Source vertical size
V_SUB_OUT Sub-sample vertical size

0x8402_012c Horizontal Subsample Control Register CAM_HSUB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				H_SUB_EN	H_SUB_IN											
Type				R/W	R/W											
Reset				0	0											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					H_SUB_OUT											

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Type					R/W											
Reset					0											

H_SUB_EN Horizontal sub-sample enable
H_SUB_IN Source horizontal size
H_SUB_OUT Sub-sample horizontal size

0x8402_0174 Result Window Vertical Size Register RWINV_SEL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RWIN_EN	RWINV_START											
Type				R/W	R/W											
Reset				0h	0h											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RWINV_END											
Type					R/W											
Reset					0h											

RWIN_EN Result window enable
RWINV_START Result window vertical start line
RWINV_END Result window vertical end line

0x8402_0178 Result Window Horizontal Size Register RWINH_SEL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RWINH_START											
Type					R/W											
Reset					0h											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RWINH_END											
Type					R/W											
Reset					0h											

RWINH_START Result window horizontal start pixel
RWINH_END Result window horizontal end pixel

0x8402_0180 Camera Interface Debug Mode Control Register CAM_DEBUG

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

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0x8402_0184 Camera Module Debug Information Write Out Destination Address CAM_DSTADDR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DST_ADD[31:16]															
Type	R/W															
Reset	4000h															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DST_ADD[15:0]															
Type	R/W															
Reset	0000h															

DST_ADD Debug Information Write Output Destination Address

0x8402_0188 Camera Module Debug Information Last Transfer Destination Address CAM_LASTADDR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LAST_ADD[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LAST_ADD[15:0]															
Type	R/W															
Reset	0															

LAST_ADD Debug Information Last Transfer Destination Address

0x8402_018C Camera Module Frame Buffer Transfer Out Count Register CAM_XFERCNT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	XFER_COUNT [31:16]															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XFER_COUNT[15:0]															
Type	RO															
Reset	0															

XFER_COUNT Pixel Transfer Count per Frame

0x8402_0190 Sensor Test Model Configuration Register 1 CAM_MDLCFG1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VSYNC								IDLE_PIXEL_PER_LINE							
Type	R/W								R/W							
Reset	0								0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			LINECHG_EN	GRAY_LEVEL			ON	RST	STILL	PATTERN	PIXEL_SEL		CLK_DIV			

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Type			R/W	R/W			R/W	R/W	R/W	R/W	R/W		R/W			
Reset			0	0			0	0	0	0	0		0			

VSYNC VSYNC high duration in line unit(IDLE_PIXEL_PER_LINE + PIXEL)

IDLE_PIXEL_PER_LINE HSYNC low duration in pixel unit

LINECHG_EN Pattern 0 2 lines change mode enable

GRAY_LEVEL Sensor Model Gray Level Enable. When gray level is enable, increased gray level pattern will be generated.

ON Enable Sensor Model.

RST Reset Sensor Model

STILL Still picture Mode

PATTERN Sensor Model Test Pattern Selection

PIXEL_SEL Sensor Model output pixel selection.

- **00** All pixels
- **01** 01 pixel
- **10** 10 pixel
- **11** 00 and 11 pixels

CLK_DIV Pixel_Clock/System_Clock Ratio

0x8402_0194 Sensor Test Model Configuration Register 2 CAM_MDLCFG2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LINE										
Type						R/W										
Reset						0										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						PIXEL										
Type						R/W										
Reset						0										

LINE Sensor Model Line Number

PIXEL Sensor Model Pixel Number (HSYNC high duration in pixel unit)

0x8402_01D8 CAM RESET Register CAM_RESET

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												TG_STATUS				
Type												R				
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISP_FRAME_COUNT[7:0]															ISP_RESET
Type	RW															RW
Reset	0															0

ISP_FRAME_COUNT ISP frame counter

ISP_RESET ISP reset

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0x8402_01DC TG STATUS Register TG_STATUS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				SYN_ VFON	LINE_COUNT[11:0]											
Type				R	R											
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PIXEL_COUNT[11:0]											
Type					R											
Reset																

SYN_VFON TG view finder status
LINE_COUNT TG line counter
PIXEL_COUNT TG pixel counter

0x8402_0248 CAM GMC DEBUG Register CAM_DEBUG

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

0x8402_0274 CAM VERSION Register CAM_VERSION

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	YEAR[16:0]															
Type	R															
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MONTH[15:0]								DATE[15:0]							
Type	R								R							
Reset																

YEAR Year ASCII
MONTH Month ASCII
DATE Date ASCII

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7 Audio Front-End

7.1 General Description

The audio front-end essentially consists of voice and audio data paths. **Figure 76** shows the block diagram of the audio front-end. All voice band data paths comply with the GSM 03.50 specification. Mono hands-free audio or external FM radio playback paths are also provided. The audio stereo path facilitates CD-quality playback, external FM radio, and voice playback through a headset.

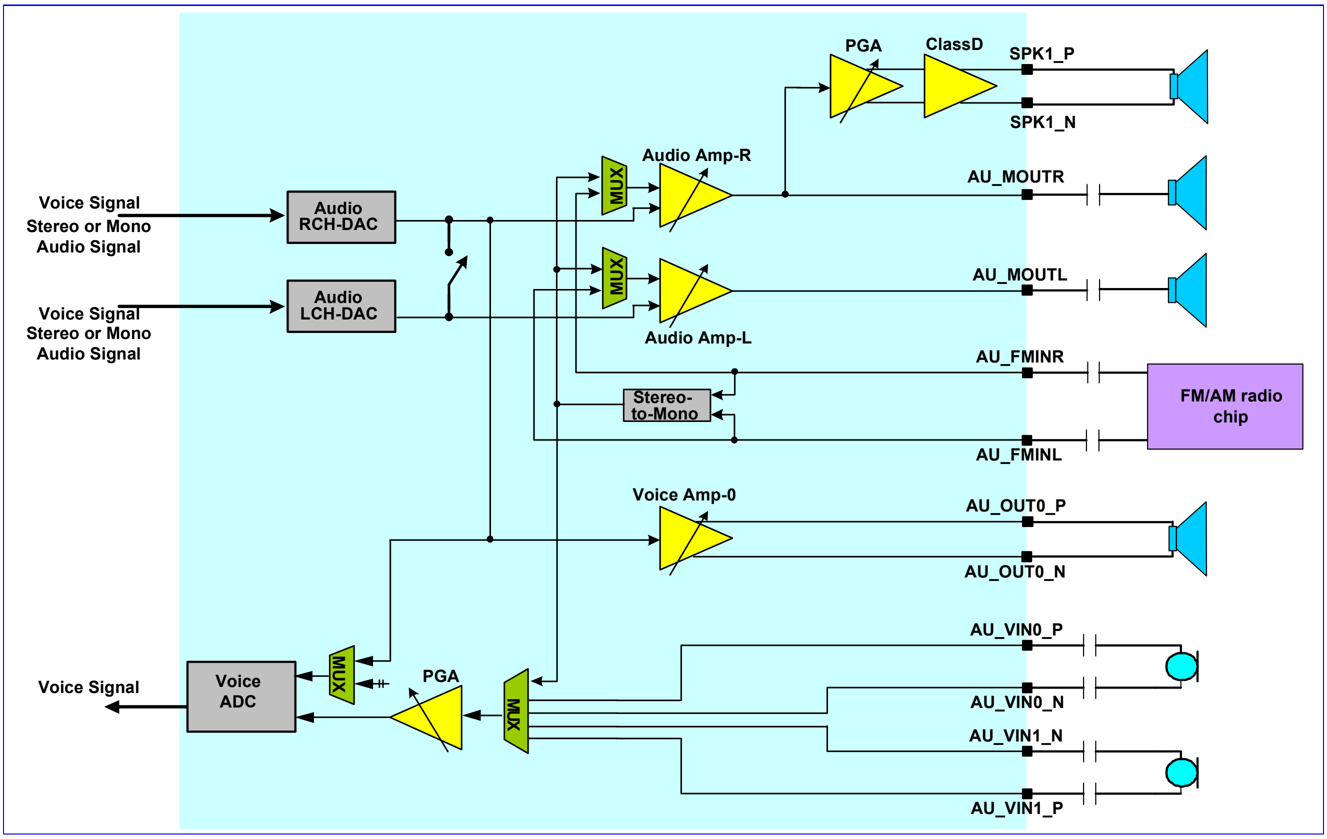

Figure 76 Block diagram of audio front end

Figure 77 shows the digital circuits block diagram of the audio front-end. The APB register block is an APB peripheral that stores settings from the MCU. The DSP audio port (DAP) block interfaces with the DSP for control and data communications. The digital filter block performs filter operations for voice band and audio band signal processing. The Digital Audio Interface (DAI) block communicates with the System Simulator for FTA or external Bluetooth modules.

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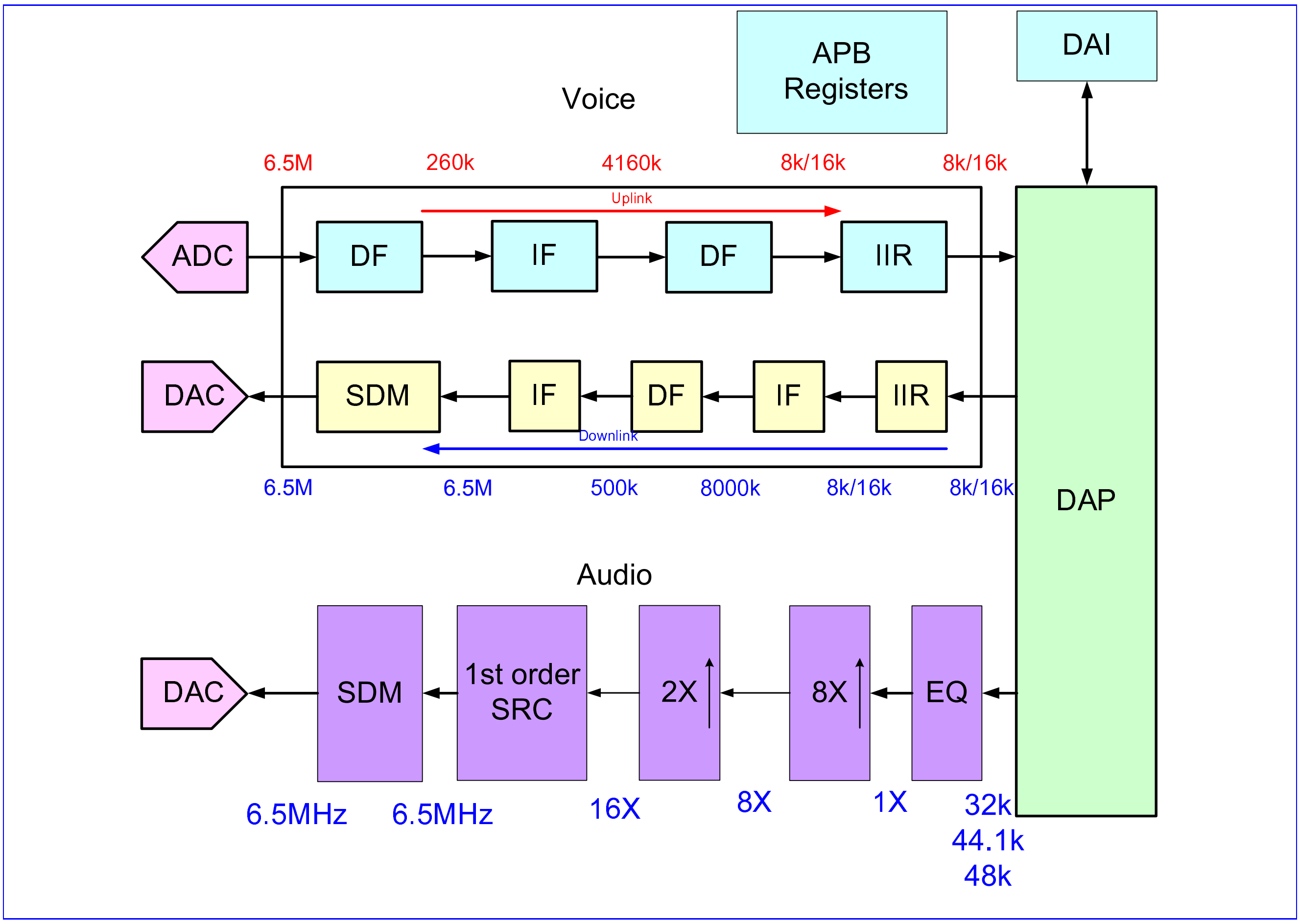

Figure 77 Block diagram of digital circuit of audio front end

To communicate with the external Bluetooth module, the master-mode PCM interface and master-mode I2S/EIAJ interface are supported. The clock of PCM interface is 256 kHz while the frame sync is 8 kHz. Both long sync and short sync interfaces are supported. The PCM interface can transmit 16-bit stereo or 32-bit mono 8 kHz sampling rate voice signal. **Figure 78** shows the timing diagram of the PCM interface. Note that the serial data changes when the clock is rising and is latched when the clock is falling.

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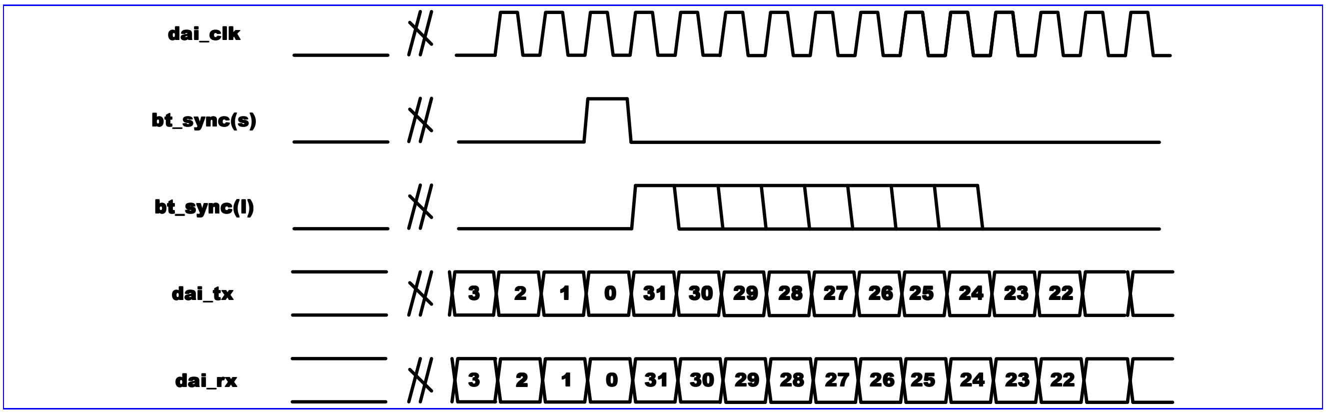

Figure 78 Timing diagram of Bluetooth application

I2S/EIAJ interface is designed to transmit high quality audio data. **Figure 78** and **Figure 79** illustrate the timing diagram of the two types of interfaces. I2S/EIAJ can support 32 kHz, 44.1 kHz, and 48 kHz sampling rate audio signals. The clock frequency of I2S/EIAJ can be 32×(sampling frequency), or 64×(sampling frequency). For example, to transmit a 44.1 kHz CD-quality music, the clock frequency should be 32 × 44.1 kHz = 1.4112 MHz or 64 × 44.1 kHz = 2.8224 MHz.

I2S/EIAJ interface is not only used for Bluetooth module, but also for external DAC components. Audio data can easily be sent to the external DAC through the I2S/EIAJ interface.

In this document, the I2S/EIAJ interface is referred to as EDI (External DAC Interface).

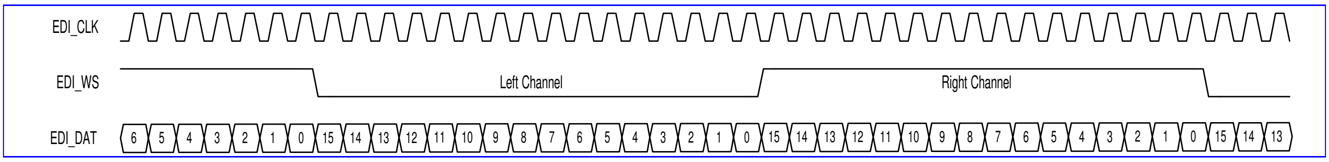

Figure 79 EDI Format 1: EIAJ (FMT = 0).

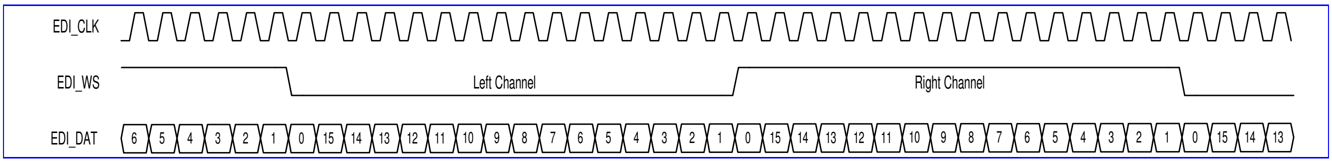

Figure 80 EDI Format 2: I^2S (FMT = 1).

7.1.1 DAI, PCM and EDI Pin Sharing

DAI, PCM, and EDI interfaces share the same pins. The pin mapping is listed in **Table 63**.

PIN NAME	DAI	PCM	EDI
DAI_CLK (OUTPUT)	DAI_CLK	PCM_CLK	EDI_CLK

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DAI_TX (OUTPUT)	DAI_TX	PCM_OUT	EDI_DAT
DAI_RX (INPUT)	DAI_RX	PCM_IN	
BT_SYNC (OUTPUT)	-	PCM_SYNC	EDI_WS

Table 63 Pin mapping of DAI, PCM, and EDI interfaces.

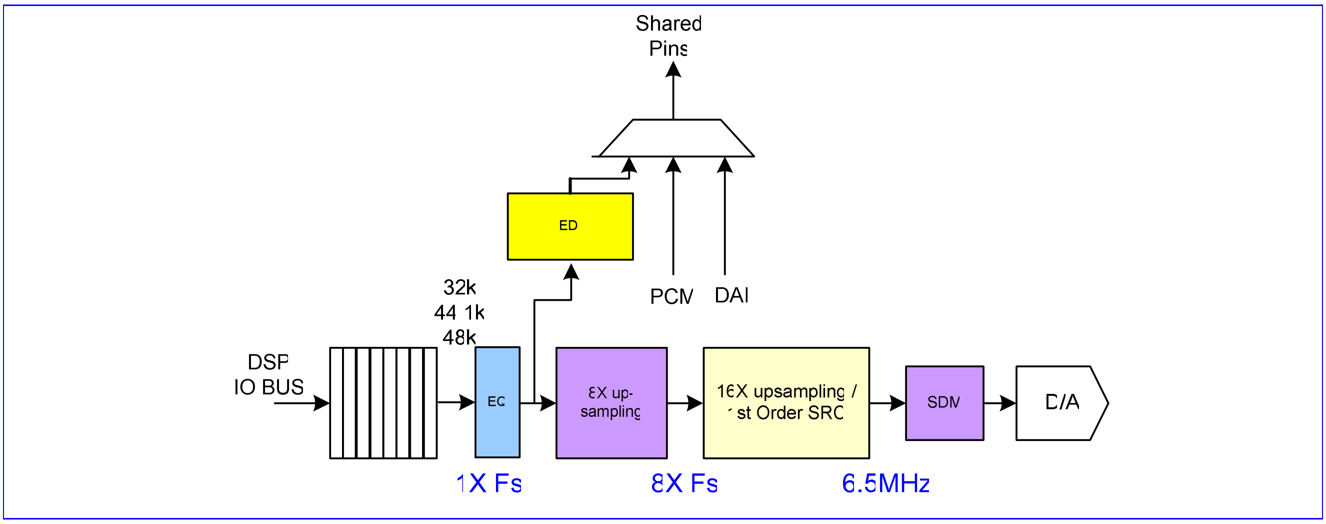

Figure 81 DAI, PCM, EDI interfaces

7.2 Register Definitions

MCU APB bus registers in audio front-end are listed as follows.

0x820F_0000 AFE Voice MCU Control Register AFE_VMCU_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VAFE ON
Type																R/W
Reset																0

MCU sets this register to start AFE voice operation. A synchronous reset signal is issued, then periodical interrupts of 8-KHz frequency are issued. Clearing this register stops the interrupt generation.

VAFEON Turn on audio front-end operations.

0 off

1 on

0x820F_000C AFE Voice MCU Control Register 1 AFE_VMCU_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name						VIDWA	VMODE4K	VAFECLR_EN	VRSDON	VDL_IIRMODE		VUL_IIRMODE		VDLDITH_VAL		VDLDITH_ON
Type						R/W	R/W	R/W	R/W	R/W		R/W		R/W		R/W
Reset						1	0	0	1	00		00		00		0

Set this register for consistency of analog circuit setting. Suggested value is 281h.

VIDWA IDWA Enable
- **0** disable IDWA
- **1** enable IDWA

VMODE4K DSP data mode selection
- **0** 8k mode
- **1** 4k mode

VAFECLR_EN Enable signal to reset voice downlink buffer or not while VAFE is powered down.
- **0** NO reset voice downlink buffer while VAFE is powered down
- **1** Reset voice downlink buffer while VAFE is powered down

VDL_IIRMODE Voice downlink IIR coefficients set selection
- **00** 4k : 90Hz, 8k: 180Hz.
- **01** 4k : 160Hz, 8k: 320Hz.
- **10** 4k : 200Hz, 8k: 400Hz
- **11** 4k : 320Hz, 8k: 640Hz

VRSDON SDM level for VBITX
- **0** 2-level
- **1** 3-level

VUL_IIRMODE Voice uplink IIR coefficients set selection
- **00** 4k : 90Hz, 8k: 180Hz.
- **01** 4k : 160Hz, 8k: 320Hz.
- **10** 4k : 200Hz, 8k: 400Hz
- **11** 4k : 320Hz, 8k: 640Hz

VDITHVAL Voice downlink dither scaling setting
- **00** 1/4x
- **01** 1/2x
- **10** 1x
- **11** 2x

VDITHON Turn on the voice downlink dither function.
- **0** Turn off
- **1** Turn on

0x820F_0010 AFE Voice MCU Control Register 2 AFE_VMCU_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							DWL_OUT_GAIN		DWL_IN_GAIN		VSDM_GAIN					

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Type							R/W		R/W		R/W					
Reset							00		00		100000					

Set this register for consistency of analog circuit setting. Suggested value is 16h.

DWL_OUT_GAIN Gain setting at Gain Stage input.

- **00** 1X
- **01** 2X
- **10** 4X
- **11** 1X

DWL_IN_GAIN Gain setting at 8k/16k input.

- **00** 1X
- **01** 1/2X
- **10** 1/4X
- **11** -3dB

VSDM_GAIN Gain settings at Voice SDM input.

- **000000** 0/32
- **000001** 1/32
- **000010** 2/32
- **000011** 3/32
- ●
- ●
- ●
- **100000** 32/32
- **111111** 63/32

0x820F_0014 AFE Voice DAI Bluetooth Control Register AFE_VDB_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									VDAIBT_CLR_EN	EDION	VDAION	VBTON	VBTSYNC	VBTSLEN		
Type									R/W	RW	R/W	R/W	R/W	R/W		
Reset									0	0	0	0	0	000		

Set this register for DAI test mode and Bluetooth application.

DAIBT_CLR_EN Enable signal to reset DAIBT buffer or not while VAFE is powered down.

- **0** NO reset DAIBT buffer while VAFE is powered down
- **1** Reset DAIBT buffer while VAFE is powered down

EDION EDI signals are selected as the output of DAI, PCM, EDI shared interface.

- **0** EDI is not selected. A dedicated EDI interface can be enabled by programming the GPIO selection. Please refer to GPIO section for details.
- **1** EDI is selected. VDAION and VBTON are not set.

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VDAION Turn on the DAI function.

VBTON Turn on the Bluetooth PCM function.

VBTSYNC Bluetooth PCM frame sync type

0: short
1: long

VBTSLEN Bluetooth PCM long frame sync length = VBTSLEN+1

0x820F_0018 AFE Voice Look-Back mode Control Register AFE_VLB_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											VDSPBYPASS	VDSPCSMODE	VBYPASSIIR	VDAPINMODE	VINTINMODE	VDECINMODE
Type											R/W	R/W	R/W	R/W	R/W	R/W
Reset											0	0	0	0	0	0

Set this register for AFE voice digital circuit configuration control. Several loop back modes are implemented for test purposes. Default values correspond to the normal function mode.

VDSPBYPASS Loopback data won't be gated by VDSPRDY.

0 Normal Mode
1 Bypass DSP loopback mode

VDSPCSMODE DSP COSIM only, to align DATA.

0 Normal mode
1 DSP COSIM mode

VBYPASSIIR Bypass IIR filter

0 Normal mode
1 Bypass

VDAPINMODE DSP audio port input mode control

0 Normal mode
1 Loop back mode

VINTINMODE interpolator input mode control

0 Normal mode
1 Loop back mode

VDECINMODE decimator input mode control

0 Normal mode
1 Loop back mode

0x820F_0020 AFE Audio MCU Control Register 0 AFE_AMCU_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																AAFEON

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Type																R/W
Reset																0

MCU sets this register to start AFE audio operation. A synchronous reset signal is issued, then periodical interrupts of 1/6 sampling frequency are issued. Clearing this register stops the interrupt generation.

AAFEON Turn on audio front-end operations.

0 off

1 on

0x820F_0024 AFE Audio Control Register 1 AFE_AMCU_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASDMCK_PHASE	MONO	SEL_IDWA2	SEL_IDWA	BYPASS		SDM_MODE	ADITHON	ADITHVAL		ARAMPSP		AMUTER	AMUTEL	AFS	
Type	R/W	R/W	R/W	R/W	RW		R/W	R/W	R/W		R/W		R/W	R/W	R/W	
Reset	0	0	0	1	00		0	1	10		00		0	0	00	

MCU sets this register to inform hardware of the sampling frequency of audio being played back.

ASDMCK_PHASE Phase of Audio SDM Clock. Please set to 0.

SEL_IDWA2 IDWA function selection.

0 Disable RMDWA

1 Enable RMDWA

SEL_IDWA IDWA function selection.

0 Disable IDWA

1 Enable IDWA

MONO Mono mode select. AFE HW will do (left + right) / 2 operation to the audio sample pair. Thus both right/left channel DAC will have the same inputs.

0 Disable mono mode.

1 Enable mono mode.

BYPASS To bypass part of the audio hardware path.

00 No bypass. The input data rate is 1/4 sampling frequency. For example, if the sampling frequency is 32 KHz, then the input data rate is 8 KHz.

01 Bypass the first stage of interpolation. The input data rate is 1/2 the sampling frequency.

10 Bypass two stages of interpolation. The input data rate is the same as the sampling frequency.

11 Bypass two stages of interpolation and EQ filter. The input data rate is the same as the sampling frequency.

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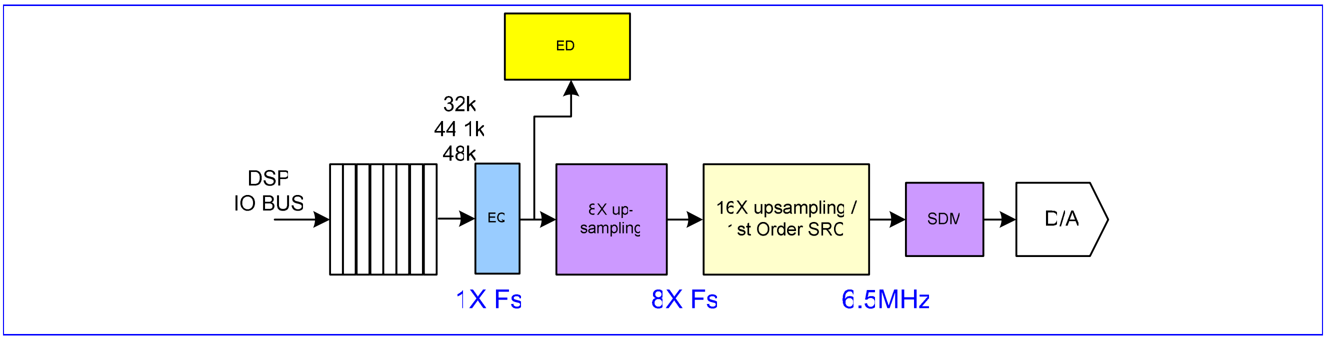

Figure 82 Block diagram of the audio path.

SDM_MODE SDM mode control

- **0** zero extension.
- **1** sign extension.

ADITHON Open dither for SDM

- **0** off. .
- **1** on.

ADITHVAL Dither strength

- **00** 1/2x. .
- **01** 1x.
- **10** 2x. .
- **11** 4x.

ARAMPSP ramp up/down speed selection

- **00** 8, 4096/AFS
- **01** 16, 2048/AFS
- **10** 24, 1024/AFS
- **11** 32, 512/AFS

AMUTER Mute the audio R-channel, with a soft ramp up/down.

- **0** no mute
- **1** mute

AMUTEL Mute the audio L-channel, with a soft ramp up/down.

- **0** no mute
- **1** mute

AFS Sampling frequency setting.

- **00** 32-KHz
- **01** 44.1-KHz
- **10** 48-KHz
- **11** reserved

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0x820F_002C AFE Audio Control Register 2 AFE_AMCU_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AV_MUX1	AV_MUX	SDMSEL	EDI_SEL	ASDM_GAIN					
Type							R/W	R/W	R/W	R/W	R/W					
Reset							0	0	0	0	100000					

Set this register for consistency of analog circuit setting. Suggested value is 10h.

AV_MUX Audio DAC input mux.

- **0** Audio data to audio DAC
- **1** Voice data to audio DAC.

AV_MUX 1 Audio DAC input mux.

- **0** Speech data output to Rch only
- **1** Speech data output to Rch/Lch..

SDMSEL SDM selection.

- **0** 2nd order SDM.
- **1** 3rd order SDM.

EDI_SEL Feed EDI input data to Audio filter directly.

- **0** Audio Data come from DSP/Sine table.
- **1** Audio Data come from EDI input.

ASDM_GAIN Gain settings at Audio SDM input (0/32 → 63/32).

- **000000** 0/32
- **000001** 1/32
- **000010** 2/32
- **000011** 3/32
- ●
- ●
- ●
- **100000** 32/32
- **111111** 63/32

0x820F_0028 AFE EDI Control Register AFE_EDI_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					I2S_MODE			DIR		WCYCLE					FMT	EN
Type					R/W			R/W		R/W					R/W	R/W
Reset					00			0		01111					0	0

This register is used to control the EDI

I2S_MODE I2S data rate selection

- **01** 1/2X AFS
- **10** 1/4X AFS

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00 1X AFS

11 1X AFS

EN Enable EDI. When EDI is disabled, EDI_DAT and EDI_WS hold low.

0 disable EDI.

1 enable EDI.

FMT EDI format

0 EIAJ

1 I2S

WCYCLE Clock cycle count in a word. Cycle count = WCYCLE + 1, and WCYCLE can be 15 or 31 only. Any other values result in an unpredictable error.

15 Cycle count is 16.

31 Cycle count is 32.

DIR Serial data bit direction

0 Output mode. Audio data is fed out to the external device.

1 Input mode or recording mode. By this recording mechanism, DSP can do some post processing or voice memos.

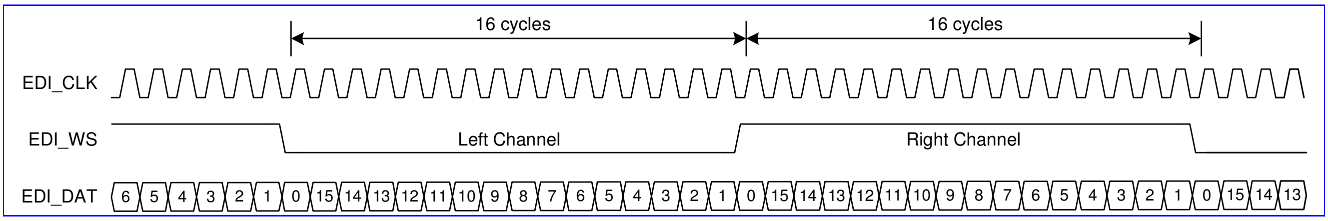

Figure 83 Cycle count is 16 for I2S format.

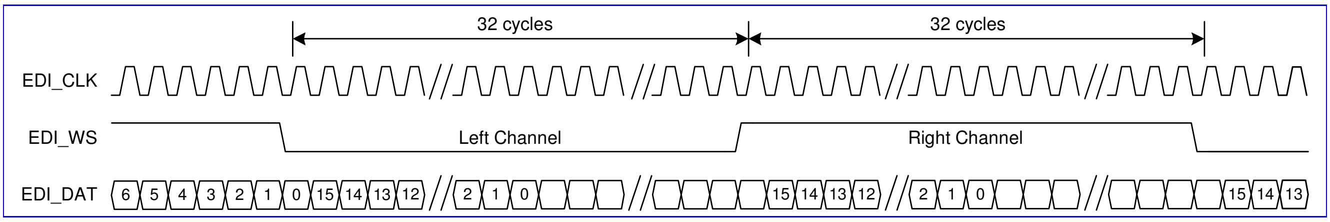

Figure 84 Cycle count is 32 for I2S format.

0x820F_0030 Audio/Voice DAC SineWave Generator AFE_DAC_TEST

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VON	AON	MUTE			AMP_DIV			FREQ_DIV							
Type	R/W	R/W	R/W			R/W			R/W							
Reset	0	0	0			111			0000_0001							

This register is only for analog design verification on audio/voice DACs.

VON Makes voice DAC output the test sine wave.

0 Voice DAC inputs are normal voice samples

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1 Voice DAC inputs are sine waves

AON Makes audio DAC output the test sine wave.

- **0** Audio DAC inputs are normal audio samples
- **1** Audio DAC inputs are sine waves

MUTE Mute switch.

- **0** Turn on the sine wave output in this test mode.
- **1** Mute the sine wave output.

AMP_DIV Amplitude setting.

- **111** full scale
- **110** 1/2 full scale
- **101** 1/4 full scale
- **100** 1/8 full scale

FREQ_DIV Frequency setting, 1X ~ 15X (voice), 1X ~ 31X (Audio).

0x820F_0034 Audio/Voice Interactive Mode Setting AFE_VAM_SET

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	A2V													PER_VAL		
Type	R/W													R/W		
Reset	0													101		

A2V Redirect audio interrupt to voice interrupt. In other words, replace voice interrupt by audio interrupt.

- **0** [voice interrupt / audio interrupt] → [voice / audio]
- **1** [audio interrupt / no interrupt] → [voice / audio]

PER_VAL Counter reset value for audio interrupt generation period setting. For example, by default, the setting = 5 causes interrupt per 6 L/R samples. Changing this value can change the rate of audio interrupt.

0x820F_0040~ 0x820F_00F0 AFE Audio Equalizer Filter Coefficient Register AFE_EQCOEF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	A															
Type	WO															

Audio front-end provides a 45-tap equalizer filter. The filter is shown below.

DO = (A44 X DI44 + A43 X DI43 … + A1 X DI1 + A0 X DI0)/32768.

DIn is the input data, and An is the coefficient of the filter, which is a 16-bit 2's complement signed integer. DI0 is the last input data.

The coefficient cannot be programmed when the audio path is enabled, or unpredictable noise may be generated. If coefficient programming is necessary while the audio path is enabled, the audio path must be muted during programming. After programming is complete, the audio path is not to be resumed (unmated) for 100 sampling periods.

A Coefficient of the filter.

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Address	Coefficient	Address	Coefficient	Address	Coefficient
0x820F_0040	A0	0x820F_007C	A15	0x820F_00B8	A30
0x820F_0044	A1	0x820F_0080	A16	0x820F_00BC	A31
0x820F_0048	A2	0x820F_0084	A17	0x820F_00C0	A32
0x820F_004C	A3	0x820F_0088	A18	0x820F_00C4	A33
0x820F_0050	A4	0x820F_008C	A19	0x820F_00C8	A34
0x820F_0054	A5	0x820F_0090	A20	0x820F_00CC	A35
0x820F_0058	A6	0x820F_0094	A21	0x820F_00D0	A36
0x820F_005C	A7	0x820F_0098	A22	0x820F_00D4	A37
0x820F_0060	A8	0x820F_009C	A23	0x820F_00D8	A38
0x820F_0064	A9	0x820F_00A0	A24	0x820F_00DC	A39
0x820F_0068	A10	0x820F_00A4	A25	0x820F_00E0	A40
0x820F_006C	A11	0x820F_00A8	A26	0x820F_00E4	A41
0x820F_0070	A12	0x820F_00Ac	A27	0x820F_00E8	A42
0x820F_0074	A13	0x820F_00B0	A28	0x820F_00EC	A43
0x820F_0078	A14	0x820F_00B4	A29	0x820F_00F0	A44

Table 64

0x820F_0100 AFE AGC Control Register 0 AFE_VAGC_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MINPGAGAIN						PGAGAIN						FRFLG	RATKFLG	SATKFLG	AGCON
Type	R/W						R/W						R/W	R/W	R/W	R/W
Reset	001010						101000						0	1	1	1

This register sets the control signals for AGC.

AGCON Switch of the AGC
- **0** Off
- **1** On

SATKFLG Sample Attack Flag
- **0** off
- **1** on

RATKFLG RMS Attack Flag
- **0** off
- **1** on

FRFLG Free Release Flag
- **0** off
- **1** on

PGAGAIN PGA gain settings (from -20dB to 43 dB), it is also the maximum PGA gain settings while AGC is on.
- **000000** -20dB

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000001 -19dB

●

●

●

111110 42dB

111111 43dB

MINPGAGAIN minima PGA gain settings (from -20 to 43 dB). PGA gain is always larger than MINPGAGAIN.

000000 -20dB

000001 -19dB

●

●

●

111110 42dB

111111 43dB

0x820F_0104 AFE AGC Control Register 1 AFE_VAGC_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			VAGC_SEL	VAGC_CTRL	ECNTRRLZS				ECNTRRLZF				ECNTRATK			
Type			R/W	R/W	R/W				R/W				R/W			
Reset			1	0	1100				1100				1000			

This register sets the control signals for AGC.

VAGC_SEL Selection of AGC output.

0 bypass AGC.

1 AGC compensation on.

VAGC_CTRL Selection the AGC gain control master.

0 Control by AFE.

1 Control by DSP.

ECNTRATK Attack counter, control attack speed.(unit: N samples@52kHz). Attach will be triggered if N samples amplitude exceed attack threshold (ENTHDATK)

0 always attack, please don't set to this values.

1~15 N=1~15

ECNTRRLZF Fast release counter, control fast release speed.(unit: N samples@52kHz). Release will be triggered if N samples amplitude lower than slow release threshold (ENTHDRLS)

0 1

1 3

2 7

3 15

4 31

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5 63
6 127
7 255
8 511
9 1023
10 2043
11 4095
12 8191
13 16383
14 32767
15 65535

ECNTRRLZS Slow release counter, control slow release speed.(unit: N samples@52kHz). Release will be triggered if N samples amplitude lower than hysteresis threshold (ENTHDHYS)

0 1
1 3
2 7
3 15
4 31
5 63
6 127
7 255
8 511
9 1023
10 2043
11 4095
12 8191
13 16383
14 32767
15 65535

0x820F_0108 AFE AGC Control Register 2 AFE_VAGC_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERMSFBATTF				ERMSFBATTR				ERMSFBF				ERMSFBR			
Type	R/W				R/W				R/W				R/W			
Reset	1010				0100				1011				0101			

This register sets the control signals for AGC.

ERMSFBR RMS rising factor. The larger the number; the slower the signal energy estimation.

0 1x RMS power estimation.
1 2x RMS power estimation.
2 4x RMS power estimation.

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3 8x RMS power estimation.

●
●
●

14 16384x RMS power estimation.
15 32768x RMS power estimation.

ERMSFBF RMS falling factor. The larger the number; the slower the signal energy estimation.

0 1x RMS power estimation.
1 2x RMS power estimation.
2 4x RMS power estimation.
3 8x RMS power estimation.

●
●
●

14 16384x RMS power estimation.
15 32768x RMS power estimation.

ERMSFBATTR RMS for Attack rising factor. The larger the number; the slower the signal energy estimation.

0 1x RMS power estimation.
1 2x RMS power estimation.
2 4x RMS power estimation.
3 8x RMS power estimation.

●
●
●

14 16384x RMS power estimation.
15 32768x RMS power estimation.

ERMSFBATTF RMS for Attack falling factor. The larger the number; the slower the signal energy estimation.

0 1x RMS power estimation.
1 2x RMS power estimation.
2 4x RMS power estimation.
3 8x RMS power estimation.

●
●
●

14 16384x RMS power estimation.
15 32768x RMS power estimation.

0x820F_010C AFE AGC Control Register 3 AFE_VAGC_CON3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	EGAINCOMP_CSS	EGAINCOMP_CSM	EGAINCOMP_CSF	EGAINCOMP_FC_THD	EGAINCOMP_LOWER	EGAINCOMP_UPPER
Type	R/W	R/W	R/W	R/W	R/W	R/W
Reset	001	011	011	101	01	01

This register sets the control signals for AGC.

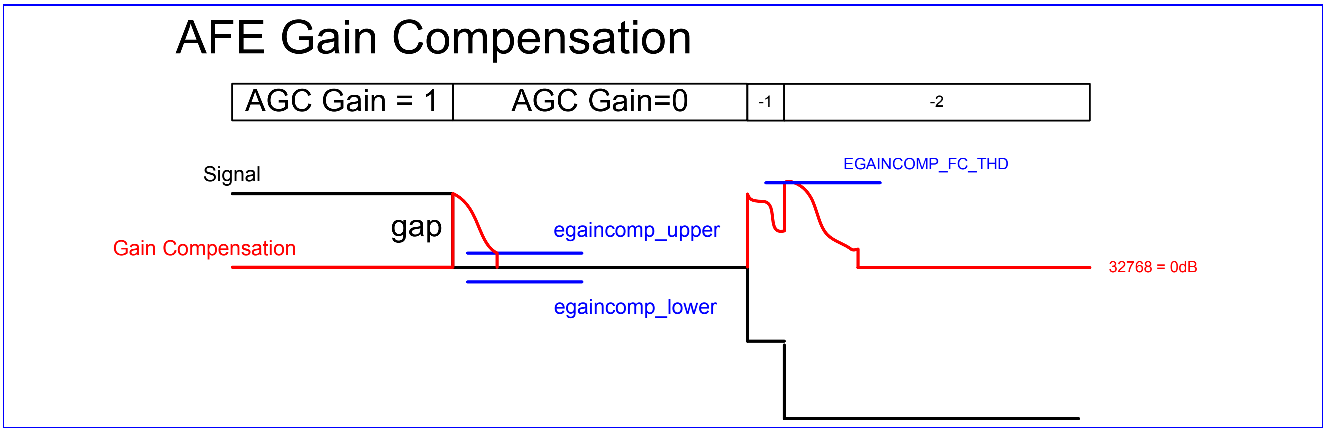

Figure 85 Gain Compensation procedures.

EGAINCOMP_UPPER Gain compensation upper threshold, 32768 = 0dB (**Figure 85**)

00 33095
01 33423
10 33751
11 34078

EGAINCOMP_LOWER Gain compensation lower threshold, 32768 = 0dB (**Figure 85**)

00 32440
01 32112
10 31784
11 31457

EGAINCOMP_FC_THD Gain compensation convergence threshold (**Figure 85**).

000 34406
001 36044
010 37683
011 39321
100 40960
101 42598
110 44236
111 45875

EGAINCOMP_FC_CSF Gain compensation fast converge speed. (While compensation gain is 0.3dB far from 32768, the convergence speed is fast)

000 31948 (8X)

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001 31129 (7X)
010 30310 (6X)
011 29491 (5X)
100 28672 (4X)
101 27852 (3X)
110 27033 (2X)
111 26214 (1X)

EGAINCOMP_FC_CSM Gain compensation converge speed middle. (While compensation gain is 0.15dB ~ 0.3dB from 32768, the convergence speed is middle)

000 32686 (8X)
001 32604 (7X)
010 32552 (6X)
011 32440 (5X)
100 32358 (4X)
101 32276 (3X)
110 32194 (2X)
111 32112 (1X)

EGAINCOMP_FC_CSS Gain compensation converge speed slow. (While compensation gain is inside 0.15dB from 32768, the convergence speed is slow)

000 32751 (8X)
001 32735 (7X)
010 32718 (6X)
011 32702 (5X)
100 32686 (4X)
101 32669 (3X)
110 32653 (2X)
111 32636 (1X)

0x820F_0110 AFE AGC Control Register 4 AFE_VAGC_CON4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENTHDATKRMS						ENTHDATK						ESRELWINWIDTH1			
Type	R/W						R/W						R/W			
Reset	000100						000001						1000			

This register sets the control signals for AGC.

ESRELWINWIDTH1 speech release window width for strong VAD

0 10 @ 52kHz samples
1 20 @ 52kHz samples
2 40 @ 52kHz samples
3 80 @ 52kHz samples
4 160 @ 52kHz samples

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5 325 @ 52kHz samples
6 650 @ 52kHz samples
7 1300 @ 52kHz samples
8 2600 @ 52kHz samples
9 5200 @ 52kHz samples
10 10000 @ 52kHz samples
11 15000 @ 52kHz samples
12 20000 @ 52kHz samples
13 25000 @ 52kHz samples
14 30000 @ 52kHz samples
15 32767 @ 52kHz samples

ENTHDATK Attack threshold

[0~63] is map to [-63~0]dB FS

ENTHDATKRMS RMS attack threshold

[0~63] is map to [-63~0]dB FS

0x820F_0114 AFE AGC Control Register 5 AFE_VAGC_CON5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENTHDRLS						ENTHDHYS						ESRELWINWIDTH2			
Type	R/W						R/W						R/W			
Reset	001101						000111						1000			

This register sets the control signals for AGC.

ESRELWINWIDTH2 speech release window width for weak VAD

0 10 @ 52kHz samples
1 20 @ 52kHz samples
2 40 @ 52kHz samples
3 80 @ 52kHz samples
4 160 @ 52kHz samples
5 325 @ 52kHz samples
6 650 @ 52kHz samples
7 1300 @ 52kHz samples
8 2600 @ 52kHz samples
9 5200 @ 52kHz samples
10 10000 @ 52kHz samples
11 15000 @ 52kHz samples
12 20000 @ 52kHz samples
13 25000 @ 52kHz samples
14 30000 @ 52kHz samples
15 32767 @ 52kHz samples

ENTHDHYS Hysteresis threshold

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[0~63] is map to [-63~0]dB FS

ENTHDRLS Slow release threshold

[0~63] is map to [-63~0]dB FS

0x820F_0118 AFE AGC Control Register 6 AFE_VAGC_CON6

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EPATTLIMITER				PATTRELD				NATKFLG	PATTRELFLG	ENTHDNOZ					
Type	R/W				R/W				R/W	R/W	R/W					
Reset	0100				0000				1	1	111101					

This register sets the control signals for AGC.

ENTHDNOZ Idle threshold

[0~63] is map to [-63~0]dB FS

PATTRELFLG post attack/release flag

0 off

1 on

NATKFLG noise adaptive attenuation enable attack flag

0 off

1 on

PATTRELD Post attack/release latency

0~15 is map to 0~15 sample @260kHz sampling rate

EPATTLIMITER Post attack limiter

[0,15] is map to [0,-7.5dBFs], the spacing is 0.5dB

7.3 DSP Register Definitions

0x640 AFE Voice Uplink Data Register 0 AFE_VUL_DAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VUL_DAT0															
Type	RO															
Reset	0															

Voice band uplink transmission data register 0. The content of this register is updated by uplink digital filter outputs. This register is read by DSP in an 8K ISR.

0x641 AFE Voice Uplink Data Register 1 AFE_VUL_DAT1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VUL_DAT1															
Type	RO															
Reset	0															

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Voice band uplink transmission data register 1. The content of this register is updated by uplink digital filter outputs. This register is read by DSP in an 8K ISR if VBYPASSIIR of AFE_LB_CON is set.

0x642 AFE Voice Downlink Data Register 0 AFE_VDL_DAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDL_DAT0															
Type	WO															
Reset	0															

Voice band downlink receiving data register 0. This register is written by DSP in an 8K ISR. The content of this register is used as downlink digital filter inputs.

0x643 AFE Voice Downlink Data Register 1 AFE_VDL_DAT1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDL_DAT1															
Type	WO															
Reset	0															

Voice band downlink receiving data register 1. This register is written by DSP in an 8K ISR if VBYPASSIIR of AFE_VLB_CON is set. The content of this register is used as downlink digital filter inputs.

0x644 AFE Voice DAI Bluetooth TX Data Register 0 AFE_VDBTX_DAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDBTX_DAT0															
Type	WO															
Reset	0															

DAI Bluetooth transmission data register 0. This register is written by DSP in an 8K ISR if the Bluetooth function is turned on. The content of this register is shifted out to the Bluetooth interface.

0x645 AFE Voice DAI Bluetooth TX Data Register 1 AFE_VDBTX_DAT1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDBTX_DAT 1															
Type	WO															
Reset	0															

DAI Bluetooth transmission data register 1. This register is written by DSP in an 8K ISR if the corresponding DAI test is set or the Bluetooth function is turned on. The content of this register is shifted out to the SS or Bluetooth interface.

0x646 AFE Voice DAI Bluetooth RX Data Register 0 AFE_VDBRX_DAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDBRX_DAT 0															
Type	RO															
Reset	0															

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DAI Bluetooth receiving data register 0. This register is read by DSP in an 8K ISR if the Bluetooth function is turned on. The content of this register is shifted in from the Bluetooth interface.

0x647 AFE Voice DAI Bluetooth RX Data Register 1 AFE_VDBRX_DAT1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDBRX_DAT 1															
Type	RO															
Reset	0															

DAI Bluetooth receiving data register 1. This register is read by DSP in an 8K ISR if the corresponding DAI test is set or the Bluetooth function is turned on. The content of this register is shifted in from the SS or Bluetooth module.

0x648 AFE Voice DAI Bluetooth Control Register AFE_VDSP_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VDSP_RDY
Type																R/W
Reset																0

DSP sets this register to inform hardware that it is ready for data transmission. In DAI test modes, DSP starts a test by setting vdsp_rdy when speech samples are required or are ready. In normal mode, the DSP asserts this bit to ungate the downlink path data. Otherwise, the downlink data remains zero.

VDSP_RDY Ready indication to start the voice band data path.

0x649 AFE I2S Input Mode Buffer AFE_EDI_RDATA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDATA															
Type	RO															
Reset	0															

This is the register for reading I2S input data. For each audio interrupt, DSP should read 6 pairs (total 12 reads) of the input data. If DSP is reading too fast or too slow, there is a 2-word margin for repeating or dropping the samples that DSP read rate can not match-up with audio front end.

DATA Read data port. Left channel first, and then right channel.

0x64A AFE AGC DSP Control AEF_VAGC_VAD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								NADPATT_DBGAIN						NGATEOPEN	VAD2	VAD
Type								R/W						R/W	R/W	R/W
Reset								000000						0	0	0

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This register is for DSP to read/write the parameter of AGC.

VAD Strong VAD flag
- **0** off
- **1** on

VAD2 Weak VAD flag
- **0** off
- **1** on

NGATEOPEN noise gate flag
- **0** noise gate close
- **1** noise gate open

NADPATT_DBGAIN noise adaptive attenuation DB gain
- **[0,63]** 0~63dB

0x64B AFE AGC DSP Control AEF_VAGC_CNTR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTR_REL_FF															TONE FLG
Type	R/W															R/W
Reset	000000000000000															0

This register is for DSP to read/write the parameter of AGC.

TONEFLG Tone flag
- **0** off
- **1** on

CNTR_REL_FF Proceed very fast release if N samples value smaller than the fast release threshold
- **0~32767** N=0~32767 @ 52kHz sampling rate.

0x64C AFE AGC DSP Control1 AEF_VAGC_CNTR1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NCNTRRLZ								NCNTRATK							
Type	RO								RO							
Reset	0000_0000								0000_0000							

This register is for DSP to read the parameter of AGC.

NCNTRRLZ Release counter (in unit of 52kHz/256 sampling rate).

NCNTRATK Attack counter (in unit of 52kHz/16 sampling rate).

0x64D AFE AGC DSP Control AEF_VAGC_STETE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SSTATE		FGAINDB					
Type									RO		RO					
Reset									00		000000					

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This register is for DSP to read the parameter of AGC.

FGAINDB Current PGA gain (from 0 to 31 dB).
SSTATE Current AGC state.

0x64E AFE AGC DSP Control AEF_VAGC_RMS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIGRMSATT								SIGRMS							
Type	RO								RO							
Reset	00000000								00000000							

This register is for DSP to read the parameter of AGC.

SIGRMS RMS of signal
SIGRMSATT RMS of signal for attack usage

0x64F AFE Audio Control Register AFE_ADSP_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															ARST_FIFO	ADSP_RDY
Type															R/W	R/W
Reset															0	0

DSP sets this register to inform hardware that it is ready for data transmission. DSP asserts this bit to ungate the audio path data. Otherwise, the audio path data remains zero.

ADSP_RDY Ready to ungate audio data path.

ARST_FIFO Reset the FIFO read/write pointers and the interrupt counter.

0x650 AFE Audio Right-Channel Data Register 0 AFE_ARCH_DAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARCH_DAT0															
Type	W															
Reset	0															

Audio right channel data register 0. The content of this register is used as the right channel digital filter inputs.

The frequency of audio interrupts varies with the audio sampling rate and bypass setting, and can be 1/6 the audio sampling rate, or 1/12 the sampling rate, or 1/24 the sampling rate. The frequency depends on the setting of BYPASS.

- BYPASS = 00b: 1/24 the sampling rate.
- BYPASS = 01b: 1/12 the sampling rate.
- BYPASS = 10b: 1/6 the sampling rate.

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- BYPASS = 11b: 1/6 the sampling rate.

For DSP, 6 audio samples are written when an interrupt is received.

0x651 AFE AGC DSP GAIN AFE_VAGC_GAIN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											VAGC_GAIN					
Type											R/W					
Reset											000000					

AGC Gain setting by AGC. It is only validate while VAGC_CTRL is set to 1.

0x658 AFE Audio Left-Channel Data Register 0 AFE_ALCH_DAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ALCH_DAT0															
Type	W															
Reset	0															

Audio left channel data register 0. The content of this register is used as the left channel digital filter inputs.

7.4 Programming Guide

Several cases – including speech call, voice memo record, voice memo playback, melody playback and DAI tests – requires that partial or the whole audio front-end be turned on.

The following are the recommended voice band path programming procedures to turn on audio front-end:

1. MCU programs the AFE_VMCU_CON1, AFE_VMCU_CON2, AFE_DAI_CON, AFE_VAGC_CON1, AFE_VAGC_CON2, AFE_VAGC_CON3, AFE_VAGC_CON4, AFE_VAGC_CON5, AFE_VAGC_CON6, AFE_VLB_CON, AFE_VAG_CON, AFE_VAC_CON0, AFE_VAC_CON1 and AFE_VAPDN_CON registers for specific operation modes. Refer also to the analog chip interface specification.
2. MCU clears the VAFE bit of the PDN_CON2 register to ungate the clock for the voice band path. Refer to the software power down control specification.
3. MCU sets AFE_VMCU_CON0 to start operation of the voice band path.

The following are the recommended voice band path programming procedures to turn off audio front-end:

1. MCU programs AFE_VAPDN_CON to power down the voice band path analog blocks.
2. MCU clears AFE_VMCU_CON0 to stop operation of the voice band path.
3. MCU sets VAFE bit of PDN_CON2 register to gate the clock for the voice band path.

The following are the recommended audio band path programming procedures to turn on audio front-end:

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1. MCU programs the AFE_AMCU_CON1, AFE_AMCU_CON2, AFE_AAG_CON, AFE_AAC_CON, and AFE_AAPDN_CON registers for specific configurations. Refer also to the analog chip interface specification.
2. MCU clears the AAFE bit of the PDN_CON2 register to ungate the clock for the audio band path. Refer to the software power down control specification.
3. MCU sets AFE_AMCU_CON0 to start operation of the audio band path.

The following are the recommended audio band path programming procedures to turn off audio front-end:

1. MCU programs the AFE_AAPDN_CON to power down the audio band path analog blocks. Refer also to the analog block specification for further details.
2. MCU clears AFE_AMCU_CON0 to stop operation of the audio band path.
3. MCU sets the AAFE bit of the PDN_CON2 register to gate the clock for the audio band path.

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8 Radio Interface Control

This chapter details the MT6253 interface control with the radio part of a GSM terminal. Providing a comprehensive control scheme, the MT6253 radio interface consists of Baseband Serial Interface (BSI), Baseband Parallel Interface (BPI) and Automatic Power Control (APC) together with APC-DAC and AFC-DAC.

8.1 Baseband Serial Interface

The Baseband Serial Interface controls external radio components. A 3-wire serial bus transfers data to RF circuitry for PLL frequency change, reception gain setting, and other radio control purposes. In this unit, BSI data registers are double-buffered in the same way as the TDMA event registers. The user writes data into the write buffer and the data is transferred from the write buffer to the active buffer when a TDMA_EVTVAL signal (from the TDMA timer) is pulsed.

Each data register BSI_D*n*_DAT is associated with one data control register BSI_D*n*_CON, where *n* denotes the index. Each data control register identifies which events (signaled by TDMA_BSISTR*n*, generated by the TDMA timer) trigger the download process of the word in register BSI_D*n*_DAT. The word and its length (in bits) is downloaded via the serial bus. A special event is triggered when the IMOD flag is set to 1: it provides immediate download process without software programming the TDMA timer.

If more than one data word is to be downloaded on the same BSI event, the word with the lowest address among them is downloaded first, followed by the next lowest and so on.

The total download time depends on the word length, the number of words to download, and the clock rates. The programmer must space the successive events to provide enough time. If the download process of the previous event is not complete before a new event arrives, it will cause the erroneous download words..

The unit has four output ports to RF core unit: BSI_CLK is the output clock, BSI_DATA is the serial data port, and BSI_CS0 is the select pin and BSI_DIN is read-back data from RF core unit.

In order to support bi-directional read and write operations of the RF chip, software can directly write values to BSI_CLK, BSI_DATA and BSI_CS by programming the BSI_DOUT register. Data from the RF chip can be read by software via the register BSI_DIN. Before software can program the 3-wire behavior, the BSI_IO_CON register must be set.

The block diagram of the BSI unit is as depicted in **Figure 86.**

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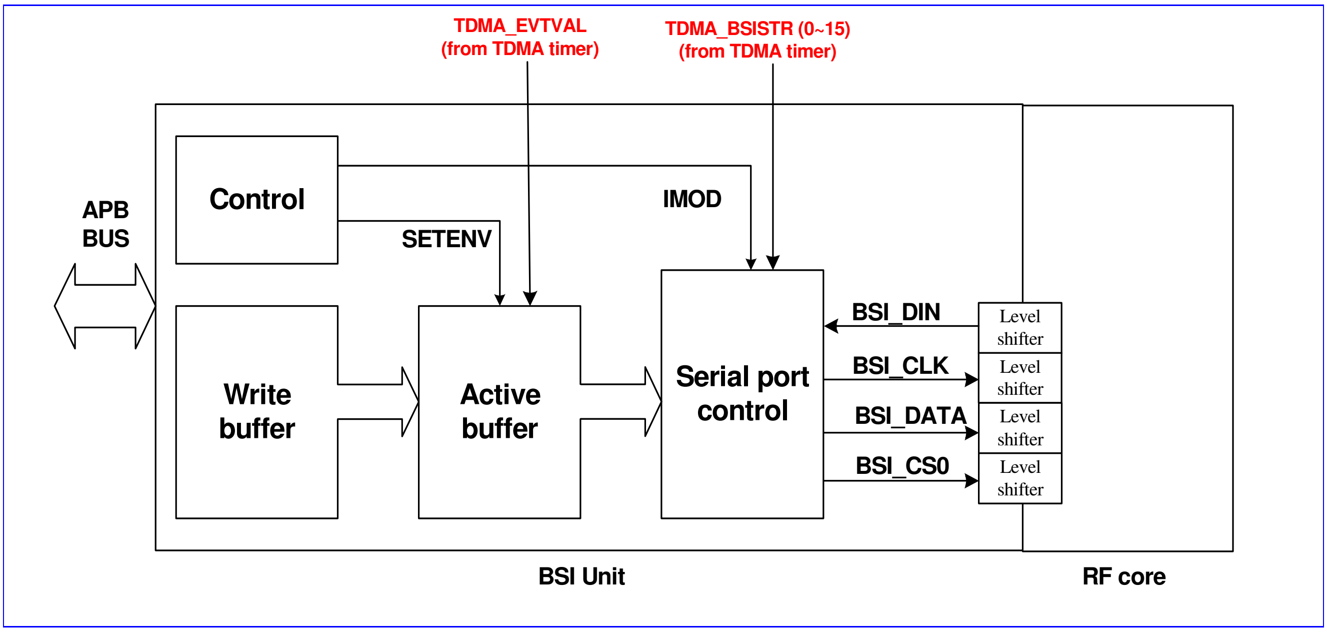

Figure 86 Block diagram of BSI unit

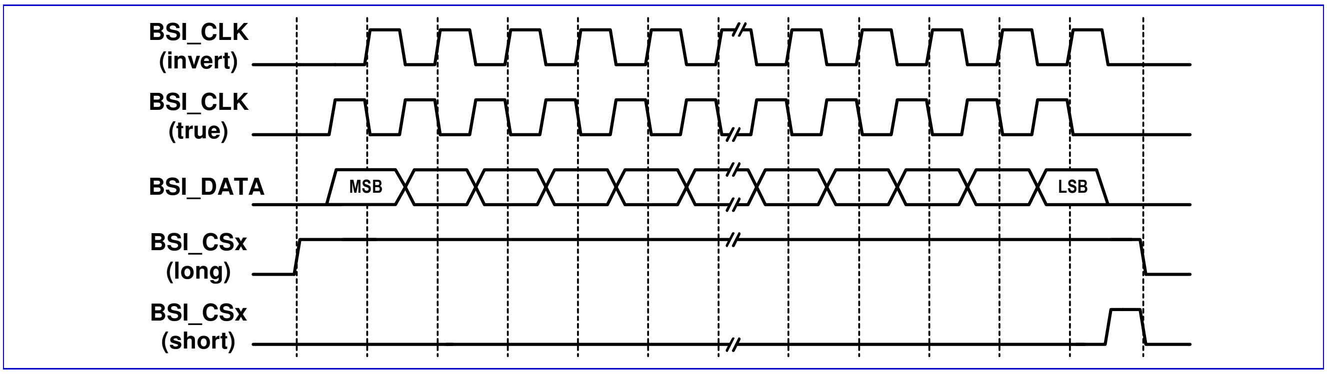

Figure 87 Timing characteristic of BSI interface

8.1.1 Register Definitions

Register Address	Register Function	Acronym
0x8201_0000	BSI control register	BSI_CON
0x8201_0190	BSI event enable register	BSI_ENA_0
0x8201_0194	BSI event enable register – MSB 4 bits	BSI_ENA_1
0x8201_0198	BSI IO mode control register	BSI_IO_CON
0x8201_019C	Software-programmed data out	BSI_DOUT

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0x8201_01A0	Input data from RF chip	BSI_DIN
0x8201_01A4	BSI data pair number	BSI_PAIR_NUM

Table 65 BSI Control Registers

0x8201_0000 BSI control register BSI_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								SETENV	EN1_POL	EN1_LEN	EN0_POL	EN0_LEN	IMOD	CLK_SPD		CLK_POL
Type								R/W	R/W	R/W	R/W	R/W	WO	R/W		R/W
Reset								0	0	0	0	0	N/A	0		0

This register is the control register for the BSI unit. The register controls the signal type of the 3-wire interface.

CLK_POL Controls the polarity of BSI_CLK. Refer to **Figure 87.**

- **0** True clock polarity
- **1** Inverted clock polarity

CLK_SPD Defines the clock rate of BSI_CLK. The 3-wire interface provides 4 choices of data bit rate. The default is 52/2 MHz.

- **00** 52/2 MHz
- **01** 52/4 MHz
- **10** 52/6 MHz
- **11** 52/8 MHz

IMOD Enables immediate mode. If the user writes 1 to the flag, the download is triggered immediately without waiting for the timer events. The words for which the register event ID equals 1Fh are downloaded following this signal. This flag is write-only. The immediate write is exercised only once: the programmer must write the flag again to invoke another immediate download. Setting the flag does not disable the other events from the timer; the programmer can disable all events by setting BSI_ENA to all zeros.

- **0** Reserved
- **1** Trigger Immediate Mode

ENX_LEN Controls the type of signals BSI_CS0. Refer to **Figure 86.**

- **0** Long enable pulse
- **1** Short enable pulse

ENX_POL Controls the polarity of signals BSI_CS0.

- **0** True enable pulse polarity
- **1** Inverted enable pulse polarity

SETENV Enables the write operation of the active buffer.

- **0** The user writes to the write buffer. The data is then latched in the active buffer after TDMA_EVTVAL is pulsed.
- **1** The user writes data directly to the active buffer. If BSI module clock is gated by SW PDN, SW can not write the active buffer in this period (power down period).

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0x8201_0004 Control part of data register 0 BSI_D0_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISB	LEN										EVT_ID				
Type	R/W	R/W										R/W				

This register is the control part of the data register 0. The register determines the required length of the download data word, the event to trigger the download process of the word, and the targeted device.

Table 66 lists the 44 data registers of this type. The max length of the first 40 data registers is 32 bits, and that of the last 4 data registers is 78 bits. Multiple data control registers may contain the same event ID. The data words of all registers with the same event ID are downloaded when the event occurs.

EVT_ID Stores the event ID for which the data word awaits to be downloaded.

00000~10011 Synchronous download of the word with the selected EVT_ID event. The relationship between this field and the event is listed as **Table 66.**

Event ID (in binary) – EVT_ID	Event name
00000	TDMA_BSISTR0
00001	TDMA_BSISTR1
00010	TDMA_BSISTR2
00011	TDMA_BSISTR3
00100	TDMA_BSISTR4
00101	TDMA_BSISTR5
00110	TDMA_BSISTR6
00111	TDMA_BSISTR7
01000	TDMA_BSISTR8
01001	TDMA_BSISTR9
01010	TDMA_BSISTR10
01011	TDMA_BSISTR11
01100	TDMA_BSISTR12
01101	TDMA_BSISTR13
01110	TDMA_BSISTR14
01111	TDMA_BSISTR15
10000	TDMA_BSISTR16
10001	TDMA_BSISTR17
10010	TDMA_BSISTR18
10011	TDMA_BSISTR19

Table 66 The relationship between the value of EVT_ID field in the BSI control registers and the TDMA_BSISTR events

10100~11110 Reserved

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11111 Immediate download

LEN The field stores the length of the data word. The actual length is defined as LEN + 1 in units of bits. For data registers 0~39, the value ranges from 0 to 31, corresponding to 1 to 32 bits in length. For data registers 40~43, the value ranges from 0 to 77, corresponding to 1 to 78 bits in length.

ISB The flag selects the target device.

0 Device 0 is selected.

1 Device 1 is selected.

0x8201_0008 Data part of data register 0 BSI_D0_DAT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT [31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT [15:0]															
Type	R/W															

This register is the data part of the data register 0. The legal length of the data is up to 32 bits. The actual number of bits to be transmitted is specified in LEN field in the BSI_D0_CON register.

DAT The field signifies the data part of the data register.

Table 67 lists the address mapping and function of the 44 pairs of data registers.

Register Address	Register Function	Acronym
0x8201_0004	Control part of data register 0	BSI_D0_CON
0x8201_0008	Data part of data register 0	BSI_D0_DAT
0x8201_000C	Control part of data register 1	BSI_D1_CON
0x8201_0010	Data part of data register 1	BSI_D1_ DAT
0x8201_0014	Control part of data register 2	BSI_D2_CON
0x8201_0018	Data part of data register 2	BSI_D2_ DAT
0x8201_001C	Control part of data register 3	BSI_D3_CON
0x8201_0020	Data part of data register 3	BSI_D3_ DAT
0x8201_0024	Control part of data register 4	BSI_D4_CON
0x8201_0028	Data part of data register 4	BSI_D4_ DAT
0x8201_002C	Control part of data register 5	BSI_D5_CON
0x8201_0030	Data part of data register 5	BSI_D5_ DAT
0x8201_0034	Control part of data register 6	BSI_D6_CON
0x8201_0038	Data part of data register 6	BSI_D6_ DAT
0x8201_003C	Control part of data register 7	BSI_D7_CON
0x8201_0040	Data part of data register 7	BSI_D7_ DAT
0x8201_0044	Control part of data register 8	BSI_D8_CON
0x8201_0048	Data part of data register 8	BSI_D8_ DAT

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0x8201_004C	Control part of data register 9	BSI_D9_CON
0x8201_0050	Data part of data register 9	BSI_D9_ DAT
0x8201_0054	Control part of data register 10	BSI_D10_CON
0x8201_0058	Data part of data register 10	BSI_D10_ DAT
0x8201_005C	Control part of data register 11	BSI_D11_CON
0x8201_0060	Data part of data register 11	BSI_D11_ DAT
0x8201_0064	Control part of data register 12	BSI_D12_CON
0x8201_0068	Data part of data register 12	BSI_D12_ DAT
0x8201_006C	Control part of data register 13	BSI_D13_CON
0x8201_0070	Data part of data register 13	BSI_D13_ DAT
0x8201_0074	Control part of data register 14	BSI_D14_CON
0x8201_0078	Data part of data register 14	BSI_D14_ DAT
0x8201_007C	Control part of data register 15	BSI_D15_CON
0x8201_0080	Data part of data register 15	BSI_D15_ DAT
0x8201_0084	Control part of data register 16	BSI_D16_CON
0x8201_0088	Data part of data register 16	BSI_D16_ DAT
0x8201_008C	Control part of data register 17	BSI_D17_CON
0x8201_0090	Data part of data register 17	BSI_D17_ DAT
0x8201_0094	Control part of data register 18	BSI_D18_CON
0x8201_0098	Data part of data register 18	BSI_D18_ DAT
0x8201_009C	Control part of data register 19	BSI_D19_CON
0x8201_00A0	Data part of data register 19	BSI_D19_ DAT
0x8201_00A4	Control part of data register 20	BSI_D20_CON
0x8201_00A8	Data part of data register 20	BSI_D20_ DAT
0x8201_00AC	Control part of data register 21	BSI_D21_CON
0x8201_00B0	Data part of data register 21	BSI_D21_ DAT
0x8201_00B4	Control part of data register 22	BSI_D22_CON
0x8201_00B8	Data part of data register 22	BSI_D22_ DAT
0x8201_00BC	Control part of data register 23	BSI_D23_CON
0x8201_00C0	Data part of data register 23	BSI_D23_ DAT
0x8201_00C4	Control part of data register 24	BSI_D24_CON
0x8201_00C8	Data part of data register 24	BSI_D24_ DAT
0x8201_00CC	Control part of data register 25	BSI_D25_CON
0x8201_00D0	Data part of data register 25	BSI_D25_ DAT
0x8201_00D4	Control part of data register 26	BSI_D26_CON
0x8201_00D8	Data part of data register 26	BSI_D26_ DAT

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0x8201_00DC	Control part of data register 27	BSI_D27_CON
0x8201_00E0	Data part of data register 27	BSI_D27_ DAT
0x8201_00E4	Control part of data register 28	BSI_D28_CON
0x8201_00E8	Data part of data register 28	BSI_D28_ DAT
0x8201_00EC	Control part of data register 29	BSI_D29_CON
0x8201_00F0	Data part of data register 29	BSI_D29_ DAT
0x8201_00F4	Control part of data register 30	BSI_D30_CON
0x8201_00F8	Data part of data register 30	BSI_D30_ DAT
0x8201_00FC	Control part of data register 31	BSI_D31_CON
0x8201_0100	Data part of data register 31	BSI_D31_ DAT
0x8201_0104	Control part of data register 32	BSI_D32_CON
0x8201_0108	Data part of data register 32	BSI_D32_ DAT
0x8201_010C	Control part of data register 33	BSI_D33_CON
0x8201_0110	Data part of data register 33	BSI_D33_ DAT
0x8201_0114	Control part of data register 34	BSI_D34_CON
0x8201_0118	Data part of data register 34	BSI_D34_ DAT
0x8201_011C	Control part of data register 35	BSI_D35_CON
0x8201_0120	Data part of data register 35	BSI_D35_ DAT
0x8201_0124	Control part of data register 36	BSI_D36_CON
0x8201_0128	Data part of data register 36	BSI_D36_ DAT
0x8201_012C	Control part of data register 37	BSI_D37_CON
0x8201_0130	Data part of data register 37	BSI_D37_ DAT
0x8201_0134	Control part of data register 38	BSI_D38_CON
0x8201_0138	Data part of data register 38	BSI_D38_ DAT
0x8201_013C	Control part of data register 39	BSI_D39_CON
0x8201_0140	Data part of data register 39	BSI_D39_ DAT
0x8201_0144	Control part of data register 40	BSI_D40_CON
0x8201_0148	Data part of data register 40 (MSB 14 bits)	BSI_D40_ DAT2
0x8201_014C	Data part of data register 40	BSI_D40_ DAT1
0x8201_0150	Data part of data register 40 (LSB 32 bits)	BSI_D40_ DAT0
0x8201_0154	Control part of data register 41	BSI_D41_CON
0x8201_0158	Data part of data register 41 (MSB 14 bits)	BSI_D41_ DAT2
0x8201_015C	Data part of data register 41	BSI_D41_ DAT1
0x8201_0160	Data part of data register 41 (LSB 32 bits)	BSI_D41_ DAT0
0x8201_0164	Control part of data register 42	BSI_D42_CON
0x8201_0168	Data part of data register 42 (MSB 14 bits)	BSI_D42_ DAT2

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0x8201_016C	Data part of data register 42	BSI_D42_ DAT1
0x8201_0170	Data part of data register 42 (LSB 32 bits)	BSI_D42_ DAT0
0x8201_0174	Control part of data register 43	BSI_D43_CON
0x8201_0178	Data part of data register 43 (MSB 14 bits)	BSI_D43_ DAT2
0x8201_017C	Data part of data register 43	BSI_D43_ DAT1
0x8201_0180	Data part of data register 43 (LSB 32 bits)	BSI_D43_ DAT0

Table 67 BSI data registers

0x8201_0190 BSI event enable register BSI_ENA_0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI15	BSI14	BSI13	BSI12	BSI11	BSI10	BSI9	BSI8	BSI7	BSI6	BSI5	BSI4	BSI3	BSI2	BSI1	BSI0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

This register enables an event by setting the corresponding bit. After a hardware reset, all bits are initialized to 1. These bits are also set to 1 after TDMA_EVTVAL pulse.

BSIx Enables downloading of the words corresponding to the events signaled by TMDA_BSI.

0 The event is not enabled.

1 The event is enabled.

0x8201_0194 BSI event enable register – MSB 4 bits BSI_ENA_1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BSI19	BSI18	BSI17	BSI16
Type													R/W	R/W	R/W	R/W
Reset													1	1	1	1

The register could enable the event by setting the corresponding bit. After hardware reset, all bits are initialized as 1. Besides, those bits are set as 1 after TDMA_EVTVAL is pulsed.

BSIx The flag enables the downloading of the words that corresponds to the events signaled by TMDA_BSI.

0 The event is not enabled.

The event is enabled.

0x8201_0198 BSI IO mode control register BSI_IO_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MODE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MODE Defines the source of BSI signal.

0 BSI signal is generated by the hardware.

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1 BSI signal is generated by the software. In this mode, the BSI clock depends on the value of the field DOUT.CLK. BSI_CS depends on the value of the field DOUT.CS and BSI_DATA depends on the value of the field DOUT.DATA.

0x8201_019C Software-programmed data out BSI_DOUT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DATA	CS	CLK
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	W	W	W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CLK Signifies the BSI_CLK signal.
CS Signifies the BSI_CS signal.
DATA Signifies the BSI_DATA signal.

0x8201_01A0 Input data from RF chip BSI_DIN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DIN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DIN Registers the input value of BSI_DATA from the RF chip.

0x8201_01A4 BSI data pair number BSI_PAIR_NUM

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											PAIR_NUM					
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R					
Reset	0	0	0	0	0	0	0	0	0	0	28					

PAIR_NUM The software can program how many pairs of data register to be used. The default value is 28 pairs. This value must be smaller or equal to 44. The first 40 pairs are 32-bit long, and the last four pairs are 78-bit long.

8.2 Baseband Parallel Interface

8.2.1 General Description

The Baseband Parallel Interface features 7 control pins, which are used for timing-critical external circuits. These pins typically control front-end components which must be turned on or off at specific times during GSM operation, such as transmit-enable, band switching, TR-switch, etc.

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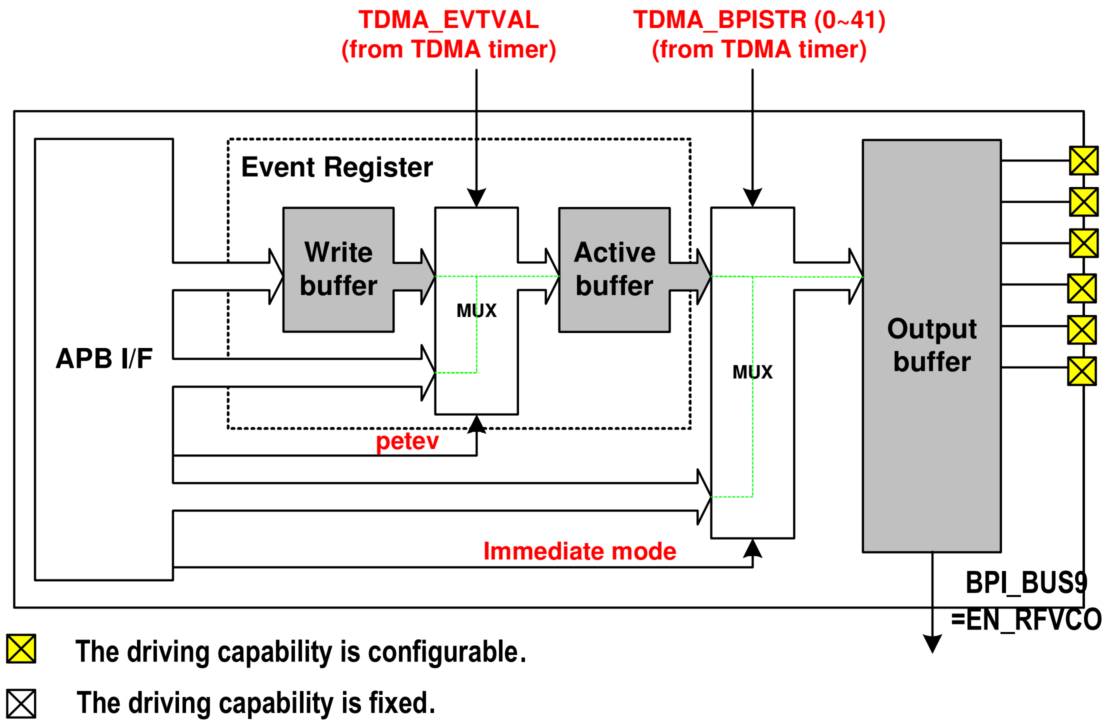

Figure 88 Block diagram of BPI interface

The user can program 42 sets of 7-bit registers to set the output value of BPI_BUS0~BPI_BUS5 and BPI_BUS9. BPI_BUS9 is used for EN_RFVCO. The data is stored in the write buffers. The write buffers are then forwarded to the active buffers when the TDMA_EVTVAL signal is pulsed, usually once per frame. Each of the 42 write buffers corresponds to an active buffer, as well as to a TDMA event.

Each TDMA_BPISTR event triggers the transfer of data in the corresponding active buffer to the output buffer, thus changing the value of the BPI bus. The user can disable the events by programming the enable registers in the TDMA timer. If the TDMA_BPISTR event is disabled, the corresponding signal TDMA_BPISTR is not pulsed, and the value on the BPI bus remains unchanged.

For applications in which BPI signals serve as the switch, current-driving components are typically added to enhance driving capability. Three configurable output pins provide current up to 8 mA, and help reduce the number of external components.

8.2.2 Register Definitions

Register Address	Register Function	Acronym
0x8202_0000	BPI control register	BPI_CON
0x8202_00B0	BPI event enable register 0	BPI_ENA0

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0x8202_00B4	BPI event enable register 1	BPI_ENA1
0x8202_00B8	BPI event enable register 2	BPI_ENA2

Table 68 BPI Control Registers

0x8202_0000 BPI control register BPI_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										PINM5	PINM4	PINM3	PINM2	PINM1	PINM0	PETEV
Type										WO	WO	WO	WO	WO	WO	R/W
Reset										0	0	0	0	0	0	0

This register is the control register of the BPI unit. The register controls the direct access mode of the active buffer and the current driving capability for the output pins.

The driving capabilities of BPI_BUSx can be 2 mA or 8 mA, determined by the value of PINMx. These output pins provide a higher driving capability and save on external current-driving components

PETEV Enables direct access to the active buffer.

- **0** The user writes data to the write buffer. The data is latched in the active buffer after the TDMA_EVTVAL signal is pulsed.
- **1** The user directly writes data to the active buffer without waiting for the TDMA_EVTVAL signal.

PINMx Controls the driving capability of BPI_BUSx.

- **0** The output driving capability is 2mA.
- **1** The output driving capability is 8mA.

0x8202_0004 BPI data register 0 BPI_BUF0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							PO9				PO5	PO4	PO3	PO2	PO1	PO0
Type							R/W				R/W	R/W	R/W	R/W	R/W	R/W

This register defines the BPI signals that are associated with the event TDMA_BPI0.

Table 69 lists 42 registers of the same structure, each of which is associated with one specific event signal from the TDMA timer. The data registers are all double-buffered. When PETEV is set to 0, the data register links to the write buffer. When PETEV is set to 1, the data register links to the active buffer.

One register, BPI_BUFI, is dedicated for use in immediate mode. Writing a value to that register effects an immediate change in the corresponding BPI signal and bus.

POx This flag defines the corresponding signals for BPIx after the TDMA event 0 takes place.

The overall data register definition is listed in **Table 69.**

Register Address	Register Function	Acronym
0x8202_0004	BPI pin data for event TDMA_BPI 0	BPI_BUF0

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0x8202_0008	BPI pin data for event TDMA_BPI 1	BPI_BUF1
0x8202_000C	BPI pin data for event TDMA_BPI 2	BPI_BUF2
0x8202_0010	BPI pin data for event TDMA_BPI 3	BPI_BUF3
0x8202_0014	BPI pin data for event TDMA_BPI 4	BPI_BUF4
0x8202_0018	BPI pin data for event TDMA_BPI 5	BPI_BUF5
0x8202_001C	BPI pin data for event TDMA_BPI 6	BPI_BUF6
0x8202_0020	BPI pin data for event TDMA_BPI 7	BPI_BUF7
0x8202_0024	BPI pin data for event TDMA_BPI 8	BPI_BUF8
0x8202_0028	BPI pin data for event TDMA_BPI 9	BPI_BUF9
0x8202_002C	BPI pin data for event TDMA_BPI 10	BPI_BUF10
0x8202_0030	BPI pin data for event TDMA_BPI 11	BPI_BUF11
0x8202_0034	BPI pin data for event TDMA_BPI 12	BPI_BUF12
0x8202_0038	BPI pin data for event TDMA_BPI 13	BPI_BUF13
0x8202_003C	BPI pin data for event TDMA_BPI 14	BPI_BUF14
0x8202_0040	BPI pin data for event TDMA_BPI 15	BPI_BUF15
0x8202_0044	BPI pin data for event TDMA_BPI 16	BPI_BUF16
0x8202_0048	BPI pin data for event TDMA_BPI 17	BPI_BUF17
0x8202_004C	BPI pin data for event TDMA_BPI 18	BPI_BUF18
0x8202_0050	BPI pin data for event TDMA_BPI 19	BPI_BUF19
0x8202_0054	BPI pin data for event TDMA_BPI 20	BPI_BUF20
0x8202_0058	BPI pin data for event TDMA_BPI 21	BPI_BUF21
0x8202_005C	BPI pin data for event TDMA_BPI 22	BPI_BUF22
0x8202_0060	BPI pin data for event TDMA_BPI 23	BPI_BUF23
0x8202_0064	BPI pin data for event TDMA_BPI 24	BPI_BUF24
0x8202_0068	BPI pin data for event TDMA_BPI 25	BPI_BUF25
0x8202_006C	BPI pin data for event TDMA_BPI 26	BPI_BUF26
0x8202_0070	BPI pin data for event TDMA_BPI 27	BPI_BUF27
0x8202_0074	BPI pin data for event TDMA_BPI 28	BPI_BUF28
0x8202_0078	BPI pin data for event TDMA_BPI 29	BPI_BUF29
0x8202_007C	BPI pin data for event TDMA_BPI 30	BPI_BUF30
0x8202_0080	BPI pin data for event TDMA_BPI 31	BPI_BUF31
0x8202_0084	BPI pin data for event TDMA_BPI 32	BPI_BUF32
0x8202_0088	BPI pin data for event TDMA_BPI 33	BPI_BUF33
0x8202_008C	BPI pin data for event TDMA_BPI 34	BPI_BUF34
0x8202_0090	BPI pin data for event TDMA_BPI 35	BPI_BUF35
0x8202_0094	BPI pin data for event TDMA_BPI 36	BPI_BUF36

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0x8202_0098	BPI pin data for event TDMA_BPI 37	BPI_BUF37
0x8202_009C	BPI pin data for event TDMA_BPI 38	BPI_BUF38
0x8202_00A0	BPI pin data for event TDMA_BPI 39	BPI_BUF39
0x8202_00A4	BPI pin data for event TDMA_BPI 40	BPI_BUF40
0x8202_00A8	BPI pin data for event TDMA_BPI 41	BPI_BUF41
0x8202_00AC	BPI pin data for immediate mode	BPI_BUFI

Table 69 BPI Data Registers

0x8202_00B0 BPI event enable register 0 BPI_ENA0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BEN15	BEN14	BEN13	BEN12	BEN11	BEN10	BEN9	BEN8	BEN7	BEN6	BEN5	BEN4	BEN3	BEN2	BEN1	BEN0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

This register enables the events that are signaled by the TDMA timer: by clearing a register bit, the corresponding event signal is ignored. After a hardware reset, all the enable bits default to 1 (enabled). Upon receiving a TDMA_EVTVAL pulse, all register bits are also set to 1 (enabled).

BENn This flag indicates whether event n signals are heeded or ignored.

- **0** Event n is disabled (ignored).
- **1** Event n is enabled.

0x8202_00B4 BPI event enable register 1 BPI_ENA1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BEN31	BEN30	BEN29	BEN28	BEN27	BEN26	BEN25	BEN24	BEN23	BEN22	BEN21	BEN20	BEN19	BEN18	BEN17	BEN16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

This register enables the events that are signaled by the TDMA timing generator: by clearing a register bit, the corresponding event signal is ignored. After a hardware reset, all the enable bits default to 1 (enabled). Upon receiving the TDMA_EVTVAL pulse, all register bits are also set to 1 (enabled).

BENn This flag indicates whether event n signals are heeded or ignored.

- **0** Event n is disabled (ignored)
- **1** Event n is enabled

0x8202_00B8 BPI event enable register 2 BPI_ENA2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							BEN41	BEN40	BEN39	BEN38	BEN37	BEN36	BEN35	BEN34	BEN33	BEN32
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset							1	1	1	1	1	1	1	1	1	1

The register is used to enable the events that are signaled by the TDMA timing generator. After hardware reset, all the enable bits defaults to be 1 (enabled). Upon receiving the TDMA_EVTVAL pulse, those bits are also set to 1 (enabled).

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BENn The flag controls the function of event n.

0 The event n is disabled.

The event n is enabled.

8.3 Automatic Power Control (APC) Unit

8.3.1 General Description

The Automatic Power Control (APC) unit controls the Power Amplifier (PA) module. Through APC unit, the proper transmit power level of the handset can be set to ensure that burst power ramping requirements are met. In one TDMA frame, up to 7 TDMA events can be enabled to support multi-slot transmission. In practice, 5 banks of ramp profiles are used in one frame to make up 4 consecutive transmission slots.

The shape and magnitude of the ramp profiles are configurable to fit ramp-up (ramp up from zero), intermediate ramp (ramp between transmission windows), and ramp-down (ramp down to zero) profiles. Each bank of the ramp profile consists of 16 8-bit unsigned values, which are adjustable for different conditions.

The entries from one bank of the ramp profile are partitioned into two parts, with 8 values in each half. In normal operation, the entries in the left half are multiplied by a 10-bit left scaling factor, and the entries in the right half are multiplied by a 10-bit right scaling factor. The values are then truncated to form 16 10-bit intermediate values. Finally the intermediate ramp profile are linearly interpolated into 32 10-bit values and sequentially used to update the D/A converter. The block diagram of the APC unit is shown in **Figure 89 .**

The APB bus interface is 32 bits wide. Four write accesses are required to program each bank of ramp profile. The detailed register allocations are listed in **Table 70.**

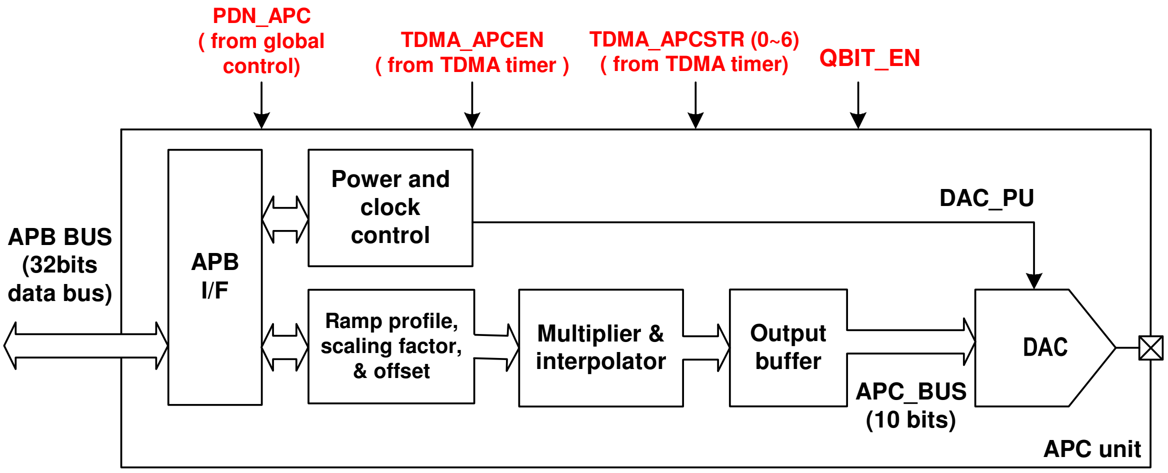

Figure 89 Block diagram of APC unit

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8.3.2 Register Definitions

0x8204_0000 APC 1st ramp profile #0 APC_PFA0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENT3								ENT2							
Type	R/W								R/W							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENT1								ENT0							
Type	R/W								R/W							

The register stores the first four entries of the first power ramp profile. The first entry resides in the least significant byte [7:0], the second entry in the second byte [15:8], the third entry in the third byte [23:16], and the fourth in the most significant byte [31:24]. Since this register provides no hardware reset, the programmer must configure it before any APC event takes place.

ENT3 The field signifies the 4th entry of the 1st ramp profile.
ENT2 The field signifies the 3rd entry of the 1st ramp profile.
ENT1 The field signifies the 2nd entry of the 1st ramp profile.
ENT0 The field signifies the 1st entry of the 1st ramp profile.

The overall ramp profile register definition is listed in **Table 70.**

Register Address	Register Function	Acronym
0x8204_0000	APC 1st ramp profile #0	APC_PFA0
0x8204_0004	APC 1st ramp profile #1	APC_PFA1
0x8204_0008	APC 1st ramp profile #2	APC_PFA2
0x8204_000C	APC 1st ramp profile #3	APC_PFA3
0x8204_0020	APC 2nd ramp profile #0	APC_PFB0
0x8204_0024	APC 2nd ramp profile #1	APC_PFB1
0x8204_0028	APC 2nd ramp profile #2	APC_PFB2
0x8204_002C	APC 2nd ramp profile #3	APC_PFB3
0x8204_0040	APC 3rd ramp profile #0	APC_PFC0
0x8204_0044	APC 3rd ramp profile #1	APC_PFC1
0x8204_0048	APC 3rd ramp profile #2	APC_PFC2
0x8204_004C	APC 3rd ramp profile #3	APC_PFC3
0x8204_0060	APC 4th ramp profile #0	APC_PFD0
0x8204_0064	APC 4th ramp profile #1	APC_PFD1
0x8204_0068	APC 4th ramp profile #2	APC_PFD2
0x8204_006C	APC 4th ramp profile #3	APC_PFD3
0x8204_0080	APC 5th ramp profile #0	APC_PFE0
0x8204_0084	APC 5th ramp profile #1	APC_PFE1
0x8204_0088	APC 5th ramp profile #2	APC_PFE2

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0x8204_008C	APC 5th ramp profile #3	APC_PFE3
0x8204_00A0	APC 6th ramp profile #0	APC_PFF0
0x8204_00A4	APC 6th ramp profile #1	APC_PFF1
0x8204_00A8	APC 6th ramp profile #2	APC_PFF2
0x8204_00AC	APC 6th ramp profile #3	APC_PFF3
0x8204_00C0	APC 7th ramp profile #0	APC_PFG0
0x8204_00C4	APC 7th ramp profile #1	APC_PFG1
0x8204_00C8	APC 7th ramp profile #2	APC_PFG2
0x8204_00CC	APC 7th ramp profile #3	APC_PFG3

Table 70 APC ramp profile registers

0x8204_0010 APC 1st ramp profile left scaling factor APC_SCAL0L

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SF									
Type							R/W									
Reset							1_0000_0000									

The register stores the left scaling factor of the 1st ramp profile. This factor multiplies the first 8 entries of the 1st ramp profile to provide the scaled profile, which is then interpolated to control the D/A converter.

After a hardware reset, the initial value of the register is 256. In this case, no scaling is done (each entry of the ramp profile is multiplied by 1), because the 8 least significant bits are truncated after multiplication.

The overall scaling factor register definition is listed in **Table 71.**

SF Scaling factor. After a hardware reset, the value is 256.

0x8204_0014 APC 1st ramp profile right scaling factor APC_SCAL0R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SF									
Type							R/W									
Reset							1_0000_0000									

The register stores the right scaling factor of the 1st ramp profile. This factor multiplies the last 8 entries of the 1st ramp profile to provide the scaled profile, which is then interpolated to control the D/A converter.

After a hardware reset, the initial value of the register is 256. In this case, no scaling is done (each entry of the ramp profile is multiplied by 1), because the 8 least significant bits are truncated after multiplication.

The overall scaling factor register definition is listed in **Table 71.**

SF Scaling factor. After a hardware reset, the value is 256.

0x8204_0018 APC 1st ramp profile offset value APC_OFFSET0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name							OFFSET
Type							R/W
Reset							0

There are 7 offset values for the corresponding ramp profile.

The 1st offset value also serves as the pedestal value. The value is used to power up the APC D/A converter before the RF signals start to transmit. The D/A converter is then biased on the value, to provide the initial control voltage for the external control loop. The exact value depends on the characteristics of the external components. The timing to output the pedestal value is configurable through the TDMA_BULCON2 register of the timing generator; its valid range is 0~127 quarter-bits of time after the baseband D/A converter is powered up.

OFFSET Offset value for the corresponding ramp profile. After a hardware reset, the default value is 0.

The overall offset register definition is listed in **Table 71.**

Register Address	Register Function	Acronym
0x8204_0010	APC 1st ramp profile left scaling factor	APC_SCAL0L
0x8204_0014	APC 1st ramp profile right scaling factor	APC_SCAL0R
0x8204_0018	APC 1st ramp profile offset value	APC_OFFSET0
0x8204_0030	APC 2nd ramp profile left scaling factor	APC_SCAL1L
0x8204_0034	APC 2nd ramp profile right scaling factor	APC_SCAL1R
0x8204_0038	APC 2nd ramp profile offset value	APC_OFFSET1
0x8204_0050	APC 3rd ramp profile left scaling factor	APC_SCAL2L
0x8204_0054	APC 3rd ramp profile right scaling factor	APC_SCAL2R
0x8204_0058	APC 3rd ramp profile offset value	APC_OFFSET2
0x8204_0070	APC 4th ramp profile left scaling factor	APC_SCAL3L
0x8204_0074	APC 4th ramp profile right scaling factor	APC_SCAL3R
0x8204_0078	APC 4th ramp profile offset value	APC_OFFSET3
0x8204_0090	APC 5th ramp profile left scaling factor	APC_SCAL4L
0x8204_0094	APC 5th ramp profile right scaling factor	APC_SCAL4R
0x8204_0098	APC 5th ramp profile offset value	APC_OFFSET4
0x8204_00B0	APC 6th ramp profile left scaling factor	APC_SCAL5L
0x8204_00B4	APC 6th ramp profile right scaling factor	APC_SCAL5R
0x8204_00B8	APC 6th ramp profile offset value	APC_OFFSET5
0x8204_00D0	APC 7th ramp profile left scaling factor	APC_SCAL6L
0x8204_00D4	APC 7th ramp profile right scaling factor	APC_SCAL6R
0x8204_00D8	APC 7th ramp profile offset value	APC_OFFSET6

Table 71 APC scaling factor and offset value registers

0x8204_00E0h APC control register APC_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name															GSM	FPU
Type															R/W	R/W
Reset															1	0

GSM Defines the operation mode of the APC module. In GSM mode, each frame has only one slot, thus only one scaling factor and one offset value must be configured. If the GSM bit is set, the programmer needs only to configure APC_SCAL0L and APC_OFFSET0. If the bit is not set, the APC module is operating in GPRS mode.

- **0** The APC module is operating in GPRS mode.
- **1** The APC module is operating in GSM mode. Default value.

FPU Forces the APC D/A converter to power up. Test only.

- **0** The APC D/A converter is not forced to power up. The converter is only powered on when the transmission window is opened. Default value.
- **1** The APC D/A converter is forced to power up.

8.3.3 Ramp Profile Programming

The first value of the first normalized ramp profile must be written in the least significant byte of the APC_PFA0 register. The second value must be written in the second least significant byte of the APC_PFA0, and so on.

Each ramp profile can be programmed to form an arbitrary shape.

The start of ramping is triggered by one of the TDMA_APCSTR signals. The timing relationship between TDMA_APCSTR and TDMA slots is depicted in **Figure 90** for 4 consecutive time slots case. The power ramping profile must comply with the timing mask defined in GSM SPEC 05.05. The timing offset values for 7 ramp profiles are stored in the TDMA timer register from TDMA_APC0 to TDMA_APC6.

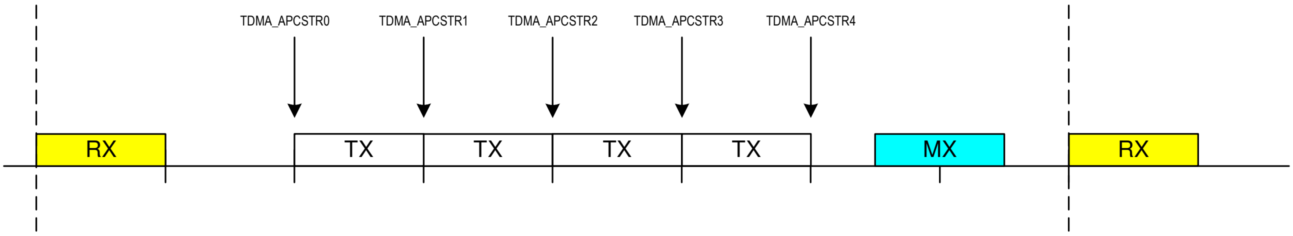

Figure 90 Timing diagram of TDMA_APCSTR

Because the APC unit provides more than 5 ramp profiles, up to 4 consecutive transmission slots can accommodated. The 2 additional ramp profiles are useful particularly when the timing between the last 2 transmission time slots and CTIRQ is uncertain; software can begin writing the ramp profiles for the succeeding frame during the current frame, alleviating the risk of not writing the succeeding frame's profile data in time.

In GPRS mode, to fit the intermediate ramp profile between different power levels, a simple scaling scheme is used to synthesize the ramp profile. The equation is as follows:

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$$DA_0 = OFF + S_0 \cdot \frac{DN_{15,pre} + DN_0}{2}$$

$$DA_{2k} = OFF + S_l \cdot \frac{DN_{k-1} + DN_k}{2}, k = 1,...,15$$

$$DA_{2k+1} = OFF + S_l \cdot DN_k, k = 0,1,...,15$$

$$l = \begin{cases} 0, & \text{if } 8 > k \geq 0 \\ 1, & \text{if } 15 \geq k \geq 8 \end{cases}$$

where **DA** = the data to present to the D/A converter,
DN = the normalized data which is stored in the register **APC_PF*n***,
S_0 = the left scaling factor stored in register **APC_SCAL*n*L**,
S_1 = the right scaling factor stored in register **APC_SCAL*n*R**, and
OFF = the offset value stored in the register **APC_OFFSET*n***.

The subscript ***n*** denotes the index of the ramp profile.

The ramp calculation before interpolation is as depicted in **Figure 91**.

During each ramp process, each word of the normalized profile is first multiplied by 10-bit scaling factors and added to an offset value to form a bank of 18-bit words. The first 8 words (in the left half part as in **Figure 91**) are multiplied by the left scaling factor **S_0** and the last 8 words (in the right half part as in **Figure 91**) are multiplied by the right scaling factor **S_1**. The lowest 8 bits of each word are then truncated to get a 10-bit result. The scaling factor is 0x100, which represents no scaling on reset. A value smaller than 0x100 scales the ramp profile down, and a value larger than 100 scales the ramp profile up.

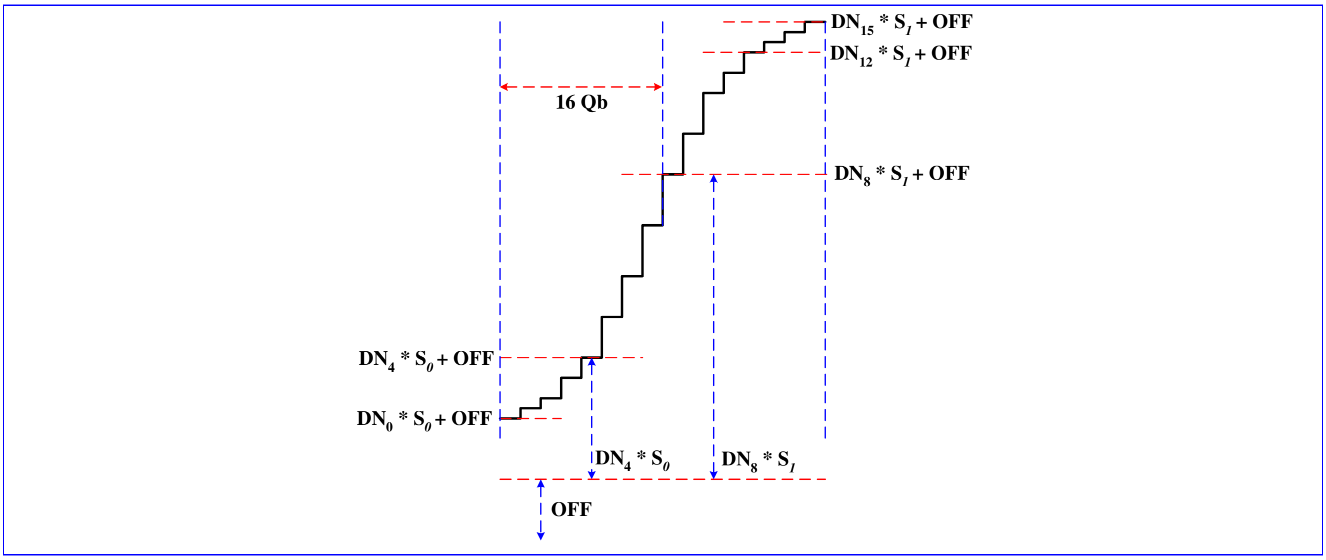

Figure 91 The timing diagram of the APC ramp

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The 16 10-bit words are linearly interpolated into 32 10-bit words. A 10-bit D/A converter is then used to convert these 32 ramp values at a rate of 1.0833 MHz, that is, at quarter-bit rate. The timing diagram is shown in **Figure 92** and the final value is retained on the output until the next event occurs.

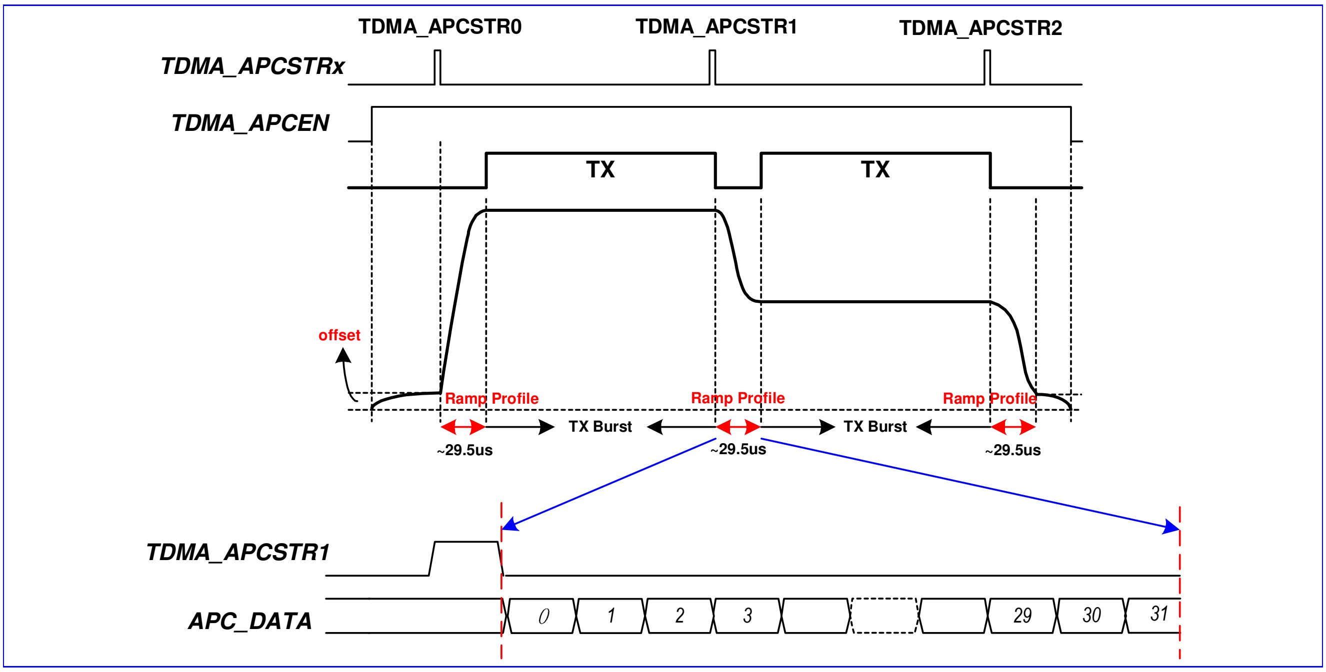

Figure 92 Timing diagram of the APC ramping

The APC unit is only powered up when the APC window is open. The APC window is controlled by configuring the TDMA registers TDMA_BULCON1 and TDMA_BULCON2. Please refer to the TDMA timer unit for more detailed information.

The first offset value stored in the register APC_OFFSET0 also serves as the pedestal value, which is used to provide the initial power level for the PA.

Since the profile is not double-buffered, the timing to write the ramping profile is critical. The programmer must be restricted from writing to the data buffer during the ramping process, otherwise the ramp profile may be incorrect and lead to a malfunction.

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9 Baseband Front End

Baseband Front End is a modem interface between TX/RX mixed-signal modules and digital signal processor (DSP). We can divide this block into two parts (see **Figure 93**). The first is the uplink (transmitting) path, which converts bit-stream from DSP into digital in-phase (I) and quadrature (Q) signals for TX mixed-signal module. The second part is the downlink (receiving) path, which receives digital in-phase (I) and quadrature (Q) signals from RX mixed-signal module, performs FIR filtering and then sends results to DSP. **Figure 93** illustrates interconnection around Baseband Front End. In the figure the shadowed blocks compose Baseband Front End.

The uplink path is mainly composed of GMSK Modulator and uplink parts of Baseband Serial Ports, and the downlink path is mainly composed of RX digital FIR filter, RX interference detection filter (ITD) including power measurement blocks, downlink parts of Baseband Serial Ports and DSP I/O. Baseband Serial Ports is a serial interface used to communicate with DSP. In addition, there is a set of control registers in Baseband Front End that is intended for control of TX/RX mixed-signal modules, inclusive of several compensation circuit: calibration of I/Q DC offset, I/Q Quadrature Phase Compensation and I/Q Gain Mismatch of uplink analog-to-digital (D/A) converters as well as I/Q Gain Mismatch for downlink digital-to-analog (A/D) converters in TX/RX mixed-signal modules. The timing of bit streaming through Baseband Front End is completely under control of TDMA timer. Usually only either of uplink and downlink paths is active at one moment. However, both of the uplink and downlink paths will be active simultaneously when Baseband Front End is in loopback mode.

When either of TX windows in TDMA timer is opened, the uplink path in Baseband Front End will be activated. Accordingly components on the uplink path such as GMSK Modulator will be powered on, and then TX mixed-signal module is also powered on. The sub-block Baseband Serial Ports will sink TX data bits from DSP and then forward them to GMSK Modulator. The outputs from GMSK Modulator are sent to TX mixed-signal module in format of I/Q signals. Finally D/A conversions are performed in TX mixed-signal module and the output analog signal is output to RF module.

Similarly, while either of RX windows in TDMA timer is opened, the downlink path in Baseband Front End will be activated. Accordingly components on the downlink path such as RX mixed-signal module and RX digital FIR filter are then powered on. First A/D conversions are performed in RX mixed-signal module, and then the results in format of I/Q signals are sourced to Low Pass Filtering with different bandwidth (Narrow one about F_C = 90 kHz, Wide one about F_C = 110khz), Interference Detection Circuit to determine which Filter to be used by judging receiving power on current burst. Additionally, “I/Q Compensation Circuit” is an option in data path for modifying Receiving I/Q pair gain mismatch. Finally the results will be sourced to DSP through Baseband Serial Ports.

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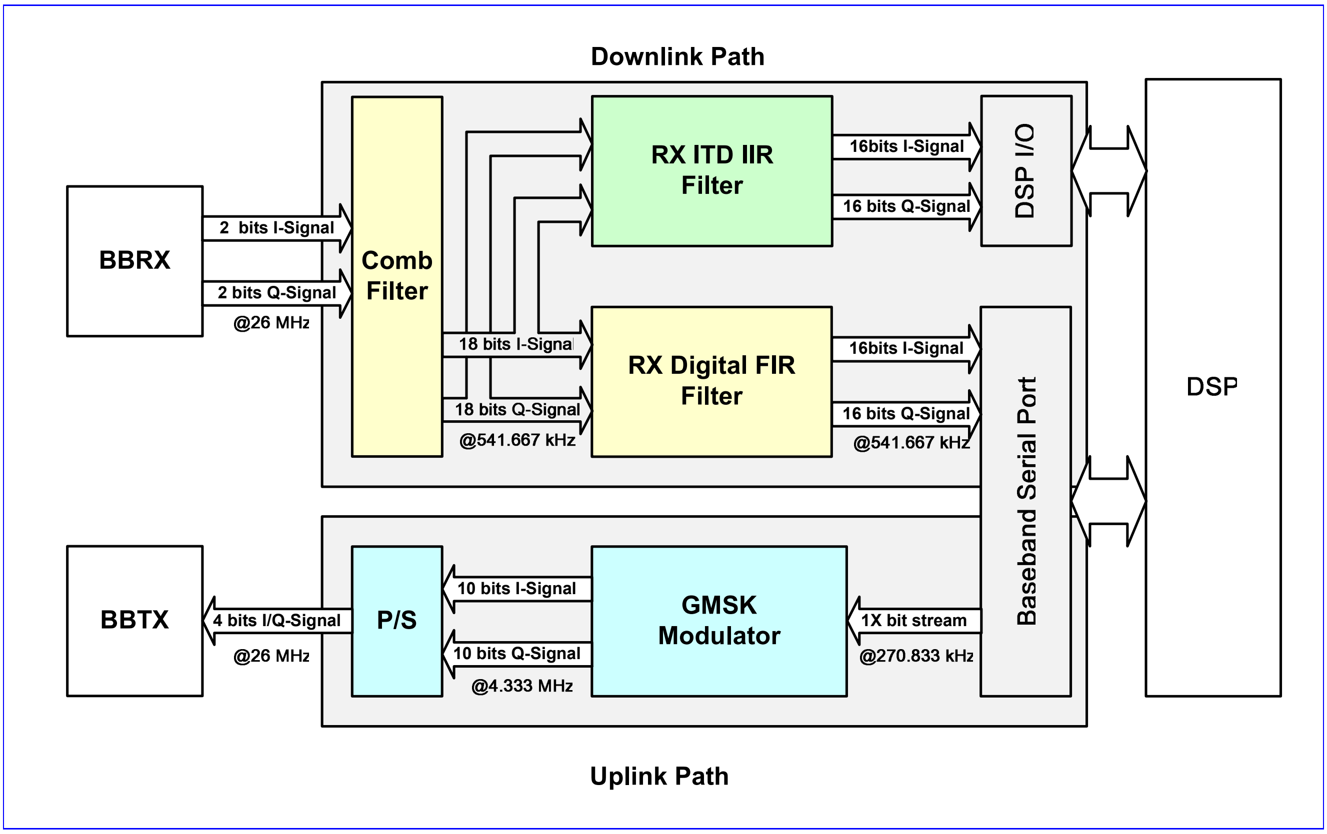

Figure 93 Block Diagram of Baseband Front End

9.1 Baseband Serial Ports

9.1.1 General Description

Baseband Front End communicates with DSP through the sub block of Baseband Serial Ports. Baseband Serial Ports interfaces with DSP in serial manner. This implies that DSP must be configured carefully in order to have Baseband Serial Ports cooperate with DSP core correctly.

If downlink path is programmed in bypass-filter mode (**NOT** bypass-filter loopback mode), behavior of Baseband Serial Ports will be completely be different from that in normal function mode. The special mode is for testing purpose. Please see the subsequent section of Downlink Path for more details.

TX and RX windows are under control of TDMA timer. Please refer to functional specification of TDMA timer for the details on how to open/close a TX/RX window. Opening/Closing of TX/RX windows have two major effects on Baseband Front End: power on/off of corresponding components and data souring/sinking. It is worth noticing that Baseband Serial Ports is only intended for sinking TX data from DSP or sourcing data to DSP. It does not involve power on/off of TX/RX mixed-signal modules.

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As far as downlink path is concerned, if a RX window is opened by TDMA timer Baseband Front End will have RX mixed-signal module proceed to make A/D conversion, two parallel RX digital filter proceed to perform filtering and Baseband Serial Ports be activated to source data from RX digital filter to Master DSP while Power Measurement through DSP I/O to DSP no matter the data is meaningful or not. However, the interval between the moment that RX mixed-signal module is powered on and the moment that data proceed to be dumped by Baseband Serial Ports can be well controlled in TDMA timer. Let us denote RX enable window as the interval that RX mixed-signal module is powered on and denote RX dump window as the interval that data is dumped by Baseband Serial Ports. If the first samples from RX digital filter desire to be discarded, the corresponding RX enable window must cover the corresponding RX dump window. Note that RX dump windows always win over RX enable windows. It means that a RX dump window will always raise a RX enable window. RX enable windows can be raised by TDMA timer or by programming RX power-down bit in global control registers to be ‘0’. This is useful in debugging environment.

Similarly, a TX dump window refers to the interval that Baseband Serial Ports sinks data from DSP on uplink path and a TX enable window refers to the interval that TX mixed-signal module is powered on. A TX window controlled by TDMA timer involves a TX dump window and a TX enable window simultaneously. The interval between the moment that TX mixed-signal module is powered on and the moment that data proceed to be forwarded from DSP to GMSK or 8PSK modulator by Baseband Serial Ports can be well controlled in TDMA timer. TX dump windows always win over TX enable windows. It means that a TX dump window will always raise a TX enable window. TX enable windows can be raised by TDMA timer or by programming TX power-down bit in global control registers to be ‘0’. It is useful in debugging environment.

Accordingly, Baseband Serial Ports are only under the control of TX/RX dump window. Note that if TX/RX dump window is not integer multiples of bit-time it will be extended to be integer multiples of bit-time. For example, if TX/RX dump window has interval of 156.25 bit-times then it will be extended to 157 bit-times in Baseband Serial Ports.

For uplink path, if uplink path is enabled, then the bit BULEN (Baseband Up-Link Enable) will be ‘1’. Otherwise the bit BULEN will be 0.

For downlink path, if BDLEN (Baseband DownLink Enable) is enabled, RX mixed-signal module will also be powered on. Similarly, once uplink path is enabled, TX mixed-signal module will also be powered on. Furthermore, enabling BDLFS (Baseband Down-Link FrameSync) Baseband Serial Ports for downlink path refers to dumping results from RX digital FIR filter to DSP.

9.1.2 Register Definitions

0x8210_0000 Base-band Common Control Register BFE_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BCIEN
Type																R/W
Reset																0

This register is for common control of Baseband Front End. It consists of ciphering encryption control.

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BCIEN The bit is for ciphering encryption control. If the bit is set to '1', XOR will be performed on some TX bits (payload of Normal Burst) and ciphering pattern bit from DSP, and then the result is forwarded to GMSK Modulator only. Meanwhile, Baseband Front End will generate signals to drive DSP ciphering process and produce corresponding ciphering pattern bits if the bit is set to '1'. If the bit is set to '0', the TX bit from DSP will be forwarded to GMSK modulator directly. Baseband Front End will not activate DSP ciphering process.

- **0** Disable ciphering encryption.
- **1** Enable ciphering encryption.

0x8210_0004 Base-band Common Status Register BFE_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							BULEN4	BULEN3	BULEN2	BULEN1	BULFS4	BULFS3	BULFS2	BULFS1	BDLFS	BDLEN
Type							RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset							0	0	0	0	0	0	0	0	0	0

This register indicates status of Baseband Front End. Under control of TDMA timer, Baseband Front End can be driven in several statuses. If downlink path is enabled, then the bit BDLEN will be '1'. Otherwise the bit BDLEN will be '0'. If downlink parts of Baseband Serial Ports is enabled, the bit BDLFS will be '1'. Otherwise the bit BDLFS will be '0'. If uplink path is enabled, then the bit BULEN will be '1'. Otherwise the bit BULEN will be 0. If uplink parts of Baseband Serial Ports is enabled, the bit BULFS will be '1'. Otherwise the bit BULFS will be '0'. Once downlink path is enabled, RX mixed-signal module will also be powered on. Similarly, once uplink path is enabled, TX mixed-signal module will also be powered on. Furthermore, enabling Baseband Serial Ports for downlink path refers to dumping results from RX digital FIR filter to DSP. Similarly, enabling Baseband Serial Ports for uplink path refers to forwarding TX bit from DSP to GMSK modulator. BDLEN stands for "**B**aseband **D**own**L**ink **EN**able". BULEN stands for "**B**aseband **U**p**L**ink **EN**able". BDLFS stands for "**B**aseband **D**own**L**ink **F**rame**S**ync". BULFS stands for "**B**aseband **U**p**L**ink **F**rame**S**ync".

BDLEN Indicate if downlink path is enabled.

- **0** Disabled
- **1** Enabled

BDLFS Indicate if Baseband Serial Ports for downlink path is enabled.

- **0** Disabled
- **1** Enabled

BULFS1 Indicate if Baseband Serial Ports for uplink path is enabled in 1st burst

- **0** Disabled
- **1** Enabled

BULFS2 Indicate if Baseband Serial Ports for uplink path is enabled in 2nd burst

- **0** Disabled
- **1** Enabled

BULFS3 Indicate if Baseband Serial Ports for uplink path is enabled in 3rd burst

- **0** Disabled
- **1** Enabled

BULFS4 Indicate if Baseband Serial Ports for uplink path is enabled in 4th burst

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0 Disabled
1 Enabled
BULEN1 Indicate if uplink path is enabled in 1st burst.
0 Disabled
1 Enabled
BULEN2 Indicate if uplink path is enabled in 2nd burst.
0 Disabled
1 Enabled
BULEN3 Indicate if uplink path is enabled in 3rd burst.
0 Disabled
1 Enabled
BULEN4 Indicate if uplink path is enabled in 4th burst.
0 Disabled
1 Enabled

9.2 Downlink Path (RX Path)

9.2.1 General Description

On the downlink path, the sub-block between RX mixed-signal module and Baseband Serial Ports is RX Path. It mainly consists of two parallel digital FIR filter with programmable tap number, two sets of multiplexing paths for loopback modes, interface for RX mixed-signal module, Interference Detection Circuit, I/Q Gain Mismatch compensation circuit, and interface for Baseband Serial Ports. The block diagram is shown in **Figure 94**.

While RX enable windows are open, RX Path will issue control signals to have RX mixed-signal module proceed to make A/D conversion. As each conversion is finished, one set of I/Q signals will be latched. There exists a digital FIR filter for these I/Q signals. The result of filtering will be dumped to Baseband Serial Ports whenever RX dump windows are opened.

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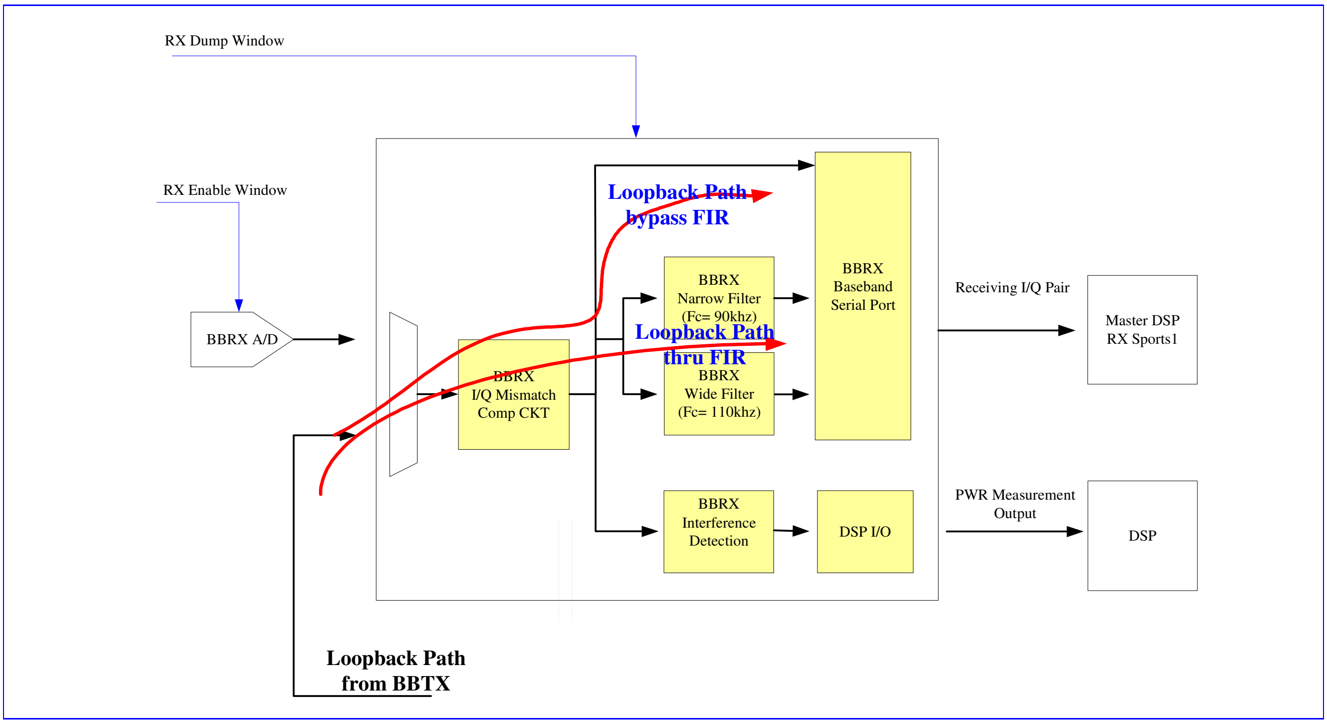

Figure 94 Block diagram of RX path

9.2.2 Comb Filter

The comb filter which takes the 2-bit A/D converter as input, and output the 18-bit I/Q data words to the baseband receiving path. The system is designed as 48X over-sampling with symbol period 541.7 kHz, thus the data inputs are 26MHz 2-bit signal. The input 2-bit signals are formed in (sign, magnitude) manner; that is, total 3 values are permitted as input: (-1, 0, +1).

The data path is mainly a decimation filter which contains the integration stages and the decimation stages. For a 3rd order design with 48X over-sampling, gain of the data path is 48^3 = 110592, which locates between 2^{16} and 2^{17}. Thus the internal word-length must be set to 18-bit to avoid overflow in the integration process.

9.2.3 Compensation Circuit - I/Q Gain Mismatch

In order to compensate I/Q Gain Mismatch , configure IGAINSEL(I Gain Selection) in RX_CON control register, the I over Q ratio can be compensate for 0.3 dB/step, totally 11 steps resulted in dynamic range up to +/-1.5dB.

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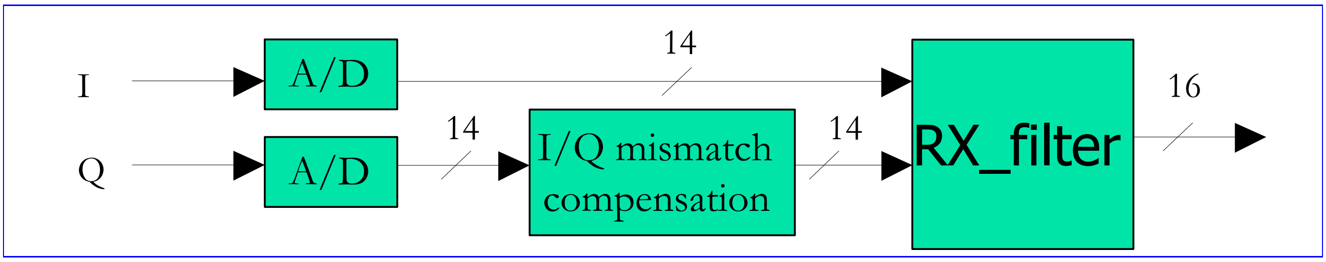

Figure 95 I/Q Mismatch Compensation Block Diagram

The I/Q swap functionality can be setting "1" for SWAP(I/Q Swapping) in RX_CFG control register, which is used to swap I/Q channel signals from RX mixed-signal module before they are latched into RX digital FIR filter. It is intended to provide flexibility for I/Q connection with RF modules

9.2.4 Phase De-rotation Circuit

Phase De-rotation Mode will usually turn on during FCB Detection for down conversion the wide spread receiving power to 67.7 kHz single tone.

Two separate control for implement this mode on data path through NarrowFIR filter or WideFIR filter by setting '1' to PHROEN_N (Phase Rotate Enable for NarrowFIR) or PHROEN_W(Phase Rotate Enable for WideFIR) in RX_CON control register, respectively.

9.2.5 Adaptive Bandwidth & Programmable Digital FIR Filter

For the two parallel digital FIR Filter, the total tap number is programmable by FIRTPNO(FIR Tap number) in RX_CFG control register, which will configure the filter with different tap buffer depth.

9.2.5.1 Programmable tap & programmable Coefficient for FIR

In order to satisfy the signal requirements in both of idle and traffic modes, two sets of coefficients must be provided for the RX digital FIR filter. Therefore, the RX digital FIR filter is implemented as a FIR filter with programmable coefficients which can be accessed on the APB bus. The coefficient number can be programmable, range from 1~31. Each coefficient is ten-bit wide and coded in 2's complement.

Take 21 Tap Coefficient for example, based on assumption that the FIR filter has symmetric coefficients, only 11 coefficients are implemented as programmable registers to save gate count. Denoting these digital filter coefficients as RX_RAM0_CS0 ~ RX_RAM0_CS11(RX_RAM0 Coefficient Set 0~11), and these tap registers for I/Q channel signals as I/QTAPR [0:20], then the RX digital FIR filtering can be represented as the following equation:

$$I_{out}(m) = \sum_{i=0}^{20} BDLDFCR[i] * ITAPR[i] \Big|_{\text{at time } n+4m} = BDLDFCR[11] * ITAPR[11] + \sum_{i=0}^{11} BDLDFCR[i] * (ITAPR[i] + ITAPR[20-i]) \Big|$$

$$Q_{out}(m) = \sum_{i=0}^{20} BDLDFCR[i] * QTAPR[i] \Big|_{\text{at time } n+4m} = BDLDFCR[11] * QTAPR[11] + \sum_{i=0}^{11} BDLDFCR[i] * (QTAPR[i] + QTAPR[20-i]) \Big|$$

$$BDLDFCR[i] = BDLDFCR[20-i], i = 0,1,...,11$$

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where ITAPR [0] and QTAPR [0] are the latest samples for I- and Q-channel respectively and assume $I_{out}(0), Q_{out}(0)$ are obtained based on the content of tap registers at time moment n. From the equation above it follows that the digital RX FIR filter will produce one output every four data conversions out of A/D converters. That is, filtering and decimation are performed simultaneously to achieve low power design.

However, different "Coefficient Set ID"(CS ID) will be dump to Slave DSP RX buffer to represent the current selecting of coefficient Set from either 2 ROM table or 2 set of programmable RAM table according to different burst mode, while ROM table are fixed coefficient and RAM table can be programmed through 2set of 16 control register (RX_RAM0_CS0~ RX_RAM_CS15, (RX_RAM1_CS0~RX_RAM1_CS15). Generally, CSID = 0 represent ROM table selection, while CSID 2~ CSID 15 represent RAM table selection. Please be noted that the total coefficient number in a RAM table should be greater than half of the FIRTPNO (total FIR Tap number) and smaller than half of maximum tap number (15) since the FIR function in symmetric behavior.

Additionally, the data sequence of two parallel FIR filter output will dump to Master DSP RX buffer in following order : "I channel output from Narrow FIR"=> " I channel output from Wide FIR""=>"Q channel output from Narrow FIR=>" Q channel output from Wide FIR.

9.2.5.1.1 Coefficient Set Selection

The Coefficient Set used for digital FIR can be changed during different burst mode switching. For example, during Normal Burst while no FB_STROBE (Frequency Burst Strobe, comes from TDMA controller) assertion, defined as "State B", "Coefficient Set ID" (CSID) selection for both Narrow/Wide filter can be configured by ST_B_WCOF_SEL (State B Wide FIR Coefficient Selection) and "ST_B_NCOF_SEL" (State B Narrow FIR Coefficient Selection) on RX_FIR_CSID_CON control register, respectively. Usually during State B, Layer 1 software will select RAM table coefficient from either RAM0 or RAM1 table in condition I for Narrow FIR and Wide FIR, respectively. The CS ID for both Narrow / Wide FIR filter be stored at Slave DSP RX buffer once TDMA trigger RX interrupt to DSP..ST_A_NCOF_SEL" (State A Narrow FIR Coefficient Selection) on RX_FIR_CSID_CON control register.

During FCB detection, MCU will notice TDMA controller by assertion FB_STROBE, defined as "StateA". "Coefficient Set ID" (CS ID) selection for both Narrow/Wide filter can be configured by ST_A_WCOF_SEL(State A Wide FIR Coefficient Selection) and "ST_A_NCOF_SEL" (State A Narrow FIR Coefficient Selection) on RX_FIR_CSID_CON control register, respectively. Usually during State B, Layer 1 software will select CS ID 2 and CSID 3 from either ROM0 or ROM1 table or RAM0 or RAM1 table in Condition II for Narrow FIR and Wide FIR, respectively.

9.2.5.2 Interference Detection Circuit for Adaptive Bandwidth Scheme

Used to compare the power of Co-channel Interference and Adjacent-channel Interference for determine if WideFIR filter is needed rather than default NarrowFIR filter. Two parallel path of power measurement for evaluating Co-channel effect or Adjacent Channel Effect by analyzing power after High Pass Filter (HPF) or Band Pass Filter (BPF), respectively. If Co-channel effect is worse than Adjacent Channel effect, WideFIR filter is needed.

The power measurement is accumulate I/Q Root Mean Square (RMS) power over the whole RX burst window, while exact accumulation period within the burst can be adjusted the starting point offset and duration length.. The "starting point Offset" and be configured by "RXID_PWR_OFF[7:0]" (RX Interference Detection Power Starting Point Offset) and

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duration period by " RXID_PWR_PER[7:0]"(RX Interference Detection Power Duration Period) in RX_PM_CON control register, while default value for starting offset is 11 and duration period is 141. The two accumulated power measurement output for Co-channel and Adjacent-channel will be dump to Slave DSP RX buffer alternatively at the end of the duration period within a burst. However, if the duration period is longer than the RX Dump Window, the accumulated measurement output will be dump out at falling edge of RX_DUMP_Window rather than the end of configured duration period.

Additionally, the power measurement data sequence at Slave DSP RX buffer will be "Coefficient Set ID for NarrowFIR filter"=> "Coefficient Set ID for WideFIR filter"=>"Power output of HPF(Co-channel)=>"Power output of BPF(Adjacent-channel), while the coefficient Set ID (CSID) is for DSP debug purpose.

The power result can be further scale down by control the PWR_SHFT_NO (power right Shift Number) in RX_CON control register. E.g. set to "1" will divide the power output by two.

9.2.5.3 Supporting Single Filter 2X symbol rate Mode

The two parallel FIR filter default output data rate in 1x Symbol rate after 2X decimation. but by programming 2XFIRSEL(2x Symbol Rate FIR Selection) in RX_CFG control register, WideFIR filter will be disable, while NarrowFIR filter will output data rate in 2X symbol rate without 2x decimation.

9.2.6 Debug Mode

9.2.6.1 Normal Mode bypass Filter

By setting "1" for BYPFLTR(Bypass Filter) in RX_CFG control register, the ADC outputs out of RX mixed-signal module will be directed into Baseband Serial Ports directly without through FIR. Limited by bandwidth of the serial interface between Baseband Serial Ports and DSP, only ADC outputs which are from either I-channel or Q-channel ADC can be dumped into DSP. Both I- and Q-channel ADC outputs cannot be dumped simultaneously. Which channel will be dumped is controlled by the register bit SWAP of the control register RX_CFG when downlink path is programmed in "Bypass RX digital FIR filter" mode. See register definition below for more details. The mode is for measurement of performance of A/D converters in RX mixed-signal module.

9.2.6.2 TX-RX Digital Loopback Mode (Debug Mode)

In addition to normal function, there are two loopback modes in RX Path. One is bypass-filter loopback mode, and the other is through-filter loopback mode. They are intended for verification of DSP firmware and hardware. The bypass-filter loopback mode refers to that RX digital FIR filter is not on the loopback path. However, the through-filter loopback mode refers to that RX digital FIR filter is on the loopback path, while " thru-Filter Loopback Mode" can be configured by setting "2'b10" for BLPEN(Baseband Loopback Enable) or "bypass-Filter Loopback Mode" by setting " 2'b01" for BLPEN in RX_CON control register.

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9.2.7 Register Definitions

9.2.7.1 APB Register

0x8210_0010 RX Configuration Register RX_CFG

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							FIRTPNO							2XFIRSEL	BYPFLTR	SWAP
Type							R/W							R/W	R/W	R/W
Reset							000000							0	0	0

This register is for configuration of downlink path, inclusive of configuration of RX mixed-signal module and RX path in Baseband Front End.

SWAP This register bit is for control of whether I/Q channel signals need to swap before they are inputted to Baseband Front End. It provides flexibility flexible of connection of I/Q channel signals between RF module and baseband module. The register bit has another purpose when the register bit "BYPFLTR" is set to 1. Please see description for the register bit "BYPFLTR".

- **0** I- and Q-channel signals are not swapped
- **1** I- and Q-channel signals are swapped

BYPFLTR Bypass RX FIR Filter control. The register bit is used to configure Baseband Front End in the state called "Bypass RX FIR filter state" or not. Once the bit is set to '1', RX FIR filter will be bypassed. That is, ADC outputs of RX mixed-signal module that are has 14-bit resolution and at sampling rate of 541kHz can be dumped into DSP by Baseband Serial Ports and RX FIR filtering will not be performed on them.

- **0** Not bypass RX FIR filter
- **1** Bypass RX FIR filter

2XFIRSEL Enable for single FIR w/ output data rate in 2x Symbol rate output Enable. This mode will disable WideFIR, while Narrow FIR w/ 2x symbol rate without 2x decimation.

- **0** Disable Single FIR 2X symbol rate output mode.
- **1** Enable Single FIR 2X symbol rate output mode.

FIRTPNO RX FIR filter tap no. select. This control register will control the two parallel digital filter with different tap buffer depth since the FIR function in symmetric behavior. The maximum tap number is 31, minimum is 1., ODD number only.

0x8210_0014 RX Control Register RX_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PWR_SHFT_NO				IGAINSEL				PH_ROEN_N	PH_ROEN_W	BLPEN	
Type					R/W				R/W				R/W	R/W	R/W	
Reset					0000				0000				0	0	00	

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This register is for control of downlink path, inclusive of control of RX mixed-signal module and RX path in Baseband Front End module.

BLPEN The register field is for loopback configuration selection in Baseband Front End.

- **00** Configure Baseband Front End in normal function mode
- **01** Configure Baseband Front End in bypass-filter loopback mode
- **10** Configure Baseband Front End in through-filter loopback mode
- **11** Reserved

PH_ROEN_W Enable for I/Q pair Phase De-rotation in Wide FIR Data Path.

- **0** Disable Phase De-rotation for I/Q pair.
- **1** Enable Phase De-rotation for I/Q pair.

PH_ROEN_N Enable for I/Q pair Phase De-rotation in Narrow FIR Data Path.

- **0** Disable Phase De-rotation for I/Q pair.
- **1** Enable Phase De-rotation for I/Q pair.

IGAINSEL RX I data Gain Compensation Select. 0.3dB/step, totally 11 steps and dynamic range up to +/-1.5dB for

- **0000** compensate 0dB for I/Q
- **0001** compensate 0.3dB for I/Q
- **0010** compensate 0.6dB for I/Q
- **0011** compensate 0.9dB for I/Q
- **0100** compensate 1.2dB for I/Q
- **0101** compensate 1.5dB for I/Q
- **1001** compensate –0.3dB for I/Q
- **1010** compensate -0.6dB for I/Q
- **1011** compensate –0.9dB for I/Q
- **1100** compensate –1.2dB for I/Q
- **1101** compensate –1.5dB for I/Q
- **Default** No compensation for I/Q

PWR_SHFT_NO Power measuring Result Right Shift Number. The Power level measurement result can be right shift from 0 to 16 bits.

0x8210_0018 RX Interference Detection Power Measurement Control Register RX_PM_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXID_PWR_PER								RXID_PWR_OFF							
Type	R/W								R/W							
Reset	8D								B							

RXID_PWR_OFF RX Interference Detection Power Measurement Starting Offset. Setting this register will delay the starting time of Interference Detection Power Measurement in symbol time unit. Maximum value is 156, while default value is 11 (0xB).

RXID_PWR_PER RX Interference Detection Power Measurement Accumulation Period. By setting this control register will determine the length of accumulation duration for power Measurement. Minimum value is 0,

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Maximum value is 156, while default value is 141(0x8D). Please notice that RXID_PWR_OFF + RXID_PWR_PER should less than 154 due to hardware implementation limitation.

0x8210_001C RX FIR Coefficient Set ID Control Register RX_FIR_CSID_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_A_NCOF_SEL								ST_B_NCOF_SEL				ST_B_WCOF_SEL			
Type	R/W								R/W				R/W			
Reset	0000								0010				0011			

These three set of Coefficient Set ID will be dump to slave DSP RX Buffer for indicating the current selection of FIR coefficient from either RAM or ROM table, while CSID= 0 represents ROM table selection, and CSID2~CSID15 represent RAM table selection.

ST_B_WCOF_SEL State B Coefficient Set Selection for Wide FIR.

ST_B_NCOF_SEL State B Coefficient Set Selection for Narrow FIR.

ST_A_NCOF_SEL State A Coefficient Set Selection for Narrow FIR.

0x8210_0070 RX RAM0Coefficient Set 0Register RX_RAM0_CS0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RX_RAM0_CS0									
Type							R/W									
Reset							000000000									

This register is 1st of the 16 coefficient in RAM0 table, Coefficient Set ID 2 or 4. The content is coded in 2's complement. That is, its maximum is 255 and its minimum is –256, while the total coefficient number in this Coefficient Set has to be greater than half of TAPNO(programmable Tap no.) and smaller than half of maximum tap no(15).

Register Address	Register Function	Acronym
0x8210_0070h	RX RAM0Coefficient Set 0 Register	RX_RAM0_CS0
0x8210_0074h	RX RAM0Coefficient Set 1 Register	RX_RAM0_CS1
0x8210_0078h	RX RAM0Coefficient Set 2 Register	RX_RAM0_CS2
0x8210_007Ch	RX RAM0Coefficient Set 3 Register	RX_RAM0_CS3
0x8210_0080h	RX RAM0Coefficient Set 4 Register	RX_RAM0_CS 4
0x8210_0084h	RX RAM0Coefficient Set 5 Register	RX_RAM0_CS 5
0x8210_0088h	RX RAM0Coefficient Set 6 Register	RX_RAM0_CS 6
0x8210_008Ch	RX RAM0Coefficient Set 7 Register	RX_RAM0_CS 7
0x8210_0090h	RX RAM0Coefficient Set 8 Register	RX_RAM0_CS 8
0x8210_0094h	RX RAM0Coefficient Set 9 Register	RX_RAM0_CS 9
0x8210_0098h	RX RAM0Coefficient Set 10 Register	RX_RAM0_CS 10
0x8210_009Ch	RX RAM0Coefficient Set 11Register	RX_RAM0_CS 11
0x8210_00a0h	RX RAM0Coefficient Set 12Register	RX_RAM0_CS 12
0x8210_00a4h	RX RAM0Coefficient Set 13Register	RX_RAM0_CS 13
0x8210_00a8h	RX RAM0Coefficient Set 14 Register	RX_RAM0_CS 14

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0x8210_00aCh	RX RAM0Coefficient Set 15 Register	RX_RAM0_CS 15

0x8210_0020 RX RAM1 Coefficient Set 0 Register RX_RAM1_CS 0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RX_RAM1_CS 0									
Type							R/W									
Reset							000000000									

This register is 1st of the 16 coefficient in RAM1 table, Coefficient Set ID 2 or 4. The content is coded in 2's complement. That is, its maximum is 255 and its minimum is –256, while the total coefficient number in this Coefficient Set has to be greater than half of TAPNO(programmable Tap no.) and smaller than half of maximum tap no(15).

Register Address	Register Function	Acronym
0x8210_0020h	RX RAM1 Coefficient Set 0 Register	RX_RAM1_CS 0
0x8210_0024h	RX RAM1 Coefficient Set 1Register	RX_RAM1_CS 1
0x8210_0028h	RX RAM1 Coefficient Set 2 Register	RX_RAM1_CS 2
0x8210_002Ch	RX RAM1 Coefficient Set 3 Register	RX_RAM1_CS 3
0x8210_0030h	RX RAM1 Coefficient Set 4 Register	RX_RAM1_CS 4
0x8210_0034h	RX RAM1 Coefficient Set 5 Register	RX_RAM1_CS 5
0x8210_0038h	RX RAM1 Coefficient Set 6 Register	RX_RAM1_CS 6
0x8210_003Ch	RX RAM1 Coefficient Set 7 Register	RX_RAM1_CS 7
0x8210_0040h	RX RAM1 Coefficient Set 8 Register	RX_RAM1_CS 8
0x8210_0044h	RX RAM1 Coefficient Set 9 Register	RX_RAM1_CS 9
0x8210_0048h	RX RAM1 Coefficient Set 10 Register	RX_RAM1_CS 10
0x8210_004Ch	RX RAM1 Coefficient Set 11 Register	RX_RAM1_CS 11
0x8210_0050h	RX RAM1 Coefficient Set 12 Register	RX_RAM1_CS 12
0x8210_0054h	RX RAM1 Coefficient Set 13 Register	RX_RAM1_CS 13
0x8210_0058h	RX RAM1 Coefficient Set 14 Register	RX_RAM1_CS 14
0x8210_005Ch	RX RAM1 Coefficient Set 15 Register	RX_RAM1_CS 15

0x8210_00B0 RX Interference Detection HPF Power Register RX_HPWR_STS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PWR_HPF															
Type	R/O															
Reset	0000000000000000															

This register is for read the power measurement result of the HPF interference detection filter.

RX_PWR_HPF Value of the power measurement result for the outband interference detection.

0x8210_00B4 RX Interference Detection BPF Power Register RX_BPWR_STS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	RX_PWR_BPF
Type	R/O
Reset	0000000000000000

This register is for read the power measurement result of the BPF interference detection filter.

RX_PWR_BPF Value of the power measurement result for the inband interference detection

9.2.7.2 DSP I/O Register

0x743h RX HPF ITD Power Register of Window0 DSPIO_ITD_H_0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ITD_H_DATA_0															
Type	R/O															
Reset	0000000000000000															

This register is for **DSP** to read the power measurement result of the BPF interference detection filter through DSP I/O.

DSPIO_ITD_H_0 Value of the power measurement result for the outband interference detection of window 0.

Register Address	Register Function	Acronym
0x743h	RX HPF ITD Power Register of Window0	DSPIO_ITD_H_0
0x747h	RX HPF ITD Power Register of Window1	DSPIO_ITD_H_1
0x74Bh	RX HPF ITD Power Register of Window2	DSPIO_ITD_H_2
0x74Fh	RX HPF ITD Power Register of Window3	DSPIO_ITD_H_3
0x753h	RX HPF ITD Power Register of Window4	DSPIO_ITD_H_4
0x757h	RX HPF ITD Power Register of Window5	DSPIO_ITD_H_5

0x744h RX BPF ITD Power Register of Window0 DSPIO_ITD_B_0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ITD_B_DATA_0															
Type	R/O															
Reset	0000000000000000															

This register is for **DSP** to read the power measurement result of the BPF interference detection filter through DSP I/O.

DSPIO_ITD_B_0 Value of the power measurement result for the inband interference detection of window 0.

Register Address	Register Function	Acronym
0x744h	RX BPF ITD Power Register of Window0	DSPIO_ITD_B_0
0x748h	RX BPF ITD Power Register of Window1	DSPIO_ITD_B_1
0x74Ch	RX BPF ITD Power Register of Window2	DSPIO_ITD_B_2
0x750h	RX BPF ITD Power Register of Window3	DSPIO_ITD_B_3
0x754h	RX BPF ITD Power Register of Window4	DSPIO_ITD_B_4
0x758h	RX BPF ITD Power Register of Window5	DSPIO_ITD_B_5

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0x759h RX ITD Power Measurement Ready Flag DSPIO_RXID_RDY

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RXID_RDY_5	RXID_RDY_4	RXID_RDY_3	RXID_RDY_2	RXID_RDY_1	RXID_RDY_0
Type											R/O	R/O	R/O	R/O	R/O	R/O
Reset											0	0	0	0	0	0

This register is for **DSP** to see whether the RX ITD power register is ready or not through DSP I/O. When the DSPIO_ITD_H_0 and DSPIO_ITD_B_0 are ready, bit 0 is set to 1. Moreover, while DSP read the data of DSPIO_ITD_H_0 and DSPIO_ITD_B_0, bit 0 is reset to 0.

RXID_RDY_0 Ready flag for DSP to read the ITD power measurement result of window0.
RXID_RDY_1 Ready flag for DSP to read the ITD power measurement result of window1.
RXID_RDY_2 Ready flag for DSP to read the ITD power measurement result of window2.
RXID_RDY_3 Ready flag for DSP to read the ITD power measurement result of window3.
RXID_RDY_4 Ready flag for DSP to read the ITD power measurement result of window4.
RXID_RDY_5 Ready flag for DSP to read the ITD power measurement result of window5.

9.3 Uplink Path (TX Path)

9.3.1 General Description

The purpose of the uplink path inside Baseband Front End is to sink TX symbols, from DSP, then perform GMSK modulation on them, then perform offset cancellation on I/Q digital signals, and finally control TX mixed-signal module to make D/A conversion on I/Q signals out of GMSK Modulator with offset cancellation. Accordingly, the uplink path is composed of uplink parts of Baseband Serial Ports, GSM Encryptor, GMSK Modulator and several compensation circuits including I/Q DC offset, I/Q Quadrature Phase Compensation, and I/Q Gain Mismatch. The block diagram of uplink path is shown as followed.

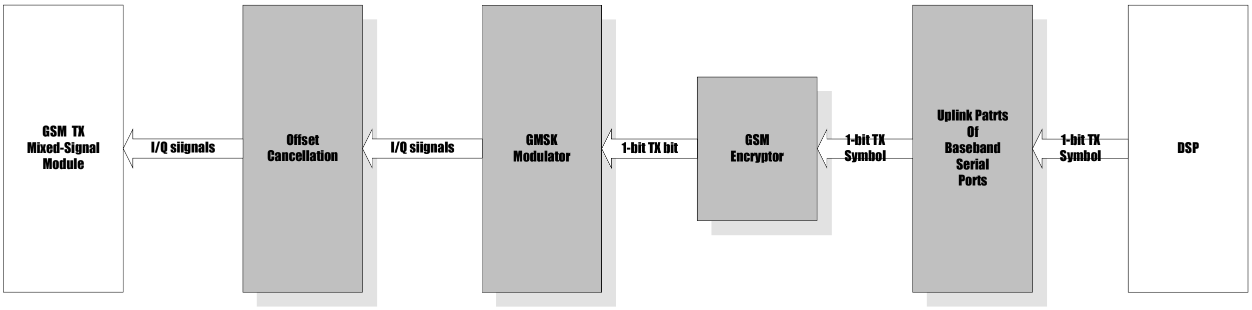

Figure 96 Block Diagram of Uplink Path

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On uplink path, the content of a burst, including tail bits, data bits, and training sequence bits is sent from DSP. DSP outputs will be t translated by GMSK Modulator. Where translated bits after modulation will become I/Q digital signals with certain latency.

TDMA timer having a quarter-bit timing accuracy gives the timing windows for uplink operation. Uplink operation is controlled by TX enable window and TX dump window of TDMA timer. Usually, TX enable window is opened earlier than TX dump window. When TX enable window of TDMA timer is opened, uplink path in Baseband Front End will power-on GSK TX mixed-signal module and thus drive valid outputs to RF module. However, uplink parts of Baseband Serial Ports still do not sink data from DSP through the serial interface between Baseband Serial Ports and DSP until TX dump window of TDMA timer is opened.

9.3.2 Compensation Circuit

9.3.2.1 Quadrature Phase

For 8PSK Modulation, in order to improve the EVM performance, use PHSEL[2:0](Phase Select) in TX_CFG control register to compensate the quadrature phase. 6 steps, 1degree/step, up to +/3 degree dynamic range.

9.3.2.2 DC offset Cancellation

Offset cancellation will be performed on these I/Q digital signals to compensate offset error of D/A converters (DAC) in TX mixed-signal module. Finally the generated I/Q digital signals will be input to TX mixed-signal module that contains two DAC for I/Q signal respectively.

9.3.3 Auxiliary Calibration Circuit - 540 kHz Sine Tone Generator

By setting ‘1’ to SGEN(Sine Tone Generation) in TX_CFG control register, the BBTX output will become 540khz single sine tone, which is used for Factory Calibration scheme for Mixed Signal Low Pass Filter Cut-off Frequency Accuracy.

9.3.4 GSM Encryptor

When uplink parts of Baseband Serial Ports pass a TX symbol to GSM Encryptor, GSM Encryptor will perform encryption on the TX symbol if set ‘1’ to BCIEN(Baseband Ciphering Encryption) in BFE_CON register. Otherwise, the TX symbol will be directed to GMSK modulator directly.

9.3.5 Modulation

9.3.5.1 GMSK Modulation

GMSK Modulator is used to convert bit stream of GSM bursts into in-phase and quadrature-phase outputs by means of GMSK modulation scheme. It consists of a ROM table, timing control logic and some state registers for GMSK modulation scheme. GMSK Modulator is activated when TX dump window is opened. There is latency between assertion of TX dump window and the first valid output of GMSK Modulator. The reason is because the bit rate of TX symbols is 270.833 KHz

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and the output rate of GMSK Modulator is 4.333 MHz, and therefore timing synchronization is necessary between the two rates.

Additionally, in order to prevent phase discontinuity in between the multiple-burst Mode, the GMSK modulator will output continuous 67.7khs sine tone outside the burst once RX DAC Enable window is still asserted. Once RX DAC Enable window is disserted, GMSK modulator will park at DC level.

9.3.5.2 I/Q Swap

By setting '1' to IQSWP in TX_CFG control register, phase on I/Q plane will rotate in inverse direction. This option is to meet the different requirement form RF chip regarding I/Q plane. This control signal is for GMSK Modulation only.

9.3.5.3 Debug Mode

9.3.5.3.1 Modulation Bypass Mode

For DSP debug purpose, set both '1' for MDBYP(Modulator Bypass) in TX_CFG control register and BYPFLR(Bypass RX Filter) in RX_CFG control register for directly loopback DSP 16-bits data (10bits valid data plus sign or zero extension) through DAC only.

9.3.5.3.2 Force GMSK Modulator turn on

By setting '1' to APNDEN(Append Enable) bit in TX CFG control register, GMSK modulator will park on constant DC level during the non-burst period, while the I/Q pair output phase maybe discontinuous since both modulator will be reset at the beginning of the burst. However, the reset of the modulator will be helpful for the debugging purpose.

9.3.6 Register Definitions

0x8210_0060 TX Configuration Register TX_CFG

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ALL_10_EN		SGEN	MDBYP				APNDEN
Type									RW		R/W	R/W				R/W
Reset									00		0	0				0

This register is for configuration of uplink path, inclusive of configuration of TX mixed-signal module and TX path in Baseband Front End.

APNDEN Appending Bits Enable. (For DSP digital loopback debug mode) The register bit is used to control the ending scheme of GPRS Mode GMSK modulation only.

- **0** Suitable for GPRS /EDGE mode. If a TX enable window contains several TX dump window, then GMSK modulator will still output in the intervals between two TX dump window and all 1's will be fed into GMSK modulator. In the other word, mainly used PA to perform the power ramp up/down, while Modulator output low amplitude sinewave. **Note that when the bit is set to '0', the interval between the moment at which TX enable window is activated and the moment at which TX dump window is activated must be multiples of one bit time.**

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1 Suitable for GSM only. After a TX dump window, GMSK modulator will only output for some bit time.

MDBYP Modulator Bypass (For DSP Debug Mode) Select. The register bit is used to select the bypass mode for I/Q pair outputs bypass the GMSK modulator

0 Regular Modulation Mode

1 Bypass Modulator Mode (DSP Debug Mode).

SGEN SineTone Generator Enable. (For Factory Calibration Purpose). The register bit is used to select the TX modulator output switch to 540 kHz Sine Tone.

0 BBTX output from regulator modulator output.

1 BBTX output switch to 540 kHz sine Tone

ALL_10GEN For Debug mode of BBTX. Generate all 1's or zero's input during BBTX valid burst. For GMSK modulation, set 2'b1 or 2'b10 will generate 67.7 kHz sine tone. Default value 2'b00 is normal mode.

0 Normal Mode, regular modulator input from Slave DSP TX Buffer.

1 Debug Mode, All zero's input pattern generated; GMSK modulator will generate 67.7 kHz sine tone.

2 Debug Mode All 1's input pattern generated; GMSK modulator will generate 67.7 kHz sine tone.

0x8210_0064 TX Control Register TX_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PHSEL											IQSWP
Type					R/W											R/W
Reset					0000											0

This register is for control of uplink path, inclusive of control of TX mixed-signal module and TX path in Baseband Front End.

IQSWP The register bit is for swapping the I- and Q-channel of the TX path. Moreover, this register is double buffered by EVENT_VALIDATE.

0: I and Q are not swapped.

1: I and Q are swapped.

PHSEL Quadrature phase compensation select

0000: 0 degree compensation.

0001: 1 degree compensation.

0010: 2 degree compensation.

0011: 3 degree compensation.

0100: 4 degree compensation.

0101: 5 degree compensation.

1010: -5 degree compensation.

1011: -4 degree compensation.

1100: -3 degree compensation.

1101: -2 degree compensation.

1110: -1 degree compensation.

1111: 0 degree compensation.

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0x8210_0068 TX I/Q Channel Offset Compensation Register TX_OFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFF_TYP		OFFQ[5:0]								OFFI[5:0]					
Type	R/W		R/W								R/W					
Reset	0		000000								000000					

The register is for offset cancellation of I-channel DAC in TX mixed-signal module. It is for compensation of offset error caused by I/Q-channel DAC in TX mixed-signal module. It is coded in 2's complement, that is, with maximum 31 and minimum –32.

OFFI Value of offset cancellation for I-channel DAC in TX mixed-signal module

OFFQ Value of offset cancellation for Q-channel DAC in TX mixed-signal module

OFF_TYP Type of the OFFI and OFFQ register. While OFF_TYP = 1, the offset values are double buffered and can be chaneged burst by burst after EVENT_VALIDATE comes. Otherwise, the offset values would change immidately after the coming of APB commands, which can't be adjusted burst by burst.

- **0** No double buffer
- **1** Double buffered

0x821000C0 Digital RF Setting Register DIG_RF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DIGI_TX_EN
Type																R/W
Reset																0

The register is for the setting of digital RF. BBTX will send GMSK output and Sync. Signal to RF digital part while DIGI_TX_EN is set.

DIGI_TX_EN Enable signal for digital RF.

- **0** Disable.
- **1** Enable.

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10 Timing Generator

Timing is the most critical issue in GSM/GPRS applications. The TDMA timer provides a simple interface for the MCU to program all the timing-related events for receive event control, transmit event control and the timing adjustment. Detailed descriptions are mentioned in Section 10.1.

10.1 TDMA timer

The TDMA timer unit is composed of three major blocks: Quarter bit counter, Signal generator and Event registers.

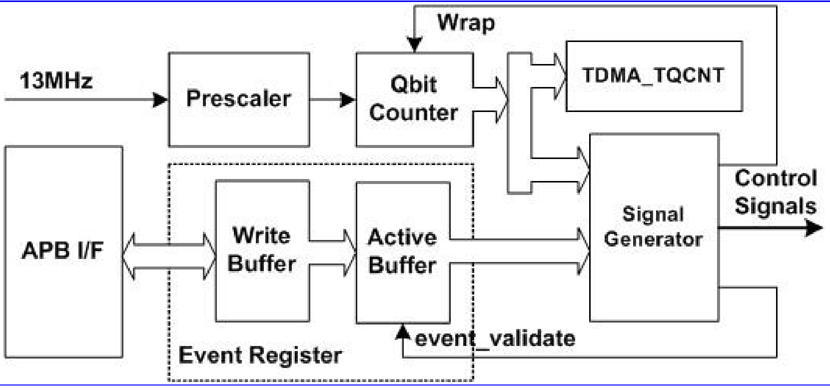

Figure 97 The block diagram of TDMA timer

By default, the quarter-bit counter continuously counts from 0 to the wrap position. In order to apply to cell synchronization and neighboring cell monitoring, the wrap position can be changed by the MCU to shorten or lengthen a TDMA frame. The wrap position is held in the TDMA_WRAP register and the current value of the TDMA quarter bit counter may be read by the MCU via the TDMA_TQCNT register.

The signal generator handles the overall comparing and event-generating processes. When a match has occurred between the quarter bit counter and the event register, a predefined control signal is generated. These control signals may be used for on-chip and off-chip purposes. Signals that change state more than once per frame make use of more than one event register.

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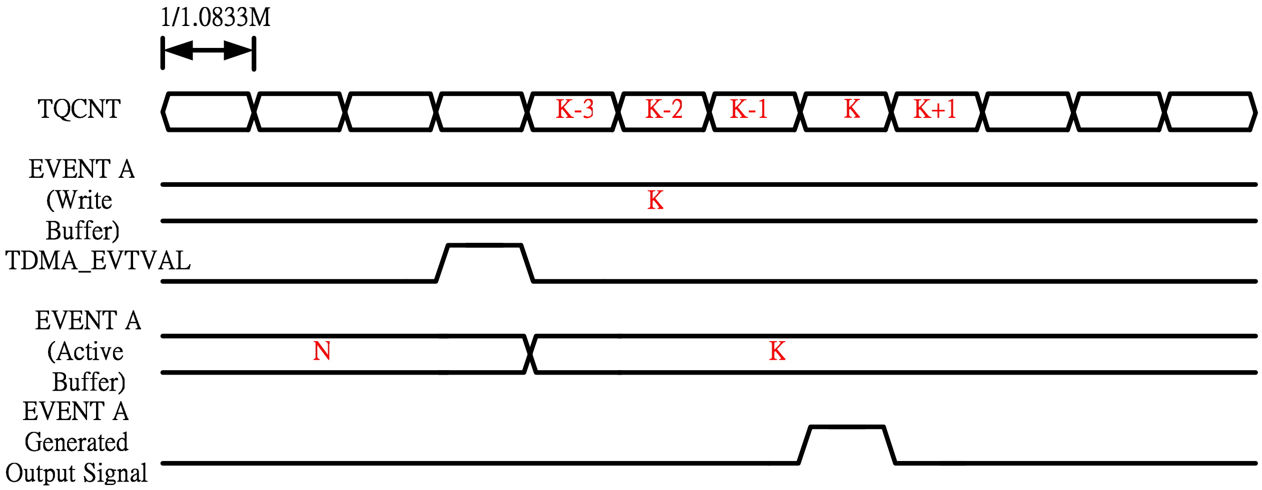

The event registers are programmed to contain the quarter bit position of the event that is to occur. The event registers are double buffered. The MCU writes into the write buffers of the registers, and the event TDMA_EVTVAL trigger HW to transfer the data from the write buffers to the active buffers. Caution: values in the active buffers are updated at the end of qbit count (TDMA_EVTVAL). The TDMA_EVTVAL signal itself may be programmed at any quarter bit position. These event registers could be classified into four groups:

On-chip Control Events

TDMA_EVTVAL

This event allows the data values written by the MCU to pass through to the active buffers.

TDMA_WRAP

TDMA quarter bit counter wrap position. This sets the position at which the TDMA quarter bit counter resets back to zero. The default value is 4999, changing this value will advance or retard the timing events in the frame following the next TDMA_EVTVAL signal. Caution: The wrap value of the first frame after the sleep mode will refer to TQWRAP_SM value if SW enables turbo sleep mode.

TDMA_DTIRQ

DSP TDMA interrupt requests. DTIRQ triggers the DSP to read the command from the MCU/DSP Shard RAM to schedule the activities that will be executed in the current frame.

TDMA_CTIRQ1/CTIRQ2

MCU TDMA interrupt requests. CTIRQx triggers the ARM to schedule the activities that will be executed in the next frame.

TDMA_AUXADC [1:0]

This signal triggers the monitoring ADC to measure the voltage, current, temperature, device id etc..

Note: For both MCU and DSP TDMA interrupt requests, these signals are all active Low during one quarter bit duration and they should be used as edge sensitive events by the respective interrupt controllers.

On-chip Receive Events

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TDMA_BDLON [5:0]

These registers are a set of six which contain the quarter bit event that initiates the receive window assertion sequence which powers up and enables the receive ADC, and then enables loading of the receive data into the receive buffer.

TDMA_BDLOFF [5:0]

These registers are a set of six which contain the quarter bit event that initiates the receive window de-assertion sequence which disables loading of the receive data into the receive buffer, and then powers down the receive ADC.

TDMA_RXWIN[5:0]

DSP TDMA interrupt requests. TDMA_RXWIN is usually used to initiate the related RX processing including two modes. In single-shot mode, TDMA_RXWIN is generated when the BRXFS signal is de-asserted. In repetitive mode, TDMA_RXWIN will be generated both regularly with a specific interval after BRXFS signal is asserted and when the BRXFS signal is de-asserted.

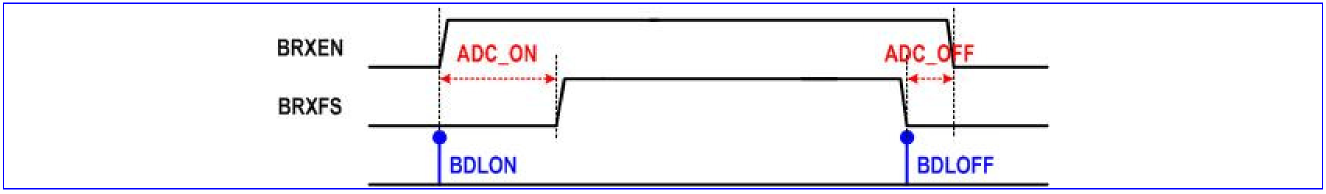

Figure 98 The timing diagram of BRXEN and BRXFS

Note: TDMA_BDLON/OFF event registers, together with TDMA_BDLCON register, generate the corresponding BRXEN and BRXFS window used to power up/down baseband downlink path and control the duration of data transmission to the DSP, respectively.

On-chip Transmit Events

TDMA_APC [6:0]

These registers initiate the loading of the transmit burst shaping values from the transmit burst shaping RAM into the transmit power control DAC.

TDMA_BULON [3:0]

This register contains the quarter bit event that initiates the transmit window assertion sequence which powers up the modulator DAC and then enables reading of bits from the transmit buffer into the GMSK modulator.

TDMA_BULOFF [3:0]

This register contains the quarter bit event that initiates the transmit window de-assertion sequence which disables the reading of bits from the transmit buffer into the GMSK modulator, and then power down the modulator DAC.

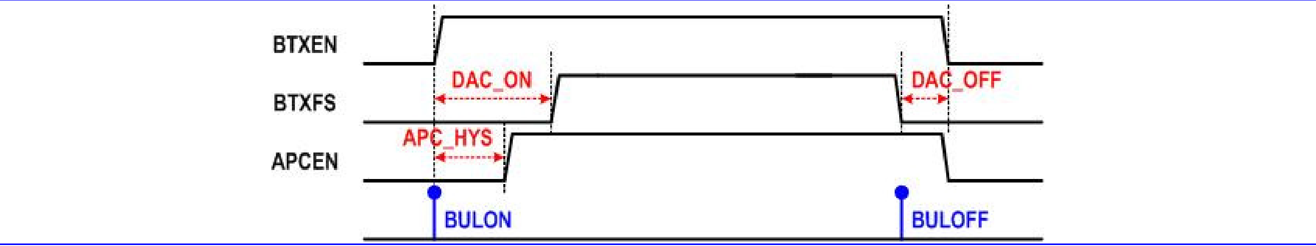

Figure 99 The timing diagram of BTXEN and BTXFS

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Note: TDMA_BULON/OFF event registers, together with TDMA_BULCON1, TDMA_BULCON2 register, generate the corresponding BTXEN, BTXFS and APCEN window used to power up/down the baseband uplink path, control the duration of data transmission from the DSP and power up/down the APC DAC, respectively.

Off-chip Control Events

TDMA_BSI [19:0]

The quarter bit positions of these 20 BSI events are used to initiate the transfer of serial words to the transceiver and synthesizer for gain control and frequency adjustment.

TDMA_BPI [41:0]

The quarter bit positions of these 30 BPI events are used to generate changes of state on the output pins to control the external radio components.

10.1.1 Register Definitions

0x8200_0150 Event Enable Register 0 TDMA_EVTENA0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					BDL5	BDL4	BDL3	BDL2	BDL1	BDL0				CTIRQ2	CTIRQ1	DTIRQ
Type					R/W	R/W	R/W	R/W	R/W	R/W				R/W	R/W	R/W
Reset					0	0	0	0	0	0				0	0	0

DTIRQ Enable TDMA_DTIRQ

CTIRQ*n* Enable TDMA_CTIRQ*n*

BDL*n* Enable TDMA_BDLON*n* and TDMA_BDLOFF*n*

For all these bits,

- **0** function is disabled
- **1** function is enabled

0x8200_0154h Event Enable Register 1 TDMA_EVTENA1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPRS				BUL3	BUL2	BUL1	BUL0		APC6	APC5	APC4	APC3	APC2	APC1	APC0
Type	R/W				R/W	R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0				0	0	0	0		0	0	0	0	0	0	0

GPRS Indicate which mode is on-going.

- **0** TDMA_APC0 & TDMA_APC1 events are controlled by APC0 & APC1 in the register TDMA_EVTENA1 & TDMA_DTXCON. (GSM mode)
- **1** TDMA_APC0 & TDMA_APC1 events are controlled by APC0 & APC1 in the register TDMA_EVTENA1 only. (GPRS mode)

APC*n* Enable TDMA_APC*n*

BUL*n* Enable TDMA_BULON*n* and TDMA_BULOFF*n*

For all these bits,

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0 function is disabled

1 function is enabled

0x8200_0158 Event Enable Register 2 TDMA_EVTENA2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI15	BSI14	BSI13	BSI12	BSI11	BSI10	BSI9	BSI8	BSI7	BSI6	BSI5	BSI4	BSI3	BSI2	BSI1	BSI0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8200_015C Event Enable Register 3 TDMA_EVTENA3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BSI19	BSI18	BSI17	BSI16
Type													R/W	R/W	R/W	R/W
Reset													0	0	0	0

BSI*n* BSI event enable control

0 Disable TDMA_BSI*n*

1 Enable TDMA_BSI*n*

0x8200_0160 Event Enable Register 4 TDMA_EVTENA4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPI15	BPI14	BPI13	BPI12	BPI11	BPI10	BPI9	BPI8	BPI7	BPI6	BPI5	BPI4	BPI3	BPI2	BPI1	BPI0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8200_0164 Event Enable Register 5 TDMA_EVTENA5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPI31	BPI30	BPI29	BPI28	BPI27	BPI26	BPI25	BPI24	BPI23	BPI22	BPI21	BPI20	BPI19	BPI18	BPI17	BPI16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BPI*n* BPI event enable control

0 Disable TDMA_BPI*n*

1 Enable TDMA_BPI*n*

0x8200_0168 Event Enable Register 6 TDMA_EVTENA6

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FH5	FH4	FH3	FH2	FH1	FH0	BPI41	BPI40	BPI39	BPI38	BPI37	BPI36	BPI35	BPI34	BPI33	BPI32
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BPI*n* BPI event enable control
- **0** Disable TDMA_BPI*n*
- **1** Enable TDMA_BPI*n*

FHn Frequency Hopping control
- **0** Disable TDMA_FHSTRn
- **1** Enable TDMA_FHSTRn

0x8200_016C Event Enable Register 7 TDMA_EVTENA7

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															AUX1	AUX0
Type															R/W	R/W
Reset															0	0

AUX Auxiliary ADC event enable control
- **0** Disable Auxiliary ADC event
- **1** Enable Auxiliary ADC event

0x8200_0170 Qbit Timer Offset Control Register TDMA_WRAPOFS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															TOI[1:0]	
Type															R/W	
Reset															0	

TOI This register defines the value used to advance the Qbit timer in unit of 1/4 quarter bit; the timing advance will be take place as soon as the TDMA_EVTVAL is occurred, and it will be cleared automatically.

0x8200_0174 Qbit Timer Biasing Control Register TDMA_REGBIAS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			TQ_BIAS[13:0]													
Type			R/W													
Reset			0													

TQ_BIAS This register defines the Qbit offset value which will be added to the registers being programmed. It only takes effects on FHSTR, BDLON/OFF, BULON/OFF, APC, AUXADC, BSI and BPI event registers.

0x8200_0180 DTX Control Register TDMA_DTXCON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DTX3	DTX2	DTX1	DTX0
Type													R/W	R/W	R/W	R/W

DTX DTX flag is used to disable the associated transmit signals

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0 BULON0~3, BULOFF0~3, APC_EV0 & APC_EV1 are controlled by TDMA_EVTENA1 register
1 BULON0~3, BULOFF0~3, APC_EV0 & APC_EV1 are disabled

0x8200_0184 Receive Interrupt Control Register TDMA_RXCON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MOD5	MOD4	MOD3	MOD2	MOD1	MOD0	RXINTCNT[9:0]									
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W									

RXINTCNT TDMA_RXWIN interrupt generation interval in quarter bit unit
MOD*n* Mode of Receive Interrupts
0 Single shot mode for the corresponding receive window
1 Repetitive mode for the corresponding receive window

0x8200_0188 Baseband Downlink Control Register TDMA_BDLCON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_ON										ADC_OFF					
Type	R/W										R/W					

ADC_ON BRXEN to BRXFS setup up time in quarter bit unit.
ADC_OFF BRXEN to BRXFS hold up time in quarter bit unit.

0x8200_018C Baseband Uplink Control Register 1 TDMA_BULCON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAC_ON								DAC_OFF							
Type	R/W								R/W							

DAC_ON BTXEN to BTXFS setup up time in quarter bit unit.
DAC_OFF BTXEN to BTXFS hold up time in quarter bit unit.

0x8200_0190 Baseband Uplink Control Register 2 TDMA_BULCON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									APC_HYS							
Type									R/W							

APC_HYS APCEN to BTXEN hysteresis time in quarter bit unit.

0x8200_0194 Frequency Burst Indication Register TDMA_FB_FLAG

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											FBDL5	FBDL4	FBDL3	FBDL2	FBDL1	FBDL0
Type											R/W	R/W	R/W	R/W	R/W	R/W

FBDLn Indication of frequency burst for RX window n

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The register is double-buffered. The value at the write buffers will be auto-cleared at the next event-validate (TDMA_EVTVAL) and its value will be at the same time loaded to the active buffer. The exact FB indication comes from the active buffer and the corresponding mode in register TDMA_RXCON (Bit15~Bit10). It will be asserted after TDMA_EVTVAL signals if the corresponding FBDLx & TDMA_RXCON[x+10] are set to 1. The FB indication de-assertion only depends TDMA_FB_CLRI and the falling edge of the corresponding RX window.

0x8200_0198 Direct Frequency Burst Closing TDMA_FB_CLRI

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																

As long as the register is written, active buffer for FB indication will be reset then therefore the frequency burst indication will be forced to 0.

0x8200_0310h DSP ROM HW Wake Up Reset TDMA_DSPSPROM_HWPD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HWEN				HW_WAKE_UP_TIME											
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

HWEN Enable the function of issuing a reset signal to DSP ROM at BB waking up from sleep mode.

- **0** Disable
- **1** Enable

HW_WAKE_UP_TIME How much time (32k period time) the reset is issued after BB waking up from sleep mode. Default is 2T (32k period) = 62.5 us

0x8200_0314h DSP ROM SW Wake Up Reset TDMA_DSPSPROM_SWPD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SWEN				SW_WAKE_UP_TIME											
Type	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

SWEN Enable the function of issuing a reset signal to DSP ROM (Caution: If SW mode is enabled, HW mode in TDMA_DSPSPROM_HWPD must be disabled). After

- **0** Disable
- **1** Enable

SW_WAKE_UP_TIME How much time (bclk_ck) the reset is issued after enabling this function. Default is 1T (52M) = 14.7456 us. This value varies at DCM turning on.

Address	Type	Width	Reset Value	Name	Description
0x8200_0000	R	[13:0]	—	TDMA_TQCNT	Read quarter bit counter
0x8200_0004	R/W	[13:0]	0x1387	TDMA_WRAP	Latched Qbit counter reset position

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0x8200_0008	R/W	[13:0]	0x1387	TDMA_WRAPIMD	Direct Qbit counter reset position
0x8200_000C	R/W	[13:0]	0x0000	TDMA_EVTVAL	Event latch position
0x8200_0010	R/W	[13:0]	—	TDMA_DTIRQ	DSP software control
0x8200_0014	R/W	[13:0]	—	TDMA_CTIRQ1	MCU software control 1
0x8200_0018	R/W	[13:0]	—	TDMA_CTIRQ2	MCU software control 2
0x8200_0030	R/W	[13:0]	—	TDMA_BDLON0	Data serialization of the 1st RX block
0x8200_0034	R/W	[13:0]	—	TDMA_BDLOFF0	
0x8200_0038	R/W	[13:0]	—	TDMA_BDLON1	Data serialization of the 2nd RX block
0x8200_003C	R/W	[13:0]	—	TDMA_BDLOFF1	
0x8200_0040	R/W	[13:0]	—	TDMA_BDLON2	Data serialization of the 3rd RX block
0x8200_0044	R/W	[13:0]	—	TDMA_BDLOFF2	
0x8200_0048	R/W	[13:0]	—	TDMA_BDLON3	Data serialization of the 4th RX block
0x8200_004C	R/W	[13:0]	—	TDMA_BDLOFF3	
0x8200_0050	R/W	[13:0]	—	TDMA_BDLON4	Data serialization of the 5th RX block
0x8200_0054	R/W	[13:0]	—	TDMA_BDLOFF4	
0x8200_0058	R/W	[13:0]	—	TDMA_BDLON5	Data serialization of the 6th RX block
0x8200_005C	R/W	[13:0]	—	TDMA_BDLOFF5	
0x8200_0060	R/W	[13:0]	—	TDMA_BULON0	Data serialization of the 1st TX slot
0x8200_0064	R/W	[13:0]	—	TDMA_BULOFF0	
0x8200_0068	R/W	[13:0]	—	TDMA_BULON1	Data serialization of the 2nd TX slot
0x8200_006C	R/W	[13:0]	—	TDMA_BULOFF1	
0x8200_0070	R/W	[13:0]	—	TDMA_BULON2	Data serialization of the 3rd TX slot
0x8200_0074	R/W	[13:0]	—	TDMA_BULOFF2	
0x8200_0078	R/W	[13:0]	—	TDMA_BULON3	Data serialization of the 4th TX slot
0x8200_007C	R/W	[13:0]	—	TDMA_BULOFF3	
0x8200_0090	R/W	[13:0]	—	TDMA_APC0	The 1st APC control
0x8200_0094	R/W	[13:0]	—	TDMA_APC1	The 2nd APC control
0x8200_0098	R/W	[13:0]	—	TDMA_APC2	The 3rd APC control
0x8200_009C	R/W	[13:0]	—	TDMA_APC3	The 4th APC control
0x8200_00A0	R/W	[13:0]	—	TDMA_APC4	The 5th APC control
0x8200_00A4	R/W	[13:0]	—	TDMA_APC5	The 6th APC control
0x8200_00A8	R/W	[13:0]	—	TDMA_APC6	The 7th APC control
0x8200_00B0	R/W	[13:0]	—	TDMA_BSI0	BSI event 0
0x8200_00B4	R/W	[13:0]	—	TDMA_BSI1	BSI event 1
0x8200_00B8	R/W	[13:0]	—	TDMA_BSI2	BSI event 2
0x8200_00BC	R/W	[13:0]	—	TDMA_BSI3	BSI event 3

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0x8200_00C0	R/W	[13:0]	—	TDMA_BSI4	BSI event 4
0x8200_00C4	R/W	[13:0]	—	TDMA_BSI5	BSI event 5
0x8200_00C8	R/W	[13:0]	—	TDMA_BSI6	BSI event 6
0x8200_00CC	R/W	[13:0]	—	TDMA_BSI7	BSI event 7
0x8200_00D0	R/W	[13:0]	—	TDMA_BSI8	BSI event 8
0x8200_00D4	R/W	[13:0]	—	TDMA_BSI9	BSI event 9
0x8200_00D8	R/W	[13:0]	—	TDMA_BSI10	BSI event 10
0x8200_00DC	R/W	[13:0]	—	TDMA_BSI11	BSI event 11
0x8200_00E0	R/W	[13:0]	—	TDMA_BSI12	BSI event 12
0x8200_00E4	R/W	[13:0]	—	TDMA_BSI13	BSI event 13
0x8200_00E8	R/W	[13:0]	—	TDMA_BSI14	BSI event 14
0x8200_00EC	R/W	[13:0]	—	TDMA_BSI15	BSI event 15
0x8200_00F0	R/W	[13:0]	—	TDMA_BSI16	BSI event 16
0x8200_00F4	R/W	[13:0]	—	TDMA_BSI17	BSI event 17
0x8200_00F8	R/W	[13:0]	—	TDMA_BSI18	BSI event 18
0x8200_00FC	R/W	[13:0]	—	TDMA_BSI19	BSI event 19
0x8200_0100	R/W	[13:0]	—	TDMA_BPI0	BPI event 0
0x8200_0104	R/W	[13:0]	—	TDMA_BPI1	BPI event 1
0x8200_0108	R/W	[13:0]	—	TDMA_BPI2	BPI event 2
0x8200_010C	R/W	[13:0]	—	TDMA_BPI3	BPI event 3
0x8200_0110	R/W	[13:0]	—	TDMA_BPI4	BPI event 4
0x8200_0114	R/W	[13:0]	—	TDMA_BPI5	BPI event 5
0x8200_0118	R/W	[13:0]	—	TDMA_BPI6	BPI event 6
0x8200_011C	R/W	[13:0]	—	TDMA_BPI7	BPI event 7
0x8200_0120	R/W	[13:0]	—	TDMA_BPI8	BPI event 8
0x8200_0124	R/W	[13:0]	—	TDMA_BPI9	BPI event 9
0x8200_0128	R/W	[13:0]	—	TDMA_BPI10	BPI event 10
0x8200_012C	R/W	[13:0]	—	TDMA_BPI11	BPI event 11
0x8200_0130	R/W	[13:0]	—	TDMA_BPI12	BPI event 12
0x8200_0134	R/W	[13:0]	—	TDMA_BPI13	BPI event 13
0x8200_0138	R/W	[13:0]	—	TDMA_BPI14	BPI event 14
0x8200_013C	R/W	[13:0]	—	TDMA_BPI15	BPI event 15
0x8200_0140	R/W	[13:0]	—	TDMA_BPI16	BPI event 16
0x8200_0144	R/W	[13:0]	—	TDMA_BPI17	BPI event 17
0x8200_0148	R/W	[13:0]	—	TDMA_BPI18	BPI event 18
0x8200_014C	R/W	[13:0]	—	TDMA_BPI19	BPI event 19

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0x8200_01A0	R/W	[13:0]	—	TDMA_BPI20	BPI event 20
0x8200_01A4	R/W	[13:0]	—	TDMA_BPI21	BPI event 21
0x8200_01A8	R/W	[13:0]	—	TDMA_BPI22	BPI event 22
0x8200_01AC	R/W	[13:0]	—	TDMA_BPI23	BPI event 23
0x8200_01B0	R/W	[13:0]	—	TDMA_BPI24	BPI event 24
0x8200_01B4	R/W	[13:0]	—	TDMA_BPI25	BPI event 25
0x8200_01B8	R/W	[13:0]	—	TDMA_BPI26	BPI event 26
0x8200_01BC	R/W	[13:0]	—	TDMA_BPI27	BPI event 27
0x8200_01C0	R/W	[13:0]	—	TDMA_BPI28	BPI event 28
0x8200_01C4	R/W	[13:0]	—	TDMA_BPI29	BPI event 29
0x8200_01C8	R/W	[13:0]	—	TDMA_BPI30	BPI event 30
0x8200_01CC	R/W	[13:0]	—	TDMA_BPI31	BPI event 31
0x8200_01D0	R/W	[13:0]	—	TDMA_BPI32	BPI event 32
0x8200_01D4	R/W	[13:0]	—	TDMA_BPI33	BPI event 33
0x8200_01D8	R/W	[13:0]	—	TDMA_BPI34	BPI event 34
0x8200_01DC	R/W	[13:0]	—	TDMA_BPI35	BPI event 35
0x8200_01E0	R/W	[13:0]	—	TDMA_BPI36	BPI event 36
0x8200_01E4	R/W	[13:0]	—	TDMA_BPI37	BPI event 37
0x8200_01E8	R/W	[13:0]	—	TDMA_BPI38	BPI event 38
0x8200_01EC	R/W	[13:0]	—	TDMA_BPI39	BPI event 39
0x8200_01F0	R/W	[13:0]	—	TDMA_BPI40	BPI event 40
0x8200_01F4	R/W	[13:0]	—	TDMA_BPI41	BPI event 41
0x8200_0400	R/W	[13:0]	—	TDMA_AUXEV0	Auxiliary ADC event 0
0x8200_0404	R/W	[13:0]	—	TDMA_AUXEV1	Auxiliary ADC event 1
0x8200_0150	R/W	[15:0]	0x0000	TDMA_EVTENA0	Event Enable Control 0
0x8200_0154	R/W	[15:0]	0x0000	TDMA_EVTENA1	Event Enable Control 1
0x8200_0158	R/W	[15:0]	0x0000	TDMA_EVTENA2	Event Enable Control 2
0x8200_015C	R/W	[3:0]	0x0000	TDMA_EVTENA3	Event Enable Control 3
0x8200_0160	R/W	[15:0]	0x0000	TDMA_EVTENA4	Event Enable Control 4
0x8200_0164	R/W	[13:0]	0x0000	TDMA_EVTENA5	Event Enable Control 5
0x8200_0168	R/W	[1:0]	0x0000	TDMA_EVTENA6	Event Enable Control 6
0x8200_016C	R/W	[11:0]	0x0000	TDMA_EVTENA7	Event Enable Control 7
0x8200_0170	R/W	[1:0]	0x0000	TDMA_WRAPOFS	TQ Counter Offset Control Register
0x8200_0174	R/W	[13:0]	0x0000	TDMA_REGBIAS	Biasing Control Register
0x8200_0180	R/W	[3:0]	—	TDMA_DTXCON	DTX Control Register
0x8200_0184	R/W	[15:0]	—	TDMA_RXCON	Receive Interrupt Control Register

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0x8200_0188	R/W	[15:0]	—	TDMA_BDLCON	Downlink Control Register
0x8200_018C	R/W	[15:0]	—	TDMA_BULCON1	Uplink Control Register 1
0x8200_0190	R/W	[7:0]	—	TDMA_BULCON2	Uplink Control Register 2
0x8200_0194	R/W	[5:0]	—	TDMA_FB_FLAG	FB indicator
0x8200_0198	W		—	TDMA_FB_CLRI	Direct clear of FB indicator
0x8200_0310	R/W	[15:0]	0x1	TDMA_DSPSPROM_HWPD	DSP ROM HW Power up Reset
0x8200_0314	R/W	[15]	0x0	TDMA_DSPSPROM_SWPD	DSP ROM SW Power up Reset
0x8200_0320	R/W	[13:0]	—	TDMA_FHSTR0	Frequency Hopping Strobe 0
0x8200_0324	R/W	[13:0]	—	TDMA_FHSTR1	Frequency Hopping Strobe 1
0x8200_0328	R/W	[13:0]	—	TDMA_FHSTR2	Frequency Hopping Strobe 2
0x8200_032c	R/W	[13:0]	—	TDMA_FHSTR3	Frequency Hopping Strobe 3
0x8200_0330	R/W	[13:0]	—	TDMA_FHSTR4	Frequency Hopping Strobe 4
0x8200_0334	R/W	[13:0]	—	TDMA_FHSTR5	Frequency Hopping Strobe 5

Table 72 TDMA Timer Register Map

10.1.2 Application Note

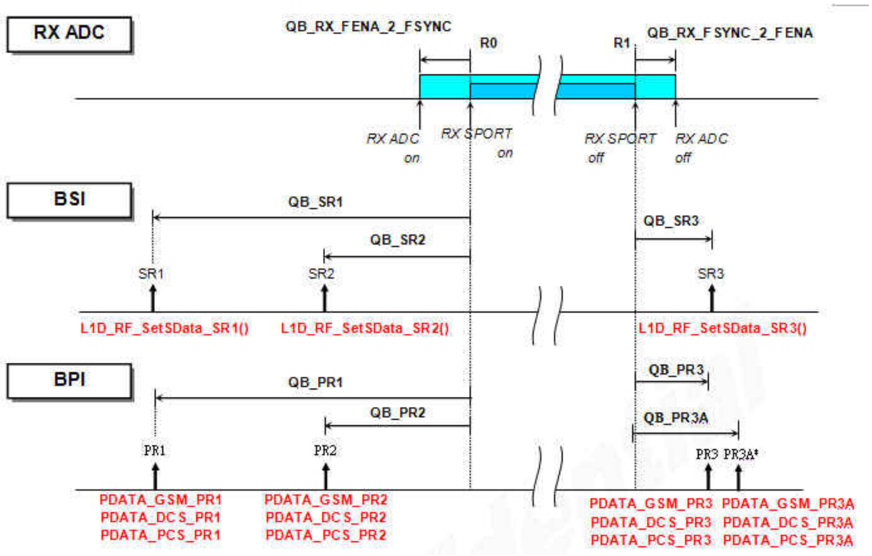

Figure 100 RX Timing Set Example

The TDMA timing and data setting are described in 2 parts. One part is that before turning on RX SPORT to receiving I/Q data. And the other part is after turning off RX SPORT to finish receiving I/Q data. To describe these two parts easily, the timing of turning on RX SPORT is taken as one base named **R0**. And the timing of turning off RX SPORT is taken as one base named **R1**.

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RX ADC part:

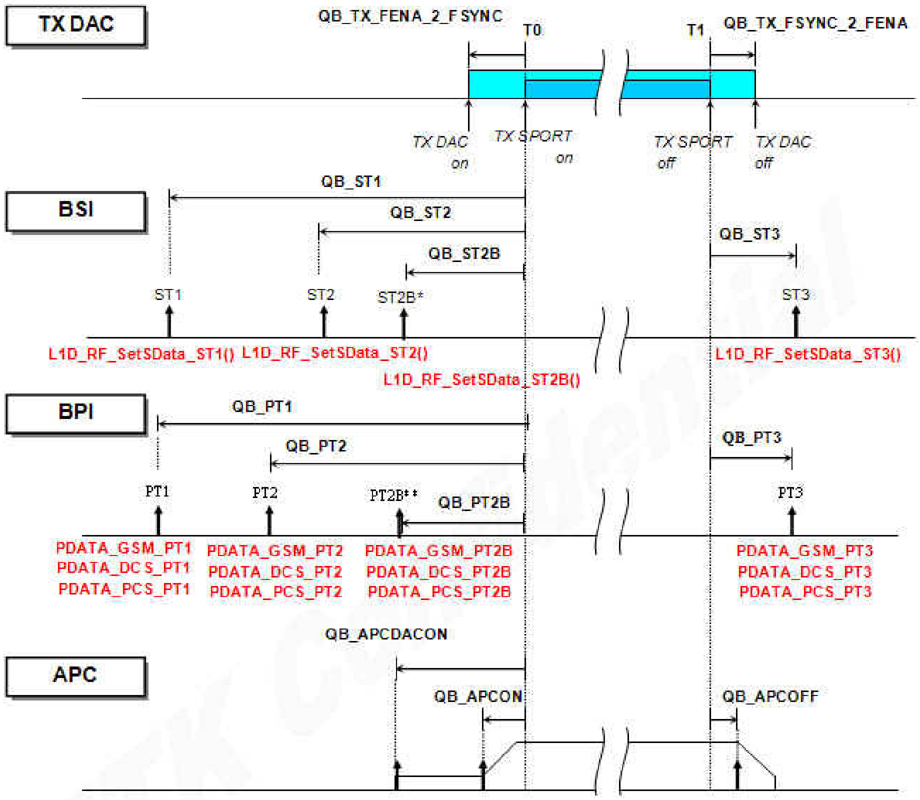
To setup the timing of RX ADC and SPORT, 2 timings need to be defined in **l1d_custom_rf.h**. The time from RX ADC enabling to RX SPORT turning on (**R0**) is defined as **QB_RX_FENA_2_FSYNC**.The time from RX SPORT turning on (**R1**) to RX ADC disabling is defined as **QB_RX_FSYNC_2_FENA**. The value of this two aliases should be positive or zero. These two values is defined in the register **TDMA_BDLCON**.

BSI part:

BSI data and events need to be set in serial to a 3-wire base RF module. Each RX window is allocated 3 BSI events. Usually 1'st BSI event is used to warm up the synthesizer and set its N-counter to lock the operation frequency. The 2'nd BSI is used to set the receiving amplifier gain of transceiver. The 3'rd BSI is used to command transceiver entering idle mode. BSI events are defined in the registers **TDMA_BSI0~19**.

BPI part:

The connection of HW signals of BPI data bus and RF module is flexible and depends on customer's design. The setting timing and data setting of BPI bus are used to specify at what time and which BPI states are changed. The BPI data may be varied by the operation band, so the dedicate BPI data of each band should be defined. The states transient of BPI signals are decided by the time of event, therefore the active time and the BPI states for each band shall be defined. BPI events are defined in the registers **TDMA_BPI0~41**.



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TX ADC part:

To setup the timing of TX DAC and SPORT, 2 timings need to be defined in **l1d_custom.h**. The time from TX DAC enabling to TX SPORT turning on (**T0**) is defined as **QB_TX_FENA_2_FSYNC**.The time from TX SPORT turning on (**T1**) to TX DAC disabling is defined as **QB_TX_FSYNC_2_FENA**. The value of this two aliases should be positive or zero. These two values is defined in the register **TDMA_BULCON1**.

BSI part:

BSI data and events need to be set in order to sent serial data to 3-wire devices on RF module. Each TX window is allocated 3 BSI events. Usually 1'st BSI event is used to warm up the set synthesizer and set its N-counter to lock the operation frequency. The 2'nd BSI is used to set the transmit command and indicate the operation band. The 3'rd BSI is used to command transceiver entering idle mode. BSI events are defined in the registers **TDMA_BSI0~19**.

BPI parts:

The setting of BPI bus includes timing and data setting to specify at what time what BPI states are changed. The BPI data may be varied by operation band, so the BPI data of each band should be defined. The 1'st BPI event is usually used to activate the RF components on RF module in transmit mode. The 2'nd BPI event is usually used to select band and switch R/TX. The 3'rd BPI event is usually used to force the RF module into idle mode. BPI events are defined in the registers **TDMA_BPI0~41**.

APC parts:

In addition to TX DAC, TX SPORT, BSI, BPI unit needs to be set, the control of PA is important for TX window. The PA is control by the APC unit of MT62xx. Before the data transmission, APC ramps up the PA to the indicated power level. Data is transmitted at that level. After finishing transmission, APC ramps down the PA. Before PA ramping up, A DC offset of PA is performed to let PA ramp up smoothly. APC events are defined in the registers **TDMA_APC0~6**.

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11 Power, Clocks and Reset

This chapter describes the power, clock and reset management functions provided by MT6253. Together with Power Management IC (PMIC), MT6253 offers both fine and coarse resolutions of power control through software programming. With this efficient method, the developer can turn on selective resources accordingly in order to achieve optimized power consumption. The operating modes of MT6253 as well as main power states provided by the PMIC are shown in **Figure 101**.

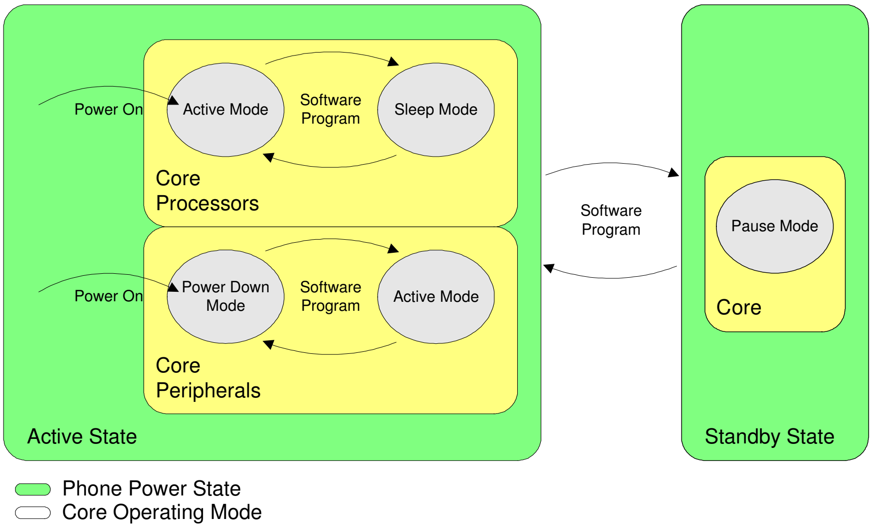

Figure 101 Major Phone Power States and Operating Modes for MT6253 based terminal

11.1 Clocks

There are two major time bases in the MT6253. For the faster one is the 26 MHz clock originating from the digital control oscillator (DCXO) of RF block. This signal is then converted to the square-wave signal through CLKSQ. The other time base is the 32768 Hz clock generated by an on-chip oscillator connected to an external crystal.**Figure 102** shows the clock sources as well as their utilizations inside the chip.

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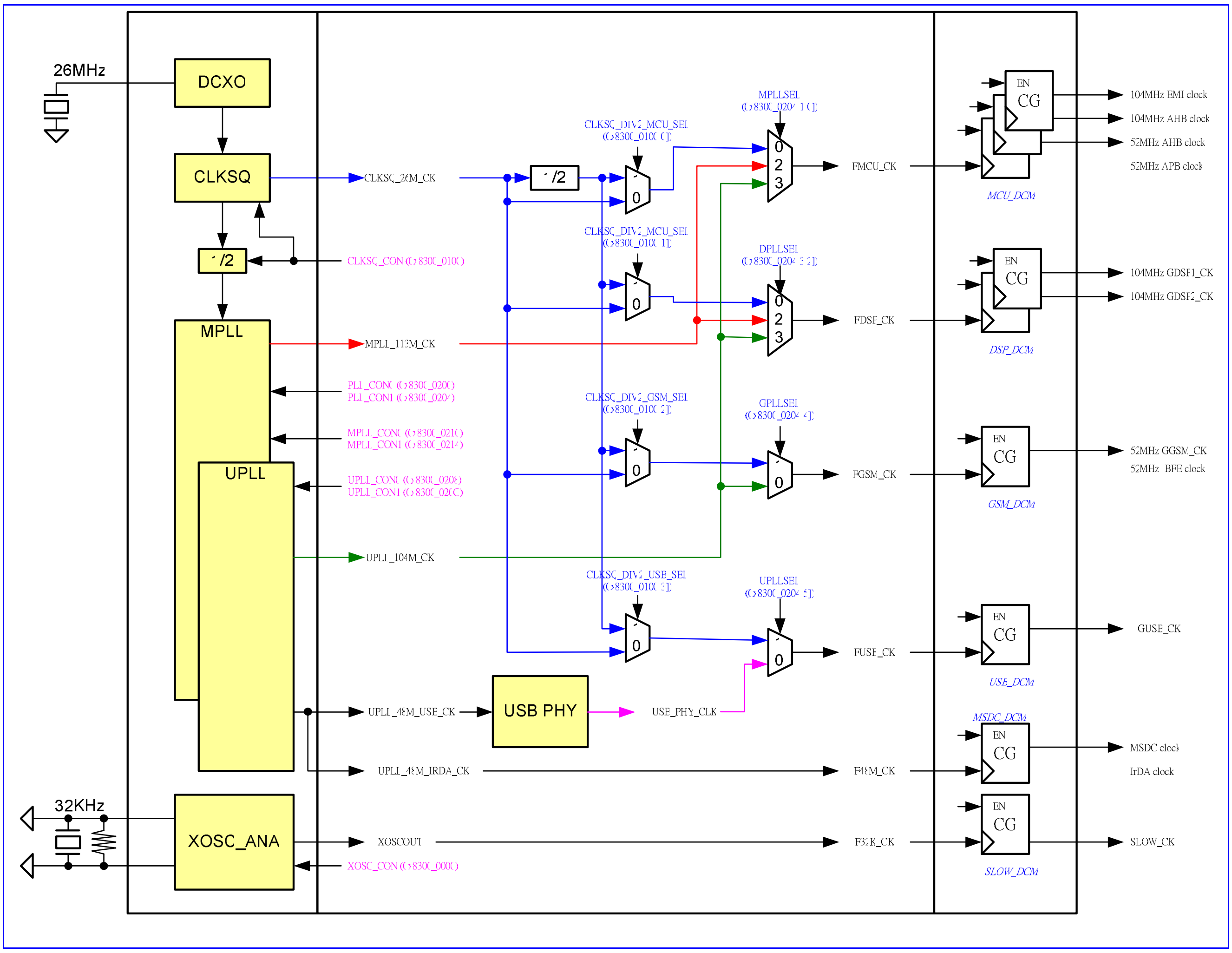

Figure 102 Clock distributions inside the MT6253

11.1.1 32.768 KHz Time Base

The 32768 Hz clock is always running. It's mainly used as the time base of the Real Time Clock (RTC) module, which maintains time and date with counters. Therefore, both the 32768Hz oscillator and the RTC module is powered by separate voltage supplies that shall not be powered down when the other supplies do.

In low power mode, the 13 MHz time base is turned off, so the 32768 Hz clock shall be employed to update the critical TDMA timer and Watchdog Timer. This time base is also used to clocks the keypad scanner logic.

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11.1.2 26 MHz Time Base

Since PLL are based on 13MHz reference clock. There is an 1/2-dividers for PLL existing to allow using 26 MHz DCXO.

There are 2 phase-locked loops (PLL) in MT6253. The UPLL generates 624Mhz clock output, then a frequency divider further divide 6, and 13 to generate fixed 104Mhz, and 48Mhz for GSM_CLOCK and USB_CLOCK, respectively. The MPLL generates dynamically programmable clock from 104~113MHz for MCU_CLOCK and DSP_CLOCK. These four primary clocks then feed into GSM, USB, MCU and DSP Clock Domain, respectively. These 2 PLLs require no off-chip components for operations and can be turn off in order to save power. After power-on, the PLLs are off by default and the source clock signal is selected through multiplexers. The software shall take cares of the PLL lock time while changing the clock selections. The PLL and usages are listed below.

- PLLs supply four clock source: MCU_CLOCK (104~113MHz), DSP_CLOCK (104~113MHz), GSM_CLOCK (104MHz) and USB_CLOCK (48MHz)
- For DSP/MCU system clock, *MCU_CLOCK and DSP_CLOCK*. The outputted 104~113MHz clock is controllable by MCU for 500KHz per step and settled time is under 100uS. The clock is also connected to DSP/MCU DCM (dynamic clock manager) for dynamically adjusting clock rate by digital clock divider. MCU_CLOCK paces the operations of the MCU cores, MCU memory system, and MCU peripherals as well
- Modem system clock, *GSM_CLOCK*, which paces the operations of the GSM/GPRS hardware, coprocessors as well. The outputted 104MHz clock is connected to GSM_DCM for dynamically adjusting clock rate by digital clock divider. Typically the GSM_DCM output clock no more than 52MHz.

Note that PLL need some time to become stable after being powered up. The software shall take cares of the PLL lock time before switching them to the proper frequency. Usually, a software loop longer than the PLL lock time is employed to deal with the problem.

For power management, the MCU software program may stop MCU Clock by setting the Sleep Control Register. Any interrupt requests to MCU can pause the sleep mode, and thus MCU return to the running mode.

AHB also can be stop by setting the Sleep Control Register. However the behavior of AHB in sleep mode is a little different from that of MCU. After entering Sleep Mode, it can be temporarily waken up by any “hreq” (bus request), and then goes back to sleep automatically after all “hreqs” de-assert. Any transactions can take place as usual in sleep mode, and it can save power while there is no transaction on it. However the penalty is losing a little system efficiency for switching on and off bus clock, but the impact is small.

11.1.3 Dynamic Clock Switch of MCU Clock

Dynamic Clock Manager is implemented to allow MCU and DSP switching clock dynamically without any jitter, and enabling signal drift, and system can operate stably during any clock rate switch.

Please note that PLL must be enabled and the frequency shall be set as 624MHz, therefore the required MCU/DSP/USB clocks can be generated from 624MHz.

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However, the settings of some hardware modules are required to be changed before or after clock rate change. Software has the responsibility to change them at proper timing. The following table is list of hardware modules needed to be changed their setting during clock rate change.

Module Name	Programming Sequence
EMI	Low clock speed -> high clock speed Changing wait state before clock change. New wait state will not take effect until current EMI access is complete. Software should insert a period of time before switching clock. High clock speed -> low clock speed Changing wait state after clock change.
LCD	Change wait state while LCD in IDLE state.

Table 73 Programming sequence during clock switch

11.1.4 Standard PLL Power-on Sequence

// 0x8300_0100: Power off Single-end CLKSQ: [6] RG_CLKSQ_SIN_PWDB=0

*CLKSQ_CON = 0x00A0;

// 0x8300_020C Power on & Reset UPLL: [1]RG_UPLL_PWDB=1, [0]RG_UPLL_RST=1

*UPLL_CON1 = 0x001F;

// 0x8300_0214: Power on & Reset MPLL: [1]RG_MPLL_PWDB=1, [0]RG_MPLL_RST=1

*MPLL_CON1 = 0xCE33;

// 0x8300_020C Release reset UPLL: [1]RG_UPLL_PWDB=1, [0]RG_UPLL_RST=0

*UPLL_CON1 = 0x001E;

// 0x8300_0214: Release reset MPLL: [1]RG_MPLL_PWDB=1, [0]RG_MPLL_RST=0

*MPLL_CON1 = 0xCE32;

for (i=0;i<200;i++); // wait for UPLL & MPLL stable

// 0x8300_0204: UPLL & MPLL output select:[5]GPLLSEL=1,[4]UPLLSEL=1,

[3:2]DPLLSEL=10,[1:0]MPLLSEL=10

*PLL_CON1 = 0x017A;

11.1.5 Register Definitions

ADDRESS	TITLE	DESCRIPTION
8300_0000	**XOSC_CON**	**XOSC control register**

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8300_0100	CLKSQ_CON	CLKSQ control register
8300_0200	PLL_CON0	PLL control register 0
8300_0204	PLL_CON1	PLL control register 1
8300_0208	UPLL_CON0	UPLL control register 0
8300_020C	UPLL_CON1	UPLL control register 1
8300_0210	MPLL_CON0	MPLL control register 0
8300_0214	MPLL_CON0	MPLL control register 1
8300_0220	MPLL_TDMAWB01	MPLL TDMA write buffer 01
8300_0224	MPLL_TDMAWB23	MPLL TDMA write buffer 23
8300_0228	MPLL_TDMAWB45	MPLL TDMA write buffer 45

0x8300_0000 XOC32 Control Register XOSC_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_XOSC_PWDB			RG_XOSC_CALI				
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	01000				

Set this register for XOSC32 circuit configuration controls.

RG_XOSC_PWDB XOSC32 power-down control setting

- **0** power-down
- **1** power-on

RG_XOSC_CALI XOSC32 calibration setting Gm value

0x8300_0100 CLKSQ Control Register CLKSQ_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CLKSQTEST_EN								SRCCLK	RG_CLKSQ_SIN_PWDB	RG_CLKSQ_DIFF_PWDB	RG_CLKSQ_CKSEL	CLKSQ_DIV2_GSM_SEL	CLKSQ_DIV2_USB_SEL	CLKSQ_DIV2_DSP_SEL	CLKSQ_DIV2_MCU_SEL
Type	R/W				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0000				0	0	0	0	1	1	1	0	0	0	0	0

Set this register for CLKSQ circuit configuration controls.

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RG_CLKSQTEST_EN CLKSQ test mode enable control

SRCCLK Off-chip temperature-compensated voltage controlled oscillator (TCVCXO) frequency identifier.

- **0** 13MHz
- **1** 26MHz

RG_CLKSQ_SIN_PWDB CLKSQ power down control for single-end circuit.

- **0** power-down
- **1** power-on

RG_CLKSQ_DIFF_PWDB CLKSQ power down control for differential circuit.

- **0** power-down
- **1** power-on

RG_CLKSQ_CKSEL CLKSQ normal mode clock selection

- **0** select differential type clksq_out
- **1** select single-end type clksq_out

CLKSQ_DIV2_GSM_SEL Control the clock divider for GSM clock domain

- **0** clksq divider 2 bypassed
- **1** clksq divider 2 not bypassed

CLKSQ_DIV2_USB_SEL Control the clock divider for USB clock domain

- **0** clksq divider 2 bypassed
- **1** clksq divider 2 not bypassed

CLKSQ_DIV2_DSP_SEL Control the clock divider for DSP clock domain

- **0** clksq divider 2 bypassed
- **1** clksq divider 2 not bypassed

CLKSQ_DIV2_MCU_SEL Control the clock divider for MCU clock domain

- **0** clksq divider 2 bypassed
- **1** clksq divider 2 not bypassed

0x8300_0200 PLL Control Register 0 PLL_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_PLL_RESB				RG_PLL_RESA					RG_PLLVLDO_CALI				RG_PLLBIAS_CALI		
Type	R/W				R/W				R/W	R/W			R/W	R/W		
Reset	0000				0000				0	000			0	000		

Set this register for PLL circuit configuration controls.

RG_PLL_RESB Reserved (for 1.2V register)

RG_PLL_RESA Reserved (for 2.8V register)

RG_PLLVLDO_CALI PLL LDO output voltage calibration

- **0** [Description for field value 0]
- **1** [Description for field value 1]

RG_PLLBIAS_CALI Input bias current calibration

- **0** [Description for field value 0]
- **1** [Description for field value 1]

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0x8300_0204 PLL Control Register 1 PLL_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_PLLTEST_EN				RG_PLLTEST_CKSEL			MPLL_FHTC_EN	MPLL_FHTC		GPLLSEL	UPLLSEL	DPLLSEL		MPLLSEL	
Type	R/W				R/W		R/W	R/W	R/W		R/W	R/W	R/W		R/W	
Reset	0000				00		0	1	01		0	0	00		00	

Set this register for PLL circuit configuration controls.

RG_PLLTEST_EN PLL test mode enable control

- **0** [Description for field value 0]
- **1** [Description for field value 1]

RG_PLLTEST_CKSEL PLL test mode clock selection

- **0** [Description for field value 0]
- **1** [Description for field value 1]

MPLL_FHTC_EN Enable setting for time constraint for MPLL frequency hopping delay switch

- **0** disable
- **1** enable

MPLL_FHTC Time constraint for MPLL frequency hopping delay switch setting

- **00** 80uS
- **01** 100uS
- **10** 150uS
- **11** 200uS

GPLLSEL Select GSM clock source.

- **0** bypass PLL, use CLKSQ or CLKSQ_DIV2, the default value after chip power up
- **1** use UPLL (fixed 104MHz clock)

UPLLSEL Select GSM clock source.

- **0** bypass PLL, use CLKSQ or CLKSQ_DIV2, the default value after chip power up
- **1** Using USB PHY (fixed 30MHz)

DPLLSEL Select GSM clock source.

- **00** bypass PLL, use CLKSQ or CLKSQ_DIV2, the default value after chip power up
- **01** reserved
- **10** use MPLL (floating 104MHz clock)
- **11** use UPLL (fixed 104MHz clock)

MPLLSEL Select GSM clock source.

- **00** bypass PLL, use CLKSQ or CLKSQ_DIV2, the default value after chip power up
- **01** reserved
- **10** use MPLL (floating 104MHz clock)
- **11** use UPLL (fixed 104MHz clock)

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0x8300_0208 UPLL Control Register 0 UPLL_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_UPLL_VCOBAND		RG_UPLL_CMDIV					RG_UPLL_CPI			RG_UPLL_CPP			
Type	R/W	R/W	R/W		R/W				R/W	R/W			R/W			
Reset	0	0	01		0001				0	011			0110			

Set this register for UPLL circuit configuration controls.

RG_UPLL_VCOBAND UPLL vco band selection

- **00** [Description for field value 0]
- **01** [Description for field value 1]
- **10** [Description for field value 0]
- **11** [Description for field value 1]

RG_UPLL_CMDIV Capacitor multiplication number for UPLL

- **0** [Description for field value 0]
- **1** [Description for field value 1]
- **....**
- **6** [Description for field value 0]
- **7** [Description for field value 1]

RG_UPLL_CPI UPLL i-path BW control

- **0** [Description for field value 0]
- **1** [Description for field value 1]
- **....**
- **6** [Description for field value 0]
- **7** [Description for field value 1]

RG_UPLL_CPP UPLL p-path BW control

- **0** [Description for field value 0]
- **1** [Description for field value 1]
- **....**
- **14** [Description for field value 0]
- **15** [Description for field value 1]

0X8300_020C UPLL Control Register 1 UPLL_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_UPLL_PORELATCHB_EN	RG_UPLL_PORELATCHA_EN	RG_UPLL_FBRELATCH_EN	RG_UPLL_PWDB	RG_UPLL_RST
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0

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Set this register for UPLL circuit configuration controls.

RG_UPLL_PORELATCHB_EN UPLL post divider A relatch function enable
- **0** [Description for field value 0]
- **1** [Description for field value 1]

RG_UPLL_PORELATCHA_EN UPLL post divider B relatch function enable
- **0** [Description for field value 0]
- **1** [Description for field value 1]

RG_UPLL_FBRELATCH_EN UPLL feedback divider relatch function enable
- **0** [Description for field value 0]
- **1** [Description for field value 1]

RG_UPLL_PWDB UPLL power down setting
- **0** power-down
- **1** power-on

RG_UPLL_RST Reset of UPLL
- **0** normal operation
- **1** reset

0x8300_0210 MPLL Control Register 0 MPLL_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_MPLL_VCOBAND		RG_MPLL_CMDIV					RG_MPLL_CPI			RG_MPLL_CPP			
Type	R/W	R/W	R/W		R/W				R/W	R/W			R/W			
Reset	0	0	00		1000				0	001			0010			

Set this register for MPLL circuit configuration controls.

RG_MPLL_VCOBAND MPLL vco band selection
- **0** [Description for field value 0]
- **1** [Description for field value 1]

RG_MPLL_CMDIV Capacitor multiplication number for MPLL
- **0** [Description for field value 0]
- **1** [Description for field value 1]

RG_MPLL_CPI MPLL i-path BW control
- **0** [Description for field value 0]
- **1** [Description for field value 1]

RG_MPLL_CPP MPLL p-path BW control
- **0** [Description for field value 0]
- **1** [Description for field value 1]

0x8300_0214 MPLL Control Register 1 MPLL_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	RG_MPLL_FBDIV			RG_MPLL_PORELATCH_EN	RG_MPLL_FBRELATCH_EN		PLL_TDMA	RG_MPLL_PWDB	RG_MPLL_RST
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	11001110	0	0	1	1	0	0	0	0

Set this register for MPLL circuit configuration controls.

RG_MPLL_FBDIV MPLL feedback divider ratio adjustment

**** MPLL frequency = 0.5MHz*(RG_MPLL_FBDIV[7:0]+2)

**** default at 104MHz

RG_MPLL_PORELATCH_EN MPLL post divider relatch function enable

0 [Description for field value 0]

1 [Description for field value 1]

RG_MPLL_FBRELATCH_EN MPLL feedback divider relatch function enable

0 [Description for field value 0]

1 [Description for field value 1]

PLL_TDMA The mode for MPLL frequency setting method

0: immediately setting mode, the MPLL would use RG_MPLL_FBDIV[7:0] for frequemcy setting

1: TDMA strobe setting mode, there are 6 strobe setting value at WB0_MPLL_FBDIV, WB1_MPLL_FBDIV, WB2_MPLL_FBDIV, WB3_MPLL_FBDIV, WB4_MPLL_FBDIV, WB5_MPLL_FBDIV (0x8300_0220 ~ 0x8300_0228)

0 disable

1 enable

RG_MPLL_PWDB MPLL power down setting

0 power-down

1 power-on

RG_MPLL_RST Rset of MPLL

0 normal operation

1 reset

0x8300_0220 MPLL TDMA Write Buffer Register 0&1 MPLL_TDMAWB01

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WB1_MPLL_FBDIV								WB0_MPLL_FBDIV							
Type	R/W								R/W							
Reset	0								0							

Set this register for MPLL circuit configuration controls.

WB1_MPLL_FBDIV MPLL TDMA write buffer 1 for frequency setting

WB0_MPLL_FBDIV MPLL TDMA write buffer 0 for frequency setting

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0x8300_0224 MPLL TDMA Write Buffer Register 2&3 MPLL_TDMAWB23

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WB3_MPLL_FBDIV								WB2_MPLL_FBDIV							
Type	R/W								R/W							
Reset	0								0							

Set this register for MPLL circuit configuration controls.

WB3_MPLL_FBDIV MPLL TDMA write buffer 3 for frequency setting
WB2_MPLL_FBDIV MPLL TDMA write buffer 2 for frequency setting

0x8300_0228 MPLL TDMA Write Buffer Register 4&5 MPLL_TDMAWB45

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WB5_MPLL_FBDIV								WB4_MPLL_FBDIV							
Type	R/W								R/W							
Reset	0								0							

Set this register for MPLL circuit configuration controls.

WB5_MPLL_FBDIV MPLL TDMA write buffer 5 for frequency setting
WB4_MPLL_FBDIV MPLL TDMA write buffer 4 for frequency setting

0x8001_0114 Sleep Control Register SLEEP_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												MODEM	SLAVE DSP	HOST DSP	AHB	MCU
Type												WO	WO	WO	WO	WO
Reset												0	0	0	0	0

MCU Stop the MCU Clock to force MCU Processor entering sleep mode. MCU clock will be resumed as long as there comes an interrupt request or system is reset.
- **0** MCU Clock is running
- **1** MCU Clock is stopped

AHB Stop the AHB Bus Clock to force the entire bus entering sleep mode. AHB clock will be resumed as long as there comes an interrupt request or system is reset.
- **0** AHB Bus Clock is running
- **1** AHB Bus Clock is stopped

HOST/SLAVE DSP Stop the DSP Clock.
- **0** DSP Bus Clock is running
- **1** DSP Bus Clock is stopped

MODEM Stop modem hardware clock
- **0** modem hardware clock is running
- **1** modem hardware clock is stopped

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0x8001_0118 MCU Clock Control Register MCUCLK_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MODEM_FSEL				ARM_FSEL				SRCCLK				MCU_FSEL			
Type	R/W				R/W				R/W				R/W			
Reset	3				3				1				3			

MCU_FSEL MCU clock frequency selection. This control register is used to control the output clock frequency of MCU Dynamic Clock Manager. The clock frequency is from 13MHz to 52MHz. The waveform of the output clock is shown in **Figure 103.**

0 13MHz
1 26MHz
2 39MHz
3 52MHz
4 65MHz
5 78MHz
6 91MHz
7 104MHz
Others reserved

When MCU Clock Source bypass PLL (MPLL_SEL[1]==0), the output frequency is controlled by SRCCLK ,CLKSQ_DIV2_MCU , MPLL_SEL[0] and MCU_FSEL[0]

SRCCLK	CLKSQ_DIV2_MCU	MPLL_SEL[0]	MCU_FSEL[0]	
0	**0**	**x**	**x**	13Mhz
1	**1**	**0**	**0**	13Mhz
1	**1**	**1**	**1**	26Mhz

Other illegal

SRCCLK off-chip temperature-compensated voltage controlled oscillator (TCVCXO) frequency identifier.

0 13MHz
1 26MHz

ARM_FSEL ARM clock frequency selection. This control register is used to control the output clock frequency of ARM Dynamic Clock Manager. The clock frequency is from 13MHz to 104MHz.

0 13MHz
1 26MHz
2 39MHz
3 52MHz
4 65MHz
5 78MHz
6 91MHz
7 104MHz
Others reserved

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In MT6253, due to platform design to accommodate 2:1 and 1:1 ARM/AHB frequency ratio, specific sequence must be followed. The principle is layer 2 masters must keep silent at the moment when DCM setting changed. There will be two sequences: one is for totally SW control, the other is HW aided control. The later control scheme can avoid interrupt mask modification which is mandatory in SW control sequence, and also provide debug visibility.

For totally SW control (default): Before the flowing program, IMASK shall be turn on, ie. No interrupt allowed to interfere break the sequence

while ((*LYR2_EMPTY && 0x8000) == 0x8000); // see if HW is still processing the previous clock change
TEMP_VARIABLE = *ARB_1T_EN & 0x8000; // get current MSB of ARB_1T_EN, WRAP_DIS
*LYR2_EMPTY_EN = *LYR2_EMPTY_EN | 0x0001; // turn on LYR2_EMPTY_EN(0x8001_0018 bit 0), which trigger the bus arbitrator to forbid all transactions from masters on layer2
while ((*LYR2_EMPTY && 0x8000) == 0x0000); // wait until Layer 2 really goes idle
*MCUCLOCK_CON = NEW_VALUE;
while ((*ARB_1T_EN & 0x8000) = = TEMP_VARIABLE); // keep polling ARB_1T_EN (0x8001_0714 bit 15) until the MSB being toggled
*LYR2_EMPTY_EN = *LYR2_RMPTY_EN & 0xfffe; // turn off LYR2_EMPTY_EN

For HW-aided control;

*LYR2_EMPTY_EN = *LYR2_RMPTY_EN | 0x8000; // one-time programming, turn on HW-aided control (0x8001_0018 bit 15)
while ((*LYR2_EMPTY && 0x8000) == 0x8000); // see if DCM controller is still busy for previous DCM setting. This while loop only take place when consecutive DCM setting occurs
*MCUCLOCK_CON = NEW_VALUE; // The new setting will trigger LYR2_EMPTY_EN automatically by HW. NEW_VALUE will not take effect until LYR2_EMPTY signal is detected being true by HW, and at the same time LYR2_EMPTY_EN will also be automatically pull-down

Please note that the clock period of 39MHz is not uniform. The shortest period of 39MHz clock is the same as the period of 52MHz. As a result, the wait states of external interfaces, such as EMI, NAND, and so on, have to be configured based on 52MHz timing. Therefore, the MCU performance executing in external memory at 39MHz may be worse than at 26MHz. 65Mhz, 78MHz and 91MHz are not uniform clocks, either.

Also note that the maximum latency of clock switch is 8 104MHz-clock periods. Software provides at least 8T locking time after clock switch command.

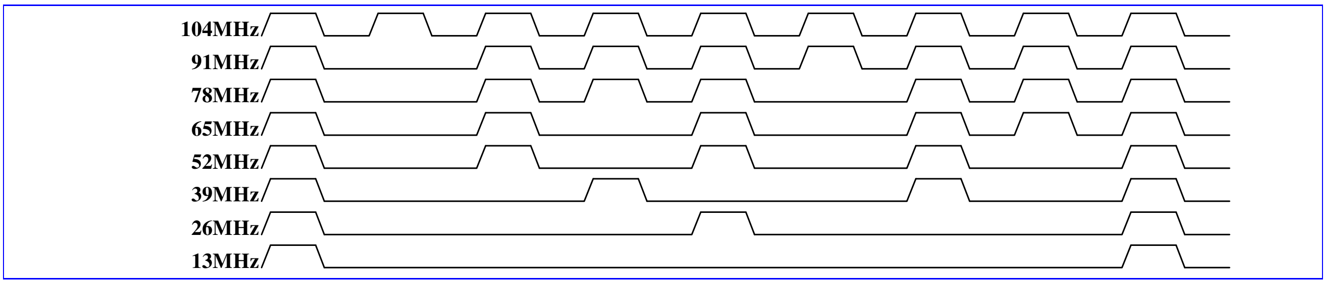

Figure 103 Output of Dynamic Clock Manager

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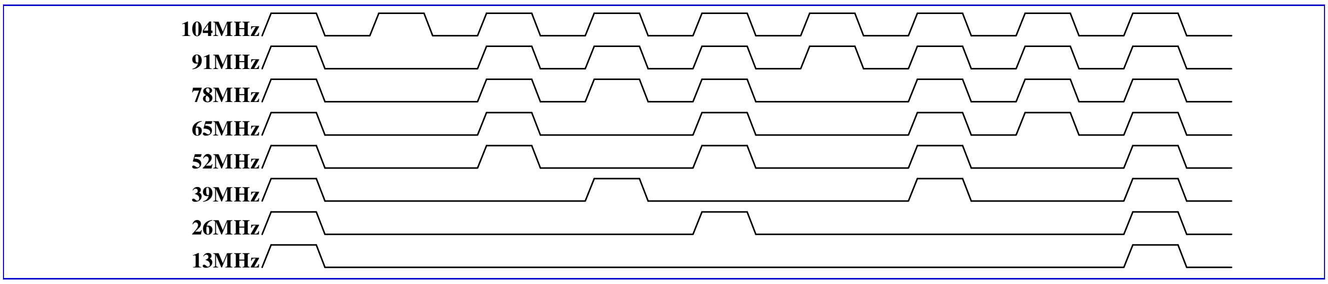
0x8001_011C DSP Clock Control Register DSPCLK_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DSP1_FSEL				DSP1_FSEL			
Type									R/W				R/W			
Reset									3				3			

DSP_FSEL DSP clock frequency selection. This control register is used to control the output clock frequency of DSP Dynamic Clock Managers. The clock frequency is from 13MHz to 104MHz. Note that 39MHz, 65MHz, 78MHz, and 91MHz are not a uniform period clock rate.

0 13MHz
1 26MHz
2 39MHz
3 52MHz
4 65MHz
5 78MHz
6 91MHz
7 104MHz
Others reserved



11.2 Reset Generation Unit (RGU)

Figure 104 shows the reset scheme used in MT6253. MT6253 provides three kinds of resets: hardware reset, watchdog reset, and software reset.

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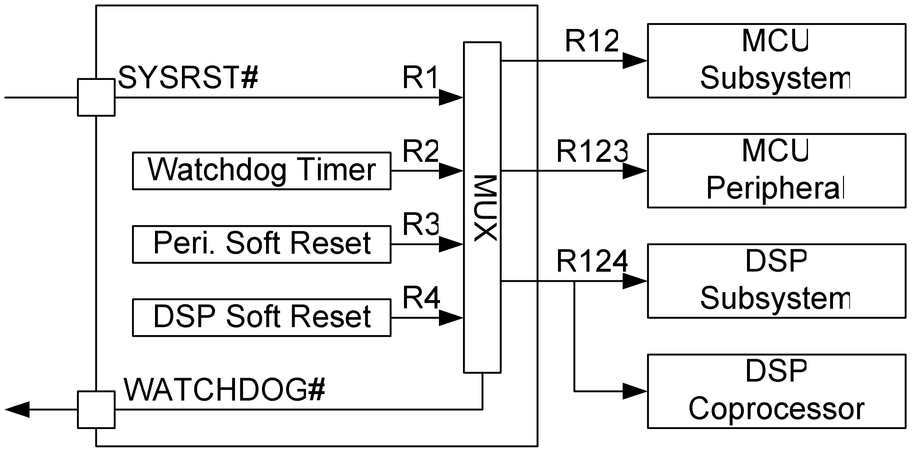

Figure 104 Reset Scheme Used in MT6253

11.2.1 General Description

11.2.1.1 Hardware Reset

This reset is input through the SYSRST# pin, which is driven low during power-on. The hardware reset has a global effect on the chip: all digital and analog circuits are initialized, except the Real Time Clock module. The initial states of the MT6253 sub-blocks are as follows:.

- All analog circuits are turned off.
- All PLLs are turned off and bypassed. The 13 MHz system clock is the default time base.

11.2.1.2 Watchdog Reset

A watchdog reset is generated when the Watchdog Timer expires: the MCU software failed to re-program the timer counter in time. This situation is typically induced by abnormal software execution, which can be aborted by a hardwired watchdog reset. Hardware blocks that are affected by the watchdog reset are:

- MCU subsystem,
- DSP subsystem, and
- External components (trigged by software).

11.2.1.3 Software Resets

Software resets are local reset signals that initialize specific hardware components. For example, if hardware failures are detected, the MCU or DSP software may write to software reset trigger registers to reset those specific hardware modules to their initial states.

The following modules have software resets.

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- DSP Core
- DSP Coprocessors

11.2.2 Register Definitions

REGISTER ADDRESS	REGISTER NAME	SYNONYM
0x8003_0000	Watchdog Timer Control Register	WDT_MODE
0x8003_0004	Watchdog Time-Out Interval Register	WDT_LENGTH
0x8003_0008	Watchdog Timer Restart Register	WDT_RESTART
0x8003_000C	Watchdog Timer Status Register	WDT_STA
0x8003_0010	CPU Peripheral Software Reset Register	SW_PERIPH_RSTN
0x8003_0014	DSP Software Reset Register	SW_DSP_RSTN
0x8003_0018	Watchdog Timer Reset Signal Duration Register	WDT_RSTINTREVAL
0x8003_001C	Watchdog Timer Software Reset Register	WDT_SWRST

Table 74 RGU Register Map

0x8003_0000 Watchdog Timer Control Register WDT_MODE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY[7:0]											AUTO-RESTART	IRQ	EXTEN	EXTPOL	ENABLE
Type	WO											R/W	R/W	R/W	R/W	R/W
Reset												0	0	0	0	1

ENABLE Enables the Watchdog Timer.

0 Disables the Watchdog Timer.

1 Enables the Watchdog Timer.

EXTPOL Defines the polarity of the external watchdog pin.

0 Active low.

1 Active high.

EXTEN Specifies whether or not to generate an external watchdog reset signal.

0 The watchdog does not generate an external watchdog reset signal.

1 If the watchdog counter reaches zero, an external watchdog signal is generated.

IRQ Issues an interrupt instead of a Watchdog Timer reset. For debug purposes, RGU issues an interrupt to the MCU instead of resetting the system.

0 Disable.

1 Enable.

AUTO-RESTART Restarts the Watchdog Timer counter with the value of WDT_LENGTH while task ID is written into Software Debug Unit.

0 Disable. The counter restarts by writing KEY into the WDT_RESTART register.

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1 Enable. The counter restarts by writing KEY into the WDT_RESTART register or by writing task ID into the software debug unit.

KEY Write access is allowed if KEY=0x22.

0x8003_0004 Watchdog Time-Out Interval Register WDT_LENGTH

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TIMEOUT[10:0]											KEY[4:0]				
Type	R/W											WO				
Reset	111_1111_1111b															

KEY Write access is allowed if KEY=08h.

TIMEOUT The counter is restarted with {TIMEOUT [10:0], 1_1111_1111b}. Thus the Watchdog Timer time-out period is a multiple of 512*T_{32k}=15.6ms.

0x8003_0008 Watchdog Timer Restart Register WDT_RESTART

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY[15:0]															
Type	WO															
Reset																

KEY Restart the counter if KEY=1971h.

0x8003_000C Watchdog Timer Status Register WDT_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDT	SW_WDT														
Type	RO	RO														
Reset	0	0														

WDT Indicates the cause of the watchdog reset.

- **0** Reset not due to Watchdog Timer.
- **1** Reset because the Watchdog Timer time-out period expired.

SW_WDT Indicates if the watchdog was triggered by software.

- **0** Reset not due to software-triggered Watchdog Timer.
- **1** Reset due to software-triggered Watchdog Timer.

NOTE: A system reset does not affect this register. This bit is cleared when the WDT_MODE register is written.

0x8003_0010 CPU Peripheral Software Reset Register SW_PERIPH_RSTN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DMARST							KEY							
Type		R/W														
Reset		0														

KEY Write access is allowed if KEY=37h.

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DMARST Reset the DMA peripheral.

- **0** No reset.
- **1** Invoke a reset.

0x8003_0014 DSP Software Reset Register SW_DSP_RSTN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RST								KEY							
Type	R/W															
Reset	0															

KEY Write access is allowed if KEY=48h.

RST Controls the DSP System Reset Control.

- **0** No reset.
- **1** Invoke a reset.

0x8003_0018 Watchdog Timer Reset Signal Duration Register WDT_RSTINTERVAL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LENGTH[11:0]											
Type					R/W											
Reset					FFFh											

LENGTH This register indicates the reset duration when Watchdog Timer times out. However, if the WDT_MODE register IRQ bit is set to 1, an interrupt is issued instead of a reset.

0x8003_001C Watchdog Timer Software Reset Register WDT_SWRST

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY[15:0]															
Type	WO															
Reset																

Software-triggered Watchdog Timer reset. If the register content matches the KEY, a watchdog reset is issued. However, if the WDT_MODE register IRQ bit is set to 1, an interrupt is issued instead of a reset.

KEY 1209h

11.3 Software Power Down Control

In addition to Pause Mode capability during Standby State, the software program can also put each peripheral independently into Power Down Mode during Active State by gating off their clock. The typical logic implementation is depicted as in **Figure 105**. For all of the configuration bits, 1 means that the function is in Power Down Mode and 0 means that it is in the Active Mode.

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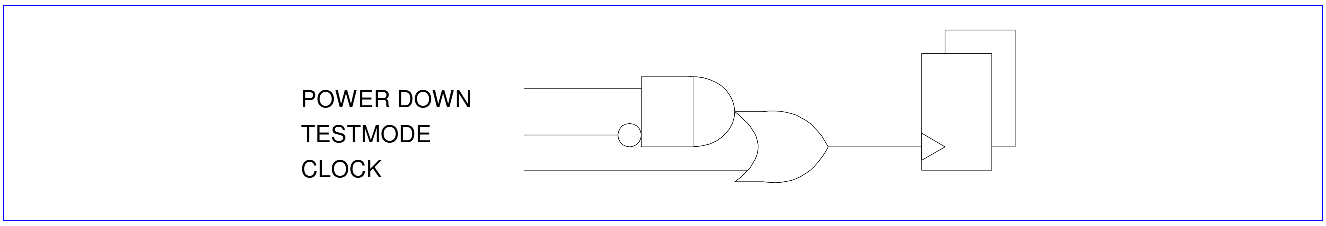

Figure 105 Power Down Control at Block Level

11.3.1 Register Definitions

0x8001_0300 Power Down Control 0 Register PDN_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRDBG2	IRDBG1		SIM2				IRDMA			WAVETABLE	GCU	USB	DMA
Type			R/W	R/W		R/W				R/W			R/W	R/W	R/W	R/W
Reset			1	1		1				1			1	1	1	1

DMA Controls the DMA Controller Power Down

GCU Controls the GCU Controller Power Down

WAVETABLE Controls the DSP Wave-Table DMA Power Down

SIM2 Controls the SIM slot 2 Controller Power Down

IRDMA Controls the IRDMA Power Down

IRDBG1 Controls the host debugger unit Power Down

IRDBG2 Controls the slave debugger Power Down

0x8001_0304 Power Down Control 1 Register PDN_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRDA	UART3	SWDBG	NFI	PWM2	TP	MSDC	UART2	LCD	ALTER	PWM1	SIM	UART1	GPIO	KP	GPT
Type	R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1		1	1	1	1	1	1	1	1	0	1	1	1

GPT Controls the General Purpose Timer Power Down

KP Controls the Keypad Scanner Power Down

GPIO Controls the GPIO Power Down

UART1 Controls the UART1 Controller Power Down

SIM Controls the SIM slot 1 Controller Power Down

PWM1 Controls the PWM1 Generator Power Down

ALTER Controls the Alerter Generator Power Down

LCD Controls the LCD Controller Power Down

UART2 Controls the UART2 Controller Power Down

MSDC Controls the Memory Card Controller Power Down

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TP Controls the Touch-panel controller Power Down
PWM2 Controls the PWM2 Generator Power Down
SWDBG Controls the SWDBG Generator Power Down
NFI Controls the NFI Generator Power Down
UART3 Controls the UART3 Controller Power Down
IRDA Controls the IRDA Controller Power Down

0x8001_0308 Power Down Control 2 Register PDN_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMSK	BBRX	I2C	AAFE	DIV	GCC	BFE	VAFE	AUXAD	FCS	APC	AFC	BPI	BSI	RTC	TDMA
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

TDMA Controls the TDMA Power Down
RTC Controls the RTC Power Down
BSI Controls the BSI Power Down. This control will not be updated until both tdma_evtval and qbit_en are asserted.
BPI Controls the BPI Power Down. This control will not be updated until both tdma_evtval and qbit_en are asserted.
AFC Controls the AFC Power Down. This control will not be updated until both tdma_evtval and qbit_en are asserted.
APC Controls the APC Power Down. This control will not be updated until both tdma_evtval and qbit_en are asserted.
FCS Controls the FCS Power Down
AUXAD Controls the AUX ADC Power Down
VAFE Controls the Audio Front End of VBI Power Down
BFE Controls the Base-Band Front End Power Down
GCU Controls the GCU Power Down
DIV Controls the Divider Power Down
AAFE Controls the Audio Front End of MP3 Power Down
I2C Controls the I2C Power Down
BBRX Controls the BB RX Power Down
GMSK Controls the GMSK Power Down

0x8001_030C Power Down Control 3 Register PDN_CON3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CAM	RESZ									SEJ	PWM3	ICE
Type				R/W	R/W									R/W	R/W	R/W
Reset				1	1									1	1	1

ICE Enables the debug feature of the ARM7EJS core. It controls the DBGEN pin of the ICEBreaker.
PWM3 Controls the PWM3 Generator Power Down
SEJ Controls the SEJ Power Down
RESZ Controls the resizer Power-Down
CAM Controls the ISP Power-Down

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0x8001_0310 Power Down Set 0 Register PDN_SET0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRDBG2	IRDBG1		SIM2				IRDMA			WAVETABLE	GCU	USB	DMA
Type			W1S	W1S		W1S				W1S			W1S	W1S	W1S	W1S

0x8001_0314 Power Down Set 1 Register PDN_SET1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRDA	UART3	SWDBG	NFI	PWM2	TP	MSDC	UART2	LCD	ALTER	PWM1	SIM	UART1	GPIO	KP	GPT
Type	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S

0x8001_0318 Power Down Set 2 Register PDN_SET2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMSK	BBRX	I2C	AAFE	DIV	GCC	BFE	VAFE	AUXAD	FCS	APC	AFC	BPI	BSI	RTC	TDMA
Type	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S

0x8001_031C Power Down Set 3 Register PDN_SET3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CAM	RESZ									SEJ	PWM3	ICE
Type				W1S	W1S									W1S		W1S

These registers are used to individually set power down control bit. Only the bits set to 1 are in effect. Setting the bits to 1 also sets the corresponding power down control bits will to 1. Otherwise, the bits keep their original value.

EACH BIT Set the Associated Power Down Control Bit to 1.

0 no effect

1 Set corresponding bit to 1

0x8001_0320 Power Down Clear 0 Register PDN_CLR0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRDBG2	IRDBG1		SIM2				IRDMA			WAVETABLE	GCU	USB	DMA
Type			W1C	W1C		W1C				W1C			W1C	W1C	W1C	W1C

0x8001_0324 Power Down Clear 1 Register PDN_CLR1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRDA	UART3	SWDBG	NFI	PWM2	TP	MSDC	UART2	LCD	ALTER	PWM1	SIM	UART1	GPIO	KP	GPT
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C

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0x8001_0328 Power Down Clear 2 Register PDN_CLR2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMSK	BBRX	SCCB	AAFE	DIV	GCC	BFE	VAFE	AUXAD	FCS	APC	AFC	BPI	BSI	RTC	TDMA
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C

0x8001_032C Power Down Clear 3 Register PDN_CLR3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CAM	RESZ									SEJ	PWM3	ICE
Type				W1C	W1C									W1C	W1C	W1C

These registers are used to individually clear power down control bit. Only the bits set to 1 are in effect. Setting the bits to 1 also sets the corresponding power down control bits to 0. Otherwise, the bits keep their original value.

EACH BIT Clear the Associated Power Down Control Bit.

- **0** no effect
- **1** Set corresponding bit to 0

0x8001_0200 Debug-mode Select IDN_SEL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									IRWIN_CON			TDMA_IDN				
Type									R/W			R/W				
Reset									0			0				

TDMA_IDN Enable TDMA debug message output. The debug mode should go accompanied with appropriate GPIO setting

- **0** Disable debug mode
- **1** Enable debug mode

IRWIN_CON Enable arbitrator favor for IRDMA

- **0** Disable the IRDMA favored mode
- **1** Enable the IRDMA favored mode

0x8001_0114 Sleep Control SLEEP_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PDN_MODEM	PDN_DSP2	PDN_DSP1	AHB_SLEEP	MCU_SLEEP
Type												R/W	R/W	R/W	R/W	R/W
Reset												0	0	0	0	0

MCU_SLEEP_REQUEST Power down AHB cycles launched by MCU

- **0** no effect
- **1** sleep request

AHB_SLEEP_REQUEST Force AHB for sleep mode

- **0** no effect

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1 sleep request

PDN_DSP1 Turn off host DSP's clock

PDN_DSP2 Turn off slave DSP's clock

PDN_MODEM Turn off modem hardware clock

0x8001_0010 Software Misc. usage, low byte SW_MISC_L

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SW_MISC_L															
Type	R/W															
Reset	0															

0x8001_0014 Software Misc. usage, high byte SW_MISC_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FAB_CODE								SW_MISC_H							
Type	RO								R/W							
Reset	0								0							

0x8001_0018 AHB Layer2 Hold Master Enable LYR2_EMPTY_EN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LYR2_EMPTY_HW_CON															LYR2_EMPTY_EN
Type	R/W															R/W
Reset	0															0

0x8001_001C AHB Layer2 Hold Master Status LYR2_EMPTY

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LYR2_EMPTY_HW_BUSY															LYR2_EMPTY
Type	R															R
Reset	0															0

LYR2_EMPTY_EN : This bit is used to force layer2 enter idle status and hold other masters request.

1: enable

0: disable

LYR2_EMPTY : This bit is used to watch if layer2 enter idle status after LYR2_EMPTY_EN was set

1: idle already

0: not idle yet

The frequency switch procedure is described as follow:

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At 6253 we have only two situation of bus frequency, that is (52:104) or (13:13) or say 1:2 or 1:1 between AHB bus and EMI. No matter SW want to switch bus frequency from (1:1) to (1:2) or from (1:2) to (1:1), SW must force AHB bus into idle status first and then turn on switch procedure. SW must set LYR2_EMPTY_EN first and wait LYR2_EMPTY = 1 then AHB bus has entered idle status and SW can go on switch frequency. After switching frequency SW must remember to set LYR2_EMPTY_EN = 0 to release bus for other masters.

0x8001_0714 Arbitration 1T enable ARB_1T_EN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WRAP_DIS	EMI_SPPED_104MHZ	EMI_SPPED_52MHZ	EMI_SPPED_13MHZ												ARB_1T_EN
Type	RO	RO	RO	RO												R/W
Reset	1	0	0	1												0

WRAP_DIS Indicate the MCU/BUS clock ratio is whether 1:1 or 2:1

- **0** 2:1
- **1** 1:1

EMI_SPEED_104MHz Indicate the EMI runs at 104MHz, useful for DCM latency before new EMI setting can apply

- **0** not 104MHz
- **1** 104MHz

EMI_SPEED_52MHz Indicate the EMI runs at 52MHz, useful for DCM latency before new EMI setting can apply

- **0** not 52MHz
- **1** 52MHz

EMI_SPEED_13MHz Indicate the EMI runs at 13MHz, useful for DCM latency before new EMI setting can apply

- **0** not 13MHz
- **1** 13MHz

0x8001_0408 Slow-down control SLOWDN_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											IR_SINGLE	WT_SINGLE	DBG2_SD_EN	DBG1_SD_EN	WT_SD_EN	IR_SD_EN
Type											R/W	R/W	R/W	R/W	R/W	R/W
Reset											0	0	1	1	0	1

IR_SD_EN Enable IRDMA slow-down. The slow-down mechanism is enabled only when the bit is true and the corresponding slow-down ratio is non-zero

- **0** Disable
- **1** Enable

WT_SD_EN Enable Wavetable DMA slow-down. The slow-down mechanism is enabled only when the bit is true and the corresponding slow-down ratio is non-zero

DBG1_SD_EN Enable IRDBG1 DMA slow-down. The slow-down mechanism is enabled only when the bit is true and the corresponding slow-down ratio is non-zero

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DBG2_SD_EN Enable IRDBG1 DMA slow-down. The slow-down mechanism is enabled only when the bit is true and the corresponding slow-down ratio is non-zero

WT_SINGLE Force Wavetable DMA issue SINGLE request only

- **0** No force
- **1** Force SINGLE type access

IR_SINGLE Force IRDMA issue SINGLE request only

0x8001_040C Slow-down ratio for wavetable and IRDMA IRDMA_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_SD_RATIO								IRDMA_SD_RATIO							
Type	R/W								R/W							
Reset	0								0							

IRDMA_SD_RATIO The ratio of IRDMA slow-down. The ratio manes that IRDMA issues request no faster than IRDMA_SD_RATIO x 4 bus cycles.

WAVE_SD_RATIO The ratio of Wavetable DMA slow-down. The ratio manes that Wavetable DMA issues request no faster than IRDMA_SD_RATIO bus cycles.

0x8001_0410 Slow-down ratio for debugger IRDBG_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG1_SD_RATIO								DBG1_SD_RATIO							
Type	R/W								R/W							
Reset	0								0							

DBG1_SD_RATIO The ratio of IRDBG1 slow-down. The ratio manes that IRDBG1 issues request no faster than IRDMA_SD_RATIO x 4 bus cycles.

DBG2_SD_RATIO The ratio of IRDBG2 slow-down. The ratio manes that IRDBG2 issues request no faster than IRDMA_SD_RATIO bus cycles.

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12 Analog Front-end & Analog Blocks

12.1 General Description

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates APB bus write and read cycle for specific addresses related to analog front-end control. During writing or reading of any of these control registers, there is a latency associated with transferring of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. The Analog Blocks includes the following analog function for complete GSM/GPRS base-band signal processing:

1. *Base-band RX*: For I/Q channels base-band A/D conversion
2. *Base-band TX*: For I/Q channels base-band D/A conversion and smoothing filtering, DC level shifting
3. *RF Control*: One DAC for automatic power control (APC) is included. It's output is provided to external RF power amplifier.
4. *Auxiliary ADC*: Providing an ADC for battery and other auxiliary analog function monitoring
5. *Audio mixed-signal blocks:* It provides complete analog voice signal processing including microphone amplification, A/D conversion, D/A conversion, earphone driver, and etc. Besides, dedicated stereo D/A conversion and amplification for audio signals are included).
6. *Clock Generation*: A clock squarer for shaping system clock, and three PLLs that provide clock signals to DSP, MCU, and USB units are included
7. *XOSC32*: It is a 32-KHz crystal oscillator circuit for RTC application Analog Block Descriptions

12.1.1 BBRX

12.1.1.1 Block Descriptions

The receiver (RX) performs base-band I/Q channels downlink analog-to-digital conversion:

1. *Analog input multiplexer:* For each channel, a 4-input multiplexer that supports offset and gain calibration is included.
2. *A/D converter:* Two 14-bit sigma-delta ADCs perform I/Q digitization for further digital signal processing.

12.1.1.2 Functional Specifications

The functional specifications of the base-band downlink receiver are listed in the following table.

Symbol	Parameter	Min	Typical	Max	Unit
N	Resolution		14		Bit
FC	Clock Rate		26		MHz

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FS	Output Sampling Rate		13/12		MSPS
	Input Swing When GAIN='00' When GAIN='01' When GAIN='10' When GAIN='11'		0.8*AVDD 0.4*AVDD 0.57*AVDD 0.33*AVDD		Vpk,diff
OE	Offset Error		+/- 10		mV
FSE	Full Swing Error		+/- 30		mV
	I/Q Gain Mismatch			0.5	dB
SINAD	Signal to Noise and Distortion Ratio - 45kHz sine wave in [0:90] kHz bandwidth - 145kHz sine wave in [10:190] kHz bandwidth	65 65			dB dB
ICN	Idle channel noise - [0:90] kHz bandwidth - [10:190] kHz bandwidth			-74 -70	dB dB
DR	Dynamic Range - [0:90] kHz bandwidth - [10:190] kHz bandwidth	74 70			dB dB
RIN	Input Resistance	75			kΩ
DVDD	Digital Power Supply	1.1	1.2	1.3	V
AVDD	Analog Power Supply	2.5	2.8	3.1	V
T	Operating Temperature	-20		80	℃
	Current Consumption Power-up Power-Down		5 5		mA µA

Table 75 Base-band Downlink Specifications

12.1.2 BBTX

12.1.2.1 Block Descriptions

The transmitter (TX) performs base-band I/Q channels up-link digital-to-analog conversion. Each channel includes:

1. *10-Bits D/A Converter:* It converts digital GMSK modulated signals to analog domain. The input to the DAC is sampled at 4.33-MHz rate with 10-bits resolution.

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2. *Smoothing Filter:* The low-pass filter performs smoothing function for DAC output signals with a 350-kHz 3rd-order Butterworth frequency response.

12.1.2.2 Function Specifications

The functional specifications of the base-band uplink transmitter are listed in the following table.

Symbol	Parameter	Min	Typical	Max	Unit
N	Resolution		10		Bit
FS	Sampling Rate		4.33		MSPS
SINAD	Signal to Noise and Distortion Ratio	57	60		dB
	Output Swing	0.26*AVDD		0.45*AVDD	V
VOCM	Output CM Voltage	0.34*AVDD	0.5*AVDD	0.62*AVDD	V
	Output Capacitance			20	PF
	Output Resistance	10			KΩ
DNL	Differential Nonlinearity		+/- 0.5		LSB
INL	Integral Nonlinearity		+/- 1.0		LSB
OE	Offset Error		+/- 15		mV
FSE	Full Swing Error		+/- 30		mV
FCUT	Filter –3dB Cutoff Frequency	300	350	400	KHz
ATT	Filter Attenuation at 100-KHz 270-KHz 4.33-MHz	0.01 1.81 69.4	0.0 0.85 65.7	0.0 0.39 61.9	dB dB dB
	I/Q Gain Mismatch		+/- 0.5		dB
	I/Q Gain Mismatch Correction Range	-0.96		+0.84	dB
DVDD	Digital Power Supply	1.1	1.2	1.3	V
AVDD	Analog Power Supply	2.5	2.8	3.1	V
T	Operating Temperature	-20		80	℃
	Current Consumption Power-up Power-Down		5 5		mA µA

Table 76 Base-band Uplink Transmitter Specifications

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12.1.3 APC-DAC

12.1.3.1 Block Descriptions

The APC-DAC is a 10-bits DAC with output buffer aimed for automatic power control. Here blow are its analog pin assignment and functional specification tables.

12.1.3.2 Function Specifications

Symbol	Parameter	Min	Typical	Max	Unit
N	Resolution		10		Bit
FS	Sampling Rate			1.0833	MSPS
SINAD	Signal to Noise and Distortion Ratio (10-KHz Sine with 1.0V Swing & 100-KHz BW)		50		dB
	99% Settling Time (Full Swing on Maximal Capacitance)			5	µS
	Output Swing			AVDD-0.2	V
	Output Capacitance			200	pF
	Output Resistance	10			KΩ
DNL	Differential Nonlinearity		+/- 0.5		LSB
INL	Integral Nonlinearity		+/- 1.0		LSB
OE	Offset Error		+/- 10		mV
FSE	Full Swing Error		+/- 10		mV
DVDD	Digital Power Supply	1.1	1.2	1.3	V
AVDD	Analog Power Supply	2.5	2.8	3.1	V
T	Operating Temperature	-20		80	℃
	Current Consumption Power-up Power-Down		400 1		µA µA

Table 77 APC-DAC Specifications

12.1.4 Auxiliary ADC

12.1.4.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

1. *Analog Multiplexer:* The analog multiplexer selects signal from one of the seven auxiliary input pins. Real word message to be monitored, like temperature, should be transferred to the voltage domain.
2. *10 bits A/D Converter:* The ADC converts the multiplexed input signal to 10-bit digital data.

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12.1.4.2 Function Specifications

The functional specifications of the auxiliary ADC are listed in the following table.

Symbol	Parameter	Min	Typical	Max	Unit
N	Resolution		10		Bit
FC	Clock Rate		1.0833		MHz
FS	Sampling Rate @ N-Bit		1.0833/(N +1)		MSPS
	Input Swing	1.0		AVDD	V
VREFP	Positive Reference Voltage (Defined by AVDD28_RFE)	1.0		AVDD	V
CIN	Input Capacitance Unselected Channel Selected Channel			 50 1.2	fF pF
RIN	Input Resistance Unselected Channel Selected Channel	 10 1.8			 MΩ MΩ
RS	Resistor String Between AUX_REF pin & ground Power Up Power Down	35 10	50	65	KΩ MΩ
	Clock Latency		11		1/FC
DNL	Differential Nonlinearity		+0.5/-0.5		LSB
INL	Integral Nonlinearity		+1.0/-1.0		LSB
OE	Offset Error		+/- 10		mV
FSE	Full Swing Error		+/- 10		mV
SINAD	Signal to Noise and Distortion Ratio (10-KHz Full Swing Input & 13-MHz Clock Rate)		50		dB
DVDD	Digital Power Supply	1.1	1.2	1.3	V
AVDD	Analog Power Supply	2.5	2.8	3.1	V
T	Operating Temperature	-20		80	℃
	Current Consumption Power-up Power-Down		150 1		µA µA

Table 78 The Functional specification of Auxiliary ADC

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12.1.5 Audio mixed-signal blocks

12.1.5.1 Block Descriptions

Audio mixed-signal blocks (AMB) integrate complete voice uplink/downlink and audio playback functions. As shown in the following figure, it includes mainly three parts. The first consists of stereo audio DACs and speaker amplifiers for audio playback. The second is the voice downlink path, including voice-band DACs and amplifiers, which produces voice signal to earphone or other auxiliary output device. Amplifiers in these two blocks are equipped with multiplexers to accept signals from internal audio/voice or external radio sources. The last is the voice uplink path, which is the interface between microphone (or other auxiliary input device) input and MT6235 DSP. A set of bias voltage is provided for external electric microphone.

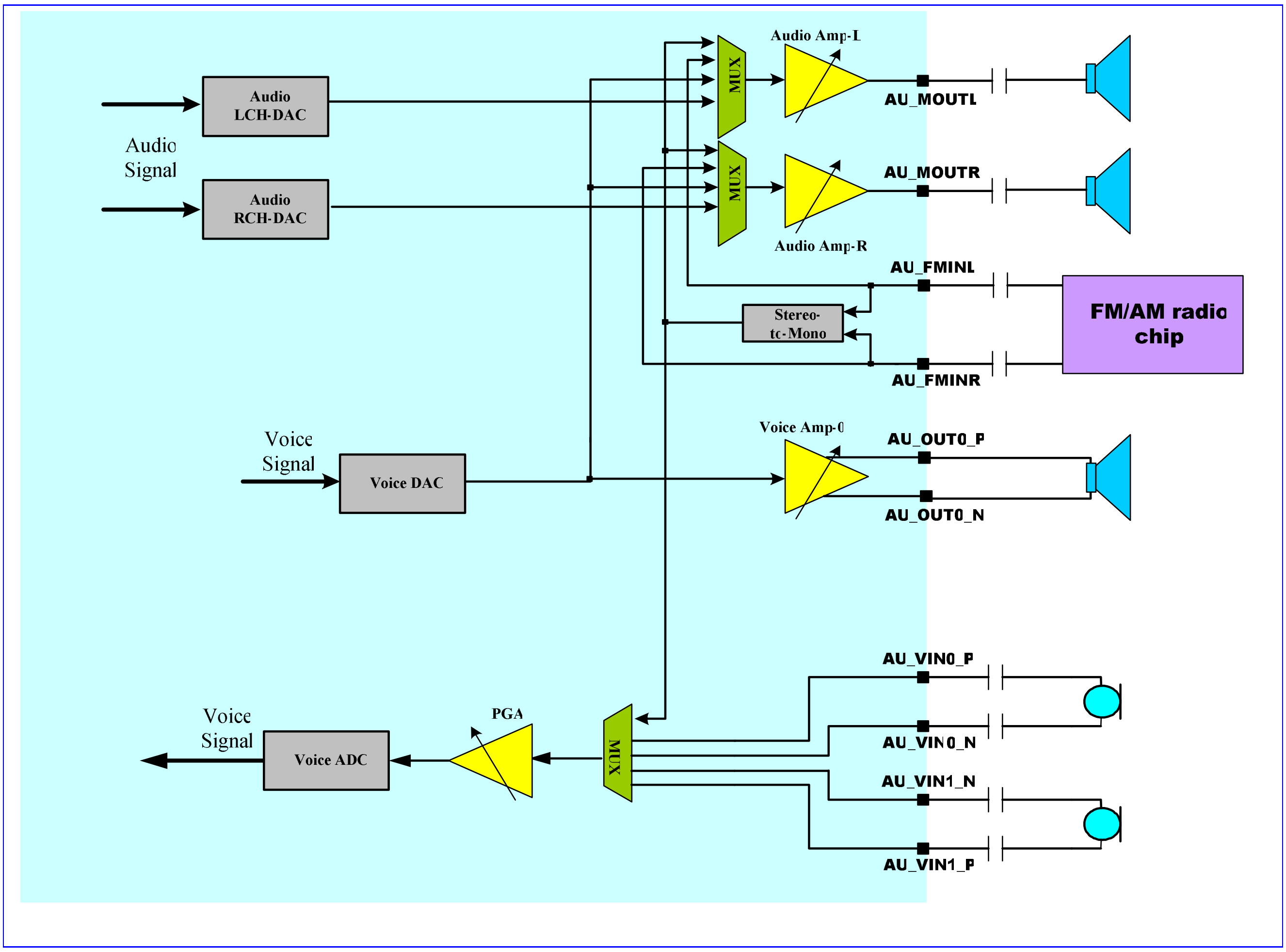

Figure 106 Block diagram of audio mixed-signal blocks

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12.1.5.2 Functional Specifications

The following table gives functional specifications of voice-band uplink/downlink blocks.

Symbol	Parameter	Min	Typical	Max	Unit
FS	Sampling Rate		6500		KHz
CREF	Decoupling Cap Between AU_VREF And ground		1		uF
DVDD	Digital Power Supply	1.08	1.2	1.32	V
AVDD	Analog Power Supply	2.5	2.8	3.1	V
T	Operating Temperature	-20		80	℃
IDC	Current Consumption		5		mA
VMIC	Microphone Biasing Voltage		1.9	2.2	V
IMIC	Current Draw From Microphone Bias Pins			2	mA
Uplink Path[1]					
IDC	Current Consumption		1.5		mA
SINAD	Signal to Noise and Distortion Ratio Input Level: -40 dbm0 Input Level: 0 dbm0	 29	 69		 dB dB
RIN	Input Impedance (Differential)	13	20	27	KΩ
ICN	Idle Channel Noise			-67	dBm0
XT	Crosstalk Level			-66	dBm0
Downlink Path[2]					
SINAD	Signal to Noise and Distortion Ratio Input Level: -40 dBm0 Input Level: 0 dBm0	 29	69		 dB dB
RLOAD	Output Resistor Load (Differential)	28			Ω
CLOAD	Output Capacitor Load			200	pF
ICN	Idle Channel Noise of Transmit Path			-67	dBm0
XT	Crosstalk Level on Transmit Path			-66	dBm0

[1] For uplink-path, not all gain setting of VUPG meets the specification listed on table, especially for the several lowest gains. The minimum gain that meets the specification is to be determined.

[2] For downlink-path, not all gain setting of VDPG meets the specification listed on table, especially for the several lowest gains. The minimum gain that meets the specification is to be determined.

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Table 79 Functional specifications of analog voice blocks

Functional specifications of the audio blocks are described in the following.

Symbol	Parameter	Min	Typical	Max	Unit
FCK	Clock Frequency		6.5		MHz
Fs	Sampling Rate	32	44.1	48	KHz
AVDD	Power Supply	2.6	2.8	3.1	V
T	Operating Temperature	-20		80	℃
IDC	Current Consumption		5		mA
PSNR	Peak Signal to Noise Ratio		80		dB
DR	Dynamic Range		80		dB
VOUT	Output Swing for 0dBFS Input Level		0.85		Vrms
THD	Total Harmonic Distortion 45mW at 16 Ω Load 22mW at 32 Ω Load			-40 -60	dB dB
RLOAD	Output Resistor Load (Single-Ended)	16			Ω
CLOAD	Output Capacitor Load			200	pF
XT	L-R Channel Cross Talk			TBD	dB

Table 80 Functional specifications of the analog audio blocks

12.1.6 Clock Squarer

12.1.6.1 Block Descriptions

In MT6253, RF is integrated and 26MHz is provided internally. Therefore, there is no dedicated input pin for 26MHz clock. For DCXO in RF, the output clock waveform is sinusoidal with too small amplitude (about several hundred mV) to make MT6253 digital circuits function well. Clock squarer is designed to convert such a small signal to a rail-to-rail clock signal with excellent duty-cycle. It provides also a pull-down function when the circuit is powered-down.

12.1.6.2 Function Specifications

The functional specification of clock squarer is shown in **Table 81**.

Symbol	Parameter	Min	Typical	Max	Unit
Fin	Input Clock Frequency		13		MHz

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Fout	Output Clock Frequency		13		MHz
Vin	Input Signal Amplitude		500	AVDD	mVpp
DcycIN	Input Signal Duty Cycle		50		%
DcycOUT	Output Signal Duty Cycle	DcycIN-5		DcycIN+5	%
TR	Rise Time on Pin CLKSQOUT			5	ns/pF
TF	Fall Time on Pin CLKSQOUT			5	ns/pF
DVDD	Digital Power Supply	1.08	1.2	1.32	V
AVDD	Analog Power Supply	2.6	2.8	3.0	V
T	Operating Temperature	-20		80	℃
	Current Consumption		TBD		MA

Table 81 The Functional Specification of Clock Squarer

12.1.6.3 Application Notes

Here below in the figure is an equivalent circuit of the clock squarer. Please be noted that the clock squarer is designed to accept a sinusoidal input signal. If the input signal is not sinusoidal, its harmonic distortion should be low enough to not produce a wrong clock output. As a reference, for a 26MHz sinusoidal signal input with amplitude of 0.2V the harmonic distortion should be smaller than 0.02V.

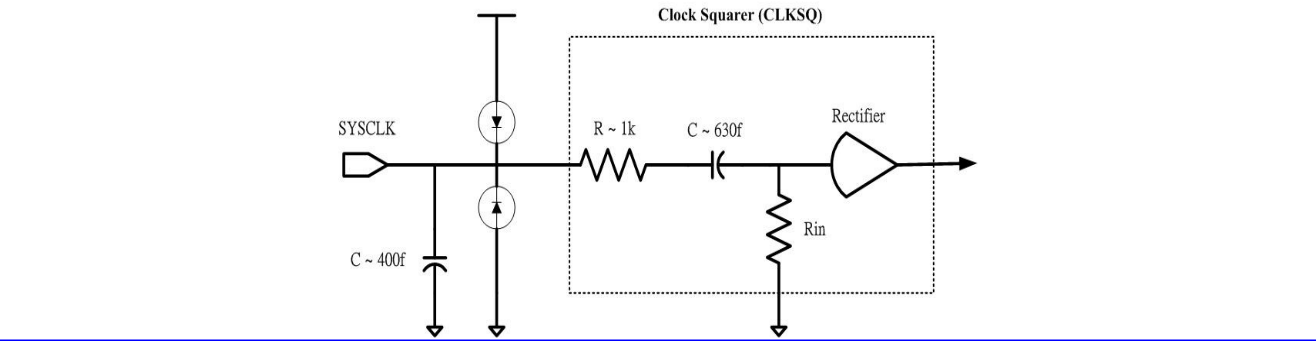

Figure 107 Equivalent circuit of Clock Square

12.1.7 Phase Locked Loop

12.1.7.1 Block Descriptions

MT6235 includes three PLLs: DSP PLL, MCU PLL, and USB PLL. DSP PLL and MCU PLL are identical and programmable to provide 104MHz and 208 MHz output clock while accepts 13MHz signal. USB PLL is designed to also accept 13MHz input clock signal and provides 48MHz output clock.

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12.1.7.2 Function Specifications

The functional specification of DSP/MCU PLL is shown in the following table.

Symbol	Parameter	Min	Typical	Max	Unit
Fin	Input Clock Frequency		2		MHz
Fout	Output Clock Frequency	104		113	MHz
	Min. output frequency step		0.5		MHz
	Settling Time for power on For band switching		160 80	200 100	us
	Output Clock Duty Cycle	45	50	55	%
	Output Clock Jitter		TBD		ps
DVDD	Digital Power Supply	1.0	1.2	1.4	V
AVDD	Analog Power Supply	2.5	2.8	3.1	V
T	Operating Temperature	-20		80	℃
	Current Consumption For AVDD For DVDD		0.8 0.2		mA
	Power Down Current Consumption For AVDD For DVDD			1 2.5	uA

Table 82 The Functional Specification of DSP/MCU PLL

The functional specification of USB PLL is shown below.

Symbol	Parameter	Min	Typical	Max	Unit
Fin	Input Clock Frequency		26		MHz
Fout	Output Clock Frequency 1		48		MHz
	Output Clock Duty Cycle	40	45	50	%
	Output Clock Jitter		TBD		ps
	Output Clock Frequency 2		104		MHz
	Output Clock Duty Cycle	45	50	55	%
	Output Clock Jitter		TBD		ps
	Settling Time		10	20	us
DVDD	Digital Power Supply	1.0	1.2	1.4	V
AVDD	Analog Power Supply	2.5	2.8	3.1	V
T	Operating Temperature	-20		80	℃

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	Current Consumption For AVDD For DVDD		1.2 0.25		mA
	Power Down Current Consumption For AVDD For DVDD			1 2.5	uA

Table 83 The Functional Specification of USB PLL

12.1.8 32-KHz Crystal Oscillator

12.1.8.1 Block Descriptions

The low-power 32-KHz crystal oscillator XOSC32 is designed to work with an external piezoelectric 32.768KHz crystal and a load composed of two functional capacitors, as shown in the following figure.

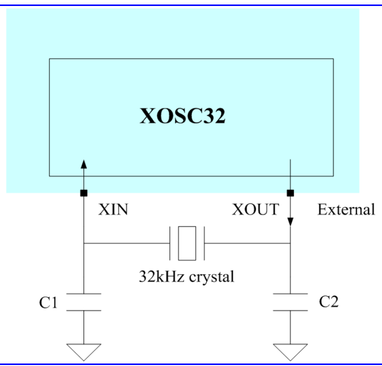

Figure 108 Block diagram of XOSC32

12.1.8.2 Functional specifications

The functional specification of XOSC32 is shown in the following table.

Symbol	Parameter	Min	Typical	Max	Unit
AVDDRTC	Analog power supply	0.8	2.8	3.0	V
Tosc	Start-up time			1	sec
Dcyc	Duty cycle	35	50		%
TR	Rise time on XOSCOUT		TBD		ns/pF
TF	Fall time on XOSCOUT		TBD		ns/pF
	Current consumption			5	µA
	Leakage current		1		µA
T	Operating temperature	-20		80	℃

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Table 84 Functional Specification of XOSC32

Here below are a few recommendations for the crystal parameters for use with XOSC32.

Symbol	Parameter	Min	Typical	Max	Unit
F	Frequency range		32768		Hz
GL	Drive level			5	uW
Δf/f	Frequency tolerance		+/- 20		ppm
ESR	Series resistance			50	KΩ
C0	Static capacitance			1.6	pF
CL[3]	Load capacitance	6		12.5	pF

Table 85 Recommended Parameters of the 32KHz crystal

12.2 ABB Register Definitions

ADDRESS	TITLE	DESCRIPTION
8301_00C	**WR_PATH**	**Switch configuration path control register**
8301_0100	**ACIF_VOICE_CON0**	**VOICE control register 0**
8301_0104	**ACIF_VOICE_CON1**	**VOICE control register 1**
8301_0108	**ACIF_VOICE_CON2**	**VOICE control register 2**
8301_010C	**ACIF_VOICE_CON3**	**VOICE control register 3**
8301_0200	**ACIF_AUDIO_CON0**	**AUDIO control register 0**
8301_0204	**ACIF_AUDIO_CON1**	**AUDIO control register 1**
8301_0208	**ACIF_AUDIO_CON2**	**AUDIO control register 2**
8301_020C	**ACIF_AUDIO_CON3**	**AUDIO control register 3**

[3] CL is the parallel combination of C1 and C2 in the block diagram. It should be adjusted according to PCB design to get a preferred frequency accuracy.

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8301_0300	ACIF_BBRX_CON	BBRX control register
8301_0400	ACIF_BBTX_CON0	BBTX control register 0
8301_0404	ACIF_BBTX_CON1	BBTX control register 1
8301_0408	ACIF_BBTX_CON2	BBTX control register 2
8301_0600	ACIF_APC_CON	APC control register
8301_0700	ACIF_AUX_CON0	AUX control register 0
8301_0704	ACIF_AUX_CON1	AUX control register 1

12.2.1 Register setting path

0x8301_000C Switch Configuring Path Control Register WR_PATH

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VSDM_PWDB	ASDM_PWDB	ESDM_PWDB	GTX_PWDB	APC_PWDB	AUX_PWDB	ABIST_MODE				VTX2AU_SEL	ACD_MODE	PMIC_WR_PATH	MODEM_WR_PATH	VBI_WR_PATH	ABI_WR_PATH
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W				R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	0				0	0	0	0	0	0

WR_PATH { PMIC_WR_PATH, MODEM_WR_PATH, VBI_WR_PATH, ABI_WR_PATH } The bit is to facilitate ACD members for verifying purpose; the hardware supports write path switching, without being disturbed by existing MCU load. However, when with manually control, all registers addresses are offset by 0x1000. For example, MCU configures **ACIF_AUDIO_CON0** through the address 0x8301_0200, while the manually control path take effect when configuring 0x8301_1200. Notice that before finishing manual control, the register must be reset to be 0. The modem part includes BBRX, BBTX, APC and AUX.

- **0** switch the register setting to MCU side.
- **1** switch the register setting to manually control by TRACE32 through JTAG.

ACD_MODE The register bit decides the input/output path of the mixed-mode module. For ABI and VBI, it can be configured to feed the pattern from AFE or from GPIO (shared with A_FUNC_MODE). For BBTX, APC and AUX, the input selection interface is divided at either MIXED_DIG or GPIO (also shared with A_FUNC_MODE). As for the BBRX, the output pattern can be bypass to CHIPIO with this register bit being true. The bit is for convenient debug-usage in normal mode, such that the data pattern can be observed or be feed-in by external device, while control register setting still comes from the chip internally(By use of JTAG). It should be notice that

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this special debug mode should be accompanied by proper setting of GPIO, which decides the PAD OE when in normal function.

0 data pattern comes from chip internally, and the output data cannot be bypassed to GPIO.

1 analog debug mode in normal function.

VTX2AU_SEL The register bit select the input source to AUDIO DAC.

0 normal path

1 loop-back path (select VOICE TX-ADC data)

ABIST_MODE The register bit control the GPIO as mixedsys monitor pins, shared with ABIST_MODE.

0 disbale

1 enable

AUX_PWDB The register bit control the power-down of AUX at A_FUNC_MODE or ACD_MODE=1

0 power-down

1 power-up

APC_PWDB The register bit control the power-down of APC at A_FUNC_MODE or ACD_MODE=1

0 power-down

1 power-up

BTX_PWDB The register bit control the power-down of BBTX at A_FUNC_MODE or ACD_MODE=1

0 power-down

1 power-up

ESDM_PWDB The register bit control the power-down of BBRX at A_FUNC_MODE or ACD_MODE=1

0 power-down

1 power-up

ASDM_PWDB The register bit control the power-down of ASDM at A_FUNC_MODE or ACD_MODE=1

0 power-down

1 power-up

VSDM_PWDB The register bit control the power-down of VSDM at A_FUNC_MODE or ACD_MODE=1

0 power-down

1 power-up

Note: A_FUNC_CK & A_FUNC_DIN[11:0] description table:

	VSDM	ASDM	BBRX	BBTX	APC	AUX	SIM
A_FUNC_CK (JTCK)	VSDM_CK	ASDM_CK	ESDM_CK	GTX_SCLK	APC_TG	AUX_SCLK	
A_FUNC[0] (KROW0)	VRXSIN	AYDL[0] / AYDR[0]		GTX_DDI[0] / GTX_DDQ[0]	APC_BUS[0]	AUX_SEL[0]	SIMCLK
A_FUNC[1] (KROW1)	VRXZIN	AYDL[1] / AYDR[1]		GTX_DDI[1] / GTX_DDQ[1]	APC_BUS[1]	AUX_SEL[1]	SIMRST
A_FUNC[2] (KROW2)	VRXPH1_6P5M_CK	AYDL[2] / AYDR[2]		GTX_DDI[2] / GTX_DDQ[2]	APC_BUS[2]	AUX_SEL[2]	SIMDATA_OE
A_FUNC[3]	VRXPH2_6P	AYDL[3] /		GTX_DDI[3] /	APC_BUS[3]	AUX_SEL[3]	SIMDATA_O

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	VSDM	ASDM	BBRX	BBTX	APC	AUX	SIM
(KROW3)	5M_CK	AYDR[3]		GTX_DDQ[3]			UT
A_FUNC[4] (KROW4)		AYDL[4] / AYDR[4]		GTX_DDI[4] / GTX_DDQ[4]	APC_BUS[4]	AUX_ST	SIM2CLK
A_FUNC[5] (KCOL0)		AYDL[5] / AYDR[5]		GTX_DDI[5] / GTX_DDQ[5]	APC_BUS[5]	AUX_CS_B	SIM2RST
A_FUNC[6] (KCOL1)		AYDL[6] / AYDR[6]		GTX_DDI[6] / GTX_DDQ[6]	APC_BUS[6]	AUX_DIN	SIM2DATA_OE
A_FUNC[7] (KCOL2)		AYDL[7] / AYDR[7]		GTX_DDI[7] / GTX_DDQ[7]	APC_BUS[7]	AUX_TPD_LATCH	SIM2DATA_OUT
A_FUNC[8] (KCOL3)		AYDL[8] / AYDR[8]		GTX_DDI[8] / GTX_DDQ[8]	APC_BUS[8]		
A_FUNC[9] (KCOL4)				GTX_DDI[9] / GTX_DDQ[9]	APC_BUS[9]		
A_FUNC[10] (PWM)				SWITCH_INPUT			
A_FUNC[11] (SECU_EN)	CLK26M_CK	CLK26M_CK	CLK26M_CK	CLK26M_CK	CLK26M_CK	CLK26M_CK	CLK26M_CK

12.2.2 BBRX

MCU APB bus registers for BBRX ADC are listed as followings.

0x8301_0300 BBRX Control Register ACIF_BBRX_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DITHDIS	QSEL		ISEL			GAIN		CALBIAS				
Type				R/W	R/W		R/W			R/W		R/W				
Reset				0	00		00			00		00000				

Set this register for BBRX analog circuit configuration controls.

CALBIAS The register field is for control of biasing current in BBRX mixed-signal module. Biasing current in BBRX mixed-signal module has impact on the performance of A/D conversion. The larger the value of the register field, the larger the biasing current in BBRX mixed-signal module, and the larger the SNR.

x0100 8/4x
x0011 7/4x
x0010 6/4x
x0001 5/4x
xx000 4/4x
x1001 4/5x
x1010 4/6x

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x1011 4/7x
x1100 4/8x

GAIN The register bits are for configuration of gain control of analog inputs in GSM RX mixed-signal module.
00 Input range is 0.80X AVDD for analog inputs in GSM RX mixed-signal module.
01 Input range is 0.40X AVDD for analog inputs in GSM RX mixed-signal module.
10 Input range is 0.57X AVDD for analog inputs in GSM RX mixed-signal module.
11 Input range is 0.33X AVDD for analog inputs in GSM RX mixed-signal module.

ISEL Loopback configuration selection for I-channel in BBRX mixed-signal module.
00 Normal mode
01 Loopback TX analog I
10 Loopback TX analog Q
11 Select the grounded input

QSEL Loopback configuration selection for Q-channel in BBRX mixed-signal module.
00 Normal mode
01 Loopback TX analog Q
10 Loopback TX analog I
11 Select the grounded input

DITHDIS Dither feature disable control register, which can effectively reduce the THD (total harmonic distortion) of the BBRX ADC.
0 enable (default value)
1 disable

12.2.3 BBTX

MCU APB bus registers for BBTX DAC are listed as followings.

0x8301_0400 BBTX Control Register 0 ACIF_BBTX_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CALRCDONE	STARTCALRC	GAIN			CALRCSEL			TRIMI				TRIMQ			
Type	R	R/W	R/W			R/W			R/W				R/W			
Reset	0	0	000			000			0000				0000			

Set this register for BBTX analog circuit configuration controls.

The procedure to perform calibration processing for smoothing filter in BBTX mixed-signal module is as follows:

1. Write 1 to the register bit STARTCALRC. Start calibration process.
2. Read the register bit CALRCDONE. If read as 1, then calibration process is finished. Otherwise repeat the step.
3. Write 0 to the register bit STARTCALRC. Stop calibration process.

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4. The result of calibration process can be read from the register field CALRCOUT in the register ACIF_BBTX_CON1. Software can set the value to the register field CALRCSEL for 3-dB cutoff frequency selection of smoothing filter in DAC of BBTX.

***Remember to set the register field CALRCCNT in the register ACIF_BBTX_CON1 to 0x0b before the calibration process. It only needs to be set once.

TRIMQ The register field is used to control gain trimming of Q-channel DAC in BBTX mixed-signal module.

0111 +0.84dB
0110 +0.72dB
....
0010 +0.24dB
0001 +0.12dB
0000 +0.00dB
1111 -0.12dB
1110 -0.24dB
....
1001 -0.84dB
1000 -0.96dB

TRIMI The register field is used to control gain trimming of I-channel DAC in BBTX mixed-signal module.

0111 +0.84dB
0110 +0.72dB
....
0010 +0.24dB
0001 +0.12dB
0000 +0.00dB
1111 -0.12dB
1110 -0.24dB
....
1001 -0.84dB
1000 -0.96dB

CALRCSEL The register field is for selection of cutoff frequency of smoothing filter in BBTX mixed-signal module.

011 0.71*Fc
010 0.80*Fc
001 0.91*Fc
000 1.00*Fc
111 1.14*Fc
110 1.25*Fc
101 1.34*Fc
100 1.43*Fc

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GAIN The register field is used to control gain of DAC in BBTX mixed-signal module. It has impact on both of I- and Q-channel DAC in BBTX mixed-signal module.

011 +2.0dB
010 +1.3dB
001 +0.6dB
000 +0.0dB
111 -0.6dB
110 -1.3dB
101 -2.0dB
100 -2.6dB

STARTCALRC Whenever 1 is writing to the bit, calibration process for smoothing filter in BBTX mixed-signal module will be triggered. Once the calibration process is completed, the register bit CARLDONE will be read as 1.

CALRCDONE The register bit indicates if calibration process for smoothing filter in BBTX mixed-signal module has finished. When calibration process is finished, this register bit would be 1. When the register bit STARTCALRC is set to 0, this register bit becomes 0 again.

0x8301_0404 BBTX Control Register 1 ACIF_BBTX_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CALRCOUT			FLOAT	CALRCCNT					CALBIAS				CMV		
Type	R			R/W	R/W					R./W				R/W		
Reset	0			0	00000					0000				000		

Set this register for BBTX analog circuit configuration controls.

CMV The register field is used to control common voltage in BBTX mixed-signal module. It is coded in 2's complement, that is, with maximum 3 and minimum –4.

011 0.62*VDDA
010 0.58*VDDA
001 0.54*VDDA
000 0.5*VDDA
111 0.46*VDDA
110 0.42*VDDA
101 0.38*VDDA
100 0.34*VDDA

CALBIAS The register field is for control of biasing current in BBTX mixed-signal module. Biasing current in BBTX mixed-signal module has impact on performance of D/A conversion. Larger the value of the register field, the larger the biasing current in BBTX mixed-signal module.

0100 8/4x
0011 7/4x
0010 6/4x

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0001 5/4x
0000 4/4x
1001 4/5x
1010 4/6x
1011 4/7x
1100 4/8x

CALRCCNT This parameter is for calibration process of smoothing filter in BBTX mixed-signal module. Note that it is NOT coded in 2's complement. Therefore the range of its value is from 0 to 31. Remember to set it to 0x16 before BBTX calibration process if clock sent to BBTX is 26Mhz. Otherwise, set to 0x0b if clock is 13Mhz.
****It only needs to be set once. In MT6251/53, only 26MHz clock is available.

FLOAT The register field is used to set the outputs of DAC in BBTX mixed-signal module float or not.

CALRCOUT After calibration processing for smoothing filter in BBTX mixed-signal module, a set of 3-bit value is obtained. It is coded in 2's complement.

0x8301_0408 BBTX Control Register 2 ACIF_BBTX_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DCCOARSEQ		DCCOARSEI		DAC_PTR				DWAEN	COARSE		CALRCAUTO	CALRCOPEN
Type				R/W		R/W		R/W				R/W	R/W		R/W	R/W
Reset				00		00		0000				0	0		0	0

Set this register for BBTX analog circuit configuration controls.

CALRCOPEN The register field is used to control normal mode(close loop) or debug mode (open loop) for BBTX comparator in mixed signal
0 normal mode (close loop)
1 debug mode (open loop)

CALRCAUTO The register field is used to control the result of calibration process of smoothing filter can automatically load to control the smoothing filter or not.
0 manual load mode (default)
1 auto load mode

COARSE The register field is used to control the central nominal value of BBTX DAC output.
00 central nominal at 1.0V
01 central nominal at 0.8V
10 reserved
11 central nominal at 1.2V

DWAEN The register field is used to turn on the DWA scheme of the BBTX DAC.
0 DWA scheme off (default).
1 DWA scheme on.

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DACPTR The register field is used to configured the staring pointer of one-hot pulling of LSB[7:0] signal to BBTX DAC, range from 0~15. There are two different configuration types. For DWAEN=0, pointer always starts from the configuration value (e.g. if DACPTR = 4'b1, one-hot will start pulling from LSB[1]). However, for DWAEN=1, the initial starting pointer will follow the configuration, while the pointer will move to most significant one-hot pointer + 1 from the last LSB[7:0] input. (e.g. if DACPTR = 4'b1,and LSB[7:0] maybe 8'b00001110, then the next starting poiter will starts from LSB[4].). Default value is 0x00.

DCCOARSEI The register field is used to control the central nominal value of BBTX DAC for I channel offset

- **00** central nominal at +0mV
- **01** central nominal at +30mV
- **10** reserved
- **11** central nominal at -30mV

DCCOARSEQ The register field is used to control the central nominal value of BBTX DAC for Q channel offset

- **00** central nominal at +0mV
- **01** central nominal at +30mV
- **10** reserved
- **11** central nominal at -30mV

1.1.1.APC DAC

MCU APB bus registers for APC DAC are listed as followings.

0x8301_0600 APC Control Register ACIF_APC_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										TGSEL	TEST		CALI			
Type										R/W	R/W		R/W			
Reset										0	0		0000			

Set this register for APC analog circuit configuration controls.

****Please refer to analog functional specification for more details.

TGSEL APC_TG trigger edge select.

- **0** Trigger the signal at rising edge.
- **1** Trigger the signal at falling edge.

TEST Bypass output buffer.

- **0** Buffer bypass mode disable.
- **1** Buffer bypass mode enable.

CALI APC DAC biasing current control.

- **0100** 8/4×
- **0011** 7/4×
- **0010** 6/4×
- **0001** 5/4×
- **0000** 4/4×

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1001 4/5×
1010 4/6×
1011 4/7×
1100 4/8×

12.2.4 Auxiliary ADC

MCU APB bus registers for AUX ADC are listed as followings.

0x8301_0700 AUX Control Register 0 ACIF_AUX_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ABIST_RSV									ENB					CALI	
Type	RW									R/W					R/W	
Reset	00000000									0					00	

Set this register for AUX analog circuit configuration controls.

****Please refer to analog functional specification for more details.

CALI AUX ADC biasing current control
- **00** 0.5x
- **01** 1.0x
- **10** 1.5x
- **11** 2.0x

ENB Comparator switch enable signal.
- **0** Enable
- **1** Disable

RG_ABIST_RSV ABIST switch control
- **[0]** Enable APC to AUX_VIN_YM switch (1: enable; 0: disable)
- **[1]** Enable APC to AUX_VIN_YP switch (1: enable; 0: disable)
- **[2]** Enable APC to AUX_VIN_XP switch (1: enable; 0: disable)
- **[3]** Reserved
- **[4]** Reserved
- **[5]** Reserved
- **[6]** Enable ABI to VBITX switch (1: enable; 0: disable)
- **[7]** Enable VBIRX to VBITX switch (1: enable; 0: disable)

0x8301_0704 AUX Control Register 1 ACIF_AUX_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name				RG_ABIST_S2D_PWDB	RG_ABIST_S2D_GAIN	RG_ABIST_SWEN
Type				RW	RW	R/W
Reset				0	00	0000000000

Set this register for AUX analog circuit configuration controls.

****Please refer to analog functional specification for more details.

RG_ABIST_S2D_PWDB ABIST S2D buffer power down control

- **0** power down
- **1** power up

RG_ABIST_S2D_GAIN ABIST S2D buffer gain control

- **00** 1.0X
- **01** 0.9X
- **10** 0.8X
- **11** 0.7X

RG_ABIST_SWEN ABIST switch enable control

- **[0]** Enable Audio R-ch to S2D switch (1: enable; 0: disable)
- **[1]** Enable Audio L-ch to S2D switch (1: enable; 0: disable)
- **[2]** Enable APC to S2D switch (1: enable; 0: disable)
- **[3]** Enable APC to FM input switch (1: enable; 0: disable)
- **[4]** Enable differential 26MHz clock to AUX_IN1/IN2 switch (1: enable; 0: disable)
- **[5]** Enable APC to AUX_IN0/IN1/IN2 switch (1: enable; 0: disable)
- **[6]** Enable APC to AUX_VIN_VBOUT switch (1: enable; 0: disable)
- **[7]** Enable APC to AUX_ VIN_ISENSE switch (1: enable; 0: disable)
- **[8]** Enable APC to AUX_ VIN_CHRIN_RATIO switch (1: enable; 0: disable)
- **[9]** Enable AUX PLL test mode control (1: enable; 0: disable)

12.2.5 Voice Front-end

MCU APB bus registers for speech are listed as followings.

0x8301_0100 Voice Control Register 0 ACIF_VOICE_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VBIRX_SCRAMEN	VABI_SEL	VUPG						VDPG0				VZERO_DTC_CMP_PWD	VZERO_DTC_EN	VZERO_DTC_CALI	VZERO_DTC_CMP_PWD
Type	R/W	R/W	R/W						R/W				R/W	R/W	R/W	R/W
Reset	0	0	000000						0000				0	0	00	0

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Set this register for VOICE PGA gains analog circuit. VUPG is set for microphone input volume control. And VDPG0 is set for output volume control.

VBIRX_SCRAMEN [Description for this register field]

- **0** [Description for field value 0]
- **1** [Description for field value 1]

VABI_SEL Select Voice signal from VBIDAC or ABIDAC

- **0** select VBIDAC (default)
- **1** select ABIDAC

VDPG0 Voice-band down-link PGA gain control bits.

VDPG0 [3:0]	Gain
1111	8dB
1110	6dB
1101	4dB
1100	2dB
1011	0dB
1010	-2dB
1001	-4dB
1000	-6dB
0111	-8dB
0110	-10dB
0101	-12dB
0100	-14dB
0011	-16dB
0010	-18dB
0001	-20dB
0000	-22dB

VUPG Voice-band up-link PGA gain control bits. For VCFG[3] = 1, it is only valid for INPUT 1.

VUPG [5:0]	Gain
111111	43 dB
111110	42 dB
111101	41 dB
111100	40 dB
111011	39 dB
111010	38 dB
111001	37 dB

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111000	36 dB
110111	35 dB
110110	34 dB
110101	33 dB
110100	32 dB
110011	31dB
110010	30 dB
110001	29 dB
110000	28 dB
101111	27 dB
101110	26 dB
101101	25 dB
101100	24 dB
1101011	23 dB
101010	22 dB
101001	21 dB
101000	20 dB
100111	19 dB
100110	18 dB
100101	17 dB
100100	16 dB
100011	15 dB
100010	14 dB
100001	13 dB
100000	12 dB
011111	11 dB
011110	10 dB
011101	9 dB
011100	8 dB
011011	7 dB
011010	6 dB
011001	5 dB
011000	4 dB
010111	3 dB
010110	2 dB

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010101	1 dB
010100	0 dB
010011	-1dB
010010	-2 dB
010001	-3 dB
010000	-4 dB
001111	-5 dB
001110	-6 dB
001101	-7 dB
001100	-8 dB
0101011	-9 dB
001010	-10 dB
001001	-11 dB
001000	-12 dB
000111	-13 dB
000110	-14 dB
000101	-15 dB
000100	-16 dB
000011	-17 dB
000010	-18 dB
000001	-19 dB
000000	-20 dB

VZERO_DTC_CMP_PWD [Description for this register field]

0 [Description for field value 0]

1 [Description for field value 1]

VZERO_DTC_EN [Description for this register field]

0 [Description for field value 0]

1 [Description for field value 1]

VZERO_DTC_CALI [Description for this register field]

0 [Description for field value 0]

1 [Description for field value 1]

0x8301_0104 Voice Control Register 1 ACIF_VOICE_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			VMIC_VREF				VCFG			VDSEND				VCALI		
Type			R/W				RW			R/W				R/W		
Reset			00				00000			00				00000		

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Set this register for VOICE analog circuit configuration controls.

VCALI The registers field is biasing current control in 2's complement format. Set VBI bias current ratio VCALI[4:3] are used to calibrate op_extigen current bias, 00 represents nominal 1.75uA current bias.

VDSEND The register field is set single-ended DACBUF output.

- **0** Differential output.
- **1** Single-ended output.

VCFG Set PGA's input selection, AC/DC coupled and GAIN/ATT mode & Set micbias single-ended configuration, active high

- **[1:0]** Input select control
  - **00** input 0
  - **01** input 1
  - **10** FM
  - **11** reserved
- **[2]** Test mode coupling control
  - **0** AC coupling;
  - **1** DC coupling
- **[3]** Gain mode control. This control register is only valid to input 1. Others can be amplification mode only.
  - **0** amplification;
  - **1** bypass VBITX PGA to test ADC only
- **[4]** Reserved

VMIC_VREF Tuning MICBIASP DC voltage.

- **00** 1.9V
- **01** 2.0V
- **10** 2.1V
- **11** 2.2V

0x8301_0108 Voice Control Register 2 ACIF_VOICE_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VUPOP_EN	VBIAS_EN		VOC_EN				VIBOOT	VFLOAT	VRSDON	VGBOOT	VADC_DVREF_CAL	VADC_DENB	VDIFF_BIAS	VADCINMODE	VDACINMODE
Type	R/W	R/W		R/W				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0		0				0	0	0	0	0	0	0	0	0

Set this register for VOICE analog circuit configuration controls. There are several loop back modes and test modes implemented for test purposes. Suggested value is 0280h.

VDACINMODE The register bit control the Voice DAC input mode.

- **0** normal mode
- **1** loop-back mode, the DAC input from the ADC output

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VADCINMODE The register bit control the Voice ADC output mode.

- **0** normal mode
- **1** loop-back mode, the ADC input from the DAC output

VDIFF_BIAS Enable the reference for VBI_BIAS block (Single end (1.4V).

- **0** Enable
- **1** Disable.

VADC_DENB ADC dither enable. VBI uplink ADC has a sub-block: dither generator. It is used to eliminate the idle tone.

- **0** Enable
- **1** Disable

VADC_DVREF_CAL ADC dither reference voltage calibration. VBI uplink ADC has a sub-block: dither generator. It needs a reference voltage to work correctly. The reference can be adjusted.

- **0** +/-0.56V
- **1** +/- 0.373V

VGBOOT VBI DAC Gain tuning

- **0** 2X gain
- **1** 1X gain

VRSDON Voice-band redundant signed digit function on.

- **0** 1-bit 2-level mode
- **1** 2-bit 3-level mode

VFLOAT VBI DACBUF output float during power-down mode.

- **0** normal
- **1** floating

VIBOOT VBI DACBUF bias current control.

- **0** 1X bias current
- **1** 2X bias current

VOC_EN VBI DACBUF over current protection.

- **0** disable
- **1** enable

VBIAS_EN VBI DACBUF bias current control.

- **00** 1.0x (default)
- **01** 1.33x
- **10** 0.33x
- **11** 0.67x

VUPOP_EN Anti pop-noise for buffer output enable.

- **0** disable
- **1** enable

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0x8301_010C Voice Control Register 3 ACIF_VOICE_CON3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											VBIAS_PWDB	VLNA_PWDB	VADC_PWDB	VDAC_PWDB		VOUT0_PWDB
Type											R/W	R/W	R/W	R/W		R/W
Reset											0	0	0	0		0

Set this register to power up VOICE analog blocks.

**** 0: power down, 1: power up.

VOUT0_PWDB OUT0 buffer block power-down control bit.

- **0** power-down
- **1** power-up

VDAC_PWDB Voice DAC block power-down control bit.

- **0** power-down
- **1** power-up

VADC_PWDB Voice ADC block power-down control bit.

- **0** power-down
- **1** power-up

VLNA_PWDB Voice low noise amplifier block power-down control bit.

- **0** power-down
- **1** power-up

VBIAS_PWDB Voice bias block power-down control bit.

- **0** power-down
- **1** power-up

12.2.6 Audio Front-end

MCU APB bus registers for audio are listed as followings.

0x8301_0200 Audio Control Register 0 ACIF_AUDIO_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VOICE2ABI						AMUTER	AMUTEL	APGR				APGL			
Type	R/W						R/W	R/W	R/W				R/W			
Reset	0						0	0	0000				0000			

Set this register for AUDIO PGA gains control analog circuit.

APGL AUDIO PGA L-channel gain control.

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APGR AUDIO PGA R-channel gain control.

APGR [3:0] / APGL [3:0]	Gain
1111	23dB
1110	20dB
1101	17dB
1100	14dB
1011	13dB
1010	8dB
1001	5dB
1000	2dB
0111	-1dB
0110	-4dB
0101	-7dB
0100	-10dB
0011	-13dB
0010	-16dB
0001	-19dB
0000	-22dB

AMUTEL AUDIO L-channel mute control.

- **0** normal
- **1** mute L-channel

AMUTER AUDIO R-channel mute control.

- **0** normal
- **1** mute R-channel

VOICE2ABI To control reference voltage of DAC, in which reference comes from

*** (ABI DAC apply original Vref, AVDD<->AVSS, when set VOICE2ABI = 1: ==> ABI DAC apply VBI Vref, 1.9V<=>0.7V).

- **0** Power 2.8V and ground 0V.
- **1** Reference buffer 2.6V and 0.2V.

0x8301_0204 Audio Control Register 1 ACIF_AUDIO_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			APRO_SC	ADEPOP		ABUFSELR			ABUFSELL			ACALI				
Type			R/W	R/W		R/W			R/W			R/W				
Reset			0	1		000			000			00000				

Set this register for AUDIO analog circuit configuration controls.

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ACALI Audio bias current control, in 2's complement format.

ABUFSELL Audio buffer L-channel input selection.

- **00X** audio DAC L-channel output
- **010** voice DAC output
- **100** external FM R/L-channel radio output, stereo to mono
- **101** external FM L-channel radio output
- **others** reserved

ABUFSELR Audio buffer R-channel input selection.

- **00X** audio DAC R-channel output
- **010** voice DAC output
- **100** external FM R/L-channel radio output, stereo to mono
- **101** external FM R-channel radio output
- **others** reserved

ADEPOP Audio de-pop noise control bit

- **0** disable
- **1** enable

APRO_SC Short circuit protection control bit.

- **0** disable
- **1** enable

0x8301_0208 Audio Control Register 2 ACIF_AUDIO_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												ABIAS_PWDB	ADACR_PWDB	ADACL_PWDB	AOUTR_PWDB	AOUTL_PWDB
Type												R/W	R/W	R/W	R/W	R/W
Reset												0	0	0	0	0

Set this register for AUDIO analog circuit configuration controls.

**** 0: power down, 1: power up. Suggested value is 00ffh.

AOUTL_PWDB Power-down AUDIO L-channel output buffer.

- **0** power-down
- **1** power-up

AOUTR_PWDB Power-down AUDIO R-channel output buffer.

- **0** power-down
- **1** power-up

ADACL_PWDB Power-down AUDIO L-channel DAC.

- **0** power-down
- **1** power-up

ADACR_PWDB Power-down AUDIO R-channel DAC.

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0 power-down
1 power-up

ABIAS_PWDB Power-down AUDIO bias current circuit.

0 power-down
1 power-up

0x8301_020C Audio Control Register 3 ACIF_AUDIO_CON3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						ABUF_INSHORT		AHFMODE	ABUF_BIAS			AMUX			AVCM_MODE	
Type						R/W		R/W	R/W			R/W			R/W	
Reset						0		0	00			00			0	

Set this register for AUDIO analog circuit configuration controls.

AVCOM_MODE Change common mode generation circuitry.

0 select new VCM circuitry
1 select old VCM circuitry

AMUX Mux audio DAC output to DM R/L pins.

00 FM input
01 FM input
10 L-channel DAC
11 R-channel O/P

ABUF_BIAS Audio buffer quasi-current select bits.

00 1.0x (default)
01 1.33x
10 0.33x
11 0.67x

AHFMODE Audio hand-free mode enable bit.

0 normal mode
1 hand-free mode

ABUF_INSHORT Audio buffer input short enable (during voice mode)

0 disable
1 enable

12.2.7 Power Management Control

Power management unit, so called PMU, is integrated into analog part. To facilitate software control and interface design, PMU control share the CCI interface along with other analog parts, such as BBTX, BBRX, VBI and ABI.

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12.2.7.1 Low Dropout Regulators (LDOs), Buck converterand Reference

The PMU Integrates 12 LDOs that are optimized for their given functions by balancing quiescent current, dropout voltage, line/load regulation, ripple rejection, and output noise.

RF LDO (Vrf)

The RF LDO is a linear regulator that could source 200mA (max) with 2.8V output voltage. It supplies the RF circuitry of the handset. The LDO is optimized for high performance and adequate quiescent current.

Digital Core Buck Converter (Vcore)

The digital core regulator is a DC-DC step-down converter (Buck converter) that could source 200mA (max) with 1.2V to 0.9V programmable output voltage based on software register setting. It supplies the power for baseband circuitry of the SoC. The buck converter is optimized for high efficiency and low quiescent current.

Analog Boost Converter (VBOOST1)

The analog boost1 regulator is a DC-DC step-up converter (Boost converter) that could source 150mA (max) with VBAT to 5.45V programmable output voltage based on software register setting. It supplies the power for 4x parallel scheme backlight LEDs. The boost converter is optimized for high efficiency and low quiescent current, low output ripple.

Digital IO LDO (Vio)

The digital IO LDO is a linear regulator that could source 100mA (max) with 2.8V output voltage. It supplies the the power for baseband circuitry of the SoC. The LDO is optimized for very low quiescent current and turns on automatically together with Vm/Va LDOs.

Analog LDO (Va)

The analog LDO is a linear regulator that could source 125mA (max) with 2.8V output voltage. It supplies the analog sections of the SoC. The LDO is optimized for low frequency ripple rejection in order to reject the ripple coming from the burst at 217Hz of RF power amplifier.

TCXO LDO (Vtcxo)

The TCXO LDO is a linear regulator that could source 20mA (max) with 2.8V output voltage. It supplies the temperature compensated crystal oscillator, which needs ultra low noise supply with very good ripple rejection.

Single-Step RTC LDO (Vrtc)

The single-step RTC LDO is a linear regulator that can charge up a capacitor-type backup coin cell to 2.6V, which also supplies the RTC module even at the absence of the main battery. The single-step LDO features the reverse current protection and is optimized for ultra low quiescent current while sustaining the RTC function as long as possible.

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Memory LDO (Vm)

The memory LDO is a linear regulator that could source 200mA (max) with 1.8V or 2.8V output voltage selection based on the supply specification of memory chips. It supplies the memory circuitry in the handset. The LDO is optimized for very low quiescent current with wide output loading range.

SIM LDO (Vsim)

The SIM LDO is a linear regulator that could source 80mA (max) with 1.8V or 3.0V output voltage selection based on the supply specs of subscriber identity modules (SIM) card. It supplies the SIM card and SIM level shifter circuitry in the handset. The Vsim LDO is controlled independently by the register named VSIM_EN.

SIM2 LDO (Vsim2)

The SIM2 LDO is a linear regulator that could source 20mA (max) with 1.8V or 3.0V output voltage selection based on the supply specs of the 2nd subscriber identity modules (SIM) card. It supplies the 2nd SIM card and SIM level shifter circuitry in the handset. The Vsim2 LDO is controlled independently by the register named VSIM2_EN.

USB LDO (Vusb)

The USB LDO is a linear regulator that could source 100mA (max) with 3.3V output dedicated for USB circuitry. It is controlled independently by the register named RG_VUSB_EN.

Memory Card / Bluetooth LDO (Vbt)

~~The VBT LDO is a linear regulator that could source 100mA (max) with 2.8V or 3.0V output for memory card or Bluetooth module. It is controlled independently by the register named RG_VBT_EN. We do this change per SA's request. 20090622.~~

The VBT LDO is a linear regulator that could source 100mA (max) with 3.0V output for memory card or Bluetooth module. It is controlled independently by the register named RG_VIBR_EN. Note: Please set RG_VIBR_SEL[1:0] to HH together with RG_VIBR_EN and the corresponding PWM to 100% duty.

Camera Analog LDO (Vcama)

The Vcama LDO is a linear regulator that could source 150mA (max) with 1.5V, 1.8V, 2.5V or 2.8V output which is selected by the register named VCAMA_SEL[1:0]. It supplies the analog power of the camera module. Vcama is controlled independently by the register named RG_VCAMA_EN.

Camera Digital LDO (Vcamd)

The Vcamd LDO is a linear regulator that could source 75mA (max) with 1.3V, 1.5V, 1.8V or 2.8V output which is selected by the register named VCAMD_SEL[1:0]. It supplies the digital power of the camera module. Vcamd is controlled independently by the register named RG_VCAMD_EN.

12.2.7.2 SIM Card Interface

There are two SIM card interface modules to support two SIM cards simultaneously. The SIM card interface circuitry of PMU meets all ETSI and IMT-2000 SIM interface requirements. It provides level shifting needs for low voltage GSM

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controller to communicate with either 1.8V or 3V SIM cards. All SIM cards contain a clock input, a reset input, and a bi-directional data input/output. The clock and reset inputs to SIM cards are level shifted from the supply of digital IO (Vio) of baseband to the SIM supply (Vsim). The bi-directional data bus is internal pull high to Vsim via 10KΩ resistor.

The 2nd SIM card interface can be used for supporting another SIM card or mobile TV. The interface pins such as SIO2, SRST2, SCLK2, can be configured as GPIO when there is no need to use the 2nd SIM card interface.

All pins that connect to the SIM card (Vsim, SRST, SCLK, SIO) withstand over 5kV HBM (human body mode) ESD. In order to ensure proper ESD protection, careful board layout is required.

12.2.7.3 Class-D high efficiency speaker driver

The embedded high efficiency Class-D speaker driver is targeted to drive 8Ω speaker. The output power can be up to 800mW from 4.2V battery. This driver is optimized for high efficiency and low SNDR.

This SPK (speaker) driver in MT6253 also equipped the Class-AB mode for specifically low noise applications (models). Though we can switch the Speaker driver back and forth between Class-AB and Class-D mode by register settings, we strongly suggest fixing the mode for dedicate application (model).

12.2.7.4 Vibrator and Keypad LED Switches

One built-in open-drain output switch drives the Keypad LED in the handset. This switch is controlled by baseband with enable registers. The switch of keypad LED can sink 150mA. The open-drain output switches are high impedance when disabled.

~~We use an LDO to drive the vibrator load sourcing current up to 250mA. The output voltages are 1.3V, 1.8V, 2.5V or 3.0V ,which are selected by the register named RG_VIBR_SEL[1:0]. We do this change per SA's request. 20090622.~~

We use an LDO to drive the vibrator load sourcing current up to 100mA. It is controlled independently by the register named RG_VBT_EN. The output voltages are 2.8V or 3.0V, which are selected by the register named RG_VBT_SEL.

12.2.7.5 Power-on Sequence and Protection Logic

The PMU handles the powering ON and OFF of the handset. There are three ways to power-on the handset system :

1. Push PWRKEY (Pull the PWRKEY pin to the low level)

Pulling PWRKEY low is the typical way to turn on the handset. The Vcore buck converter will be turned-on first, and then Va/Vio/Vm LDOs turn-on at the same time. The supplies for the baseband are ready and then the system reset ends at the moment when the Vcore/Va/Vio/Vm are fully turned-on to ensure the correct timing and function. After that, baseband would send the PWRBB signal back to PMU for acknowledgement. To successfully power-on the handset, PWRKEY should be kept low until PMU receives the PWRBB from baseband.

2. RTC module generate PWRBB to wakeup the system

If the RTC module is scheduled to wakeup the handset at some time, the PWRBB signal will directly send to the PMU. In this case, PWRBB becomes high at the specific moment and let PMU power-on just like the sequence described above. This is the case named RTC alarm.

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3. Valid charger plug-in (CHRIN voltage is within the valid range)

Charger plugging-in will also turn on the handset if the charger is valid (no OVP take place). However, if the battery voltage is too low to power-on the handset (UVLO state), the system won't be turned-on by any of these three ways. In this case, charger will charge the battery first and the handset will be powered-on automatically as long as the battery voltage is high enough.

Phone State	CHRON	UVLO	PWRKEY && (~PWRBB)	Vrtc	Vcore, Vio, Vm, Va	Vtcxo, Vrf
No Battery or Vbat < 2.5V	X	H	X	Off	Off	Off
2.5V < Vbat < 3.2V	L	H	X	On	Off	Off
Pre-Charging	H	H	X	On	Off	Off
Charger-on (Vbat>3.2V)	H	L	X	On	On	On
Switched off	L	L	H	On	Off	Off
Stand-by	L	L	L	On	On	Off
Active	L	L	L	On	On	On

Table 86 States of mobile handset and regulator

Under-voltage Lockout (UVLO)

The UVLO state in the PMU prevents startup if the initial voltage of the main battery is below the 3.2V threshold. It ensures that the handset is powered-on with the battery in good condition. The UVLO function is performed by a hysteretic comparator which can ensure the smooth power-on sequence. In addition, when the battery voltage is getting lower and lower, it will enter UVLO state and the PMU will be turned-off by itself, except for Vrtc LDO, to prevent further discharging. Once the PMU enters UVLO state, it draws low quiescent current. The RTC LDO is still working until the DDLO disables it.

Deep Discharge Lockout (DDLO)

PMU will enter to the deep discharge lockout (DDLO) state when the battery voltage drops below 2.5V. In this state, the Vrtc LDO will be shutdown. Otherwise, it draws very low quiescent current to prevent further discharging or even damage to the cells.

Reset

The PMU contains a reset control circuit which takes effect at both power-up and power-down. The **RESETB** pin is held at low in the beginning of power-up and returns to high after the pre-determined delay time. The delay time is controlled by a large counter, which use clock from internal ring-oscillator. At power-off, **RESETB** pin will return to low immediately without any delay.

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Over-temperature Protection

If the die temperature of PMU exceeds 150°C, the PMU will automatically disable all the LDOs except the Vrtc. Once the over-temperature state is resolved, a new power on sequence is required to enable the LDOs.

Battery Charger

The battery charger is optimized for the Li-ion batteries. The typical charging procedure can be divided into three phases: pre-charging, constant current mode charging, and constant voltage mode charging. **Figure 109** shows the flow chart of the charging procedure. Most of the charger circuits are integrated in the PMU except for one PMOS, one diode and one accurate resistor for current sensing. Those components should be applied externally.

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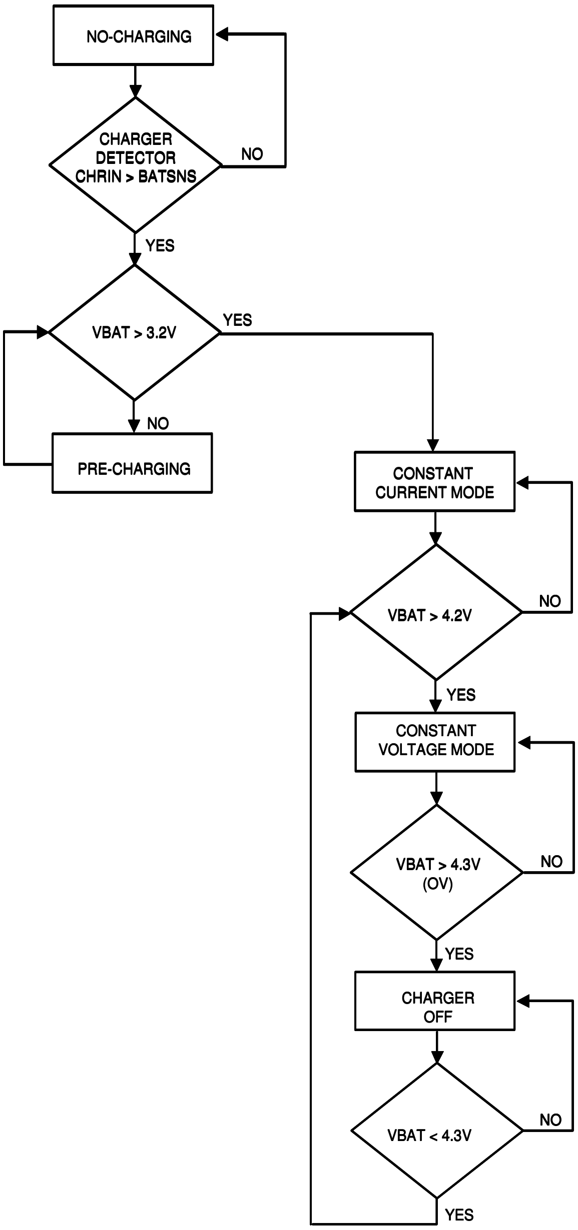

Figure 109 Battery Charger Flow Chart

1. Charge Detection

The PMU charger block has a detection circuit that senses the charger plug-in/out and provides the correct information to the baseband. If the CHRIN voltage is over 7V, the detection circuit reports invalid charger and CHRDET signal goes low to stop charging.

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2. Pre-Charging mode

When the battery voltage is below the UVLO threshold, the charging status is in the pre-charging mode. There are two steps in this mode. While the battery voltage is deeply discharged below 2V, a 10mA trickle current generated internally charges the battery. When the battery voltage exceeds 2V, the closed-loop pre-charge mode is enabled, which allows 10mV (typically) voltage drop across the external current sense resistor. The pre-charge current can be calculated:

$$I_{PRE_CHARGING} = \frac{V_{SENSE}}{R_{SENSE}} = \frac{10mV}{R_{SENSE}} \qquad (2)$$

3. Constant Current Charging Mode

Once the battery voltage has exceeded the UVLO threshold, the charger will switch to the constant current charging mode. It allows up to 800mA constant charging current which is controlled by the registers. The relation between the voltage drop across the external current sense resistor and the charging current is as follows,

$$I_{CONSTANT} = \frac{V_{SENSE}}{R_{SENSE}} \qquad (3)$$

Before the battery voltage reaches 4.2V, the charger will be in the constant current charging mode.

4. Constant Voltage Charging Mode

If the battery voltage has reached 4.2V, a constant voltage is applied to the battery and keeps it at 4.2V. As the charger is kept in the constant voltage charging mode, the charging current will be lower and lower until the charge completion. The charge termination is determined by the baseband, which will set the register RG_CHR_EN to stop the charger. Once the battery voltage exceeds 4.3V, a hardware over voltage protection (OV) should be activated and turn off the charger immediately.

12.2.7.6 External Components Selection

Input Capacitor Selection

For each of input pins (VBAT) of PMU, a local bypass capacitor is recommended. Use a 10µF, low ESR capacitor. MLCC capacitors provide the best combination of low ESR and small size. Using a 10µF Tantalum capacitor with a small (1µF or 2.2µF) ceramic in parallel is an alternative low cost solution.

For charger input pin (CHRIN), a bypass 1µF ceramic capacitor is recommended.

LDO/Buck converter Capacitor/inductor Selection

The analog and RF LDOs require a 4.7µF capacitor, the digital core buck converter requires a 2.2uF capacitor??, and the other LDOs require a 1µF capacitor. Large value capacitor may be used for desired noise or PSRR requirement. But the acceptable settling time should be taken into consideration. The MLCC X5R type capacitors must be used with VRF, VTCXO, VCAM_A and VA LDOs for good system performance. For other LDOs, MLCC X5R type capacitors are also recommended to use.

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Setting the Charge Current

PMU is capable of charging battery. The charging current is controlled with an external sense resistor, *Rsense*. It is calculated as the Eq.(3). If the charge current is pre-defined, Rsense can be determined.

Accurate sense resistors are available from the following vendors: Vishay Dale, IRC, Panasonic.

Charger FET Selection

The PMOS FET selection used in charger should consider the minimum drain-source breakdown voltage (BVDS), the minimum turn-on threshold voltage (VGS), and heat-dissipating ability.

These specifications can be calculated as below:

$V_{GS} = V_{CHRIN} - V_{GATEDRV}$

$V_{DS} = V_{CHRIN} - V_{DIODE} - V_{SENSE} - VBAT$

$$R_{DS(ON)} = \frac{V_{DS}}{I_{CHR}}$$

$P_{DISS} = (V_{CHRIN}-V_{DIODE}-V_{SENSE}-VBAT) \times I_{CHR}$

Appropriate PMOS FETs are available from the following vendors: Siliconix, IR, Fairchild.

Charger Diode Selection

The diode is used to prevent the battery from discharging through the PMOS's body diode into the charger's internal circuits. Choose a diode with sufficient current rating to handle the battery charging current and voltage rating greater than Vbat.

Layout Guideline

Use the general guidelines listed below to design the printed circuit boards:

1. Split battery connection to the VBAT, VBATRF and AVBAT pins for PMU. Place the input capacitor as close to the power pins as possible.
2. Va and Vtcxo capacitors should be returned to AGND. Vrf capacitor should be returned to AGND_RF.
3. Split the ground connection. Use separate traces or planes for the analog, digital, and power grounds (i.e. AGND, AGND_RF, DGND, PGND pins of PMU, respectively) and tie them together at a single point, preferably close to battery return.
4. Place a separate trace from the BATSNS pin to the battery input to prevent voltage drop error when sensing the battery voltage.
5. Kelvin-connect the charge current sense resistor by placing separate traces to the BATSNS and ISENSE pins. Make sure that the traces are terminated as close to the resistor's body as possible.

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6. Careful use of copper area, weight, and multi-layer construction will help to improve thermal performance.

12.2.7.7 Functional Specification

12.2.7.7.1 Electrical Characteristics

VBAT = 3 V ~ 5 V, minimum loads applied on all outputs, unless other noted. Typical values are at T_A = 25 °C.

Parameter	Conditions	Min.	Typical	Max.	Unit
Switch-Off Mode: Supply Current					
VBAT < 2.5 V	RTC LDO OFF		TBD		µA
2.5 V < VBAT < 3.3 V	VBAT=3.3V		TBD		µA
3.3 V < VBAT	VBAT=4.2V		TBD		µA
Operation: Supply Current					
All outputs on	VBAT=4.2V		TBD		µA
VSIM, VSIM2, VTXCO, VRF, VUSB, VCAM_A, VCAM_D, VBT off; all others on	VBAT=4.2V		TBD		µA
Under Voltage (UV)					
Under voltage falling threshold 1	UV_SEL[1:0] = 00	2.85	2.9	2.95	V
Under voltage falling threshold 2	UV_SEL[1:0] = 01	2.7	2.75	2.8	V
Under voltage falling threshold 3	UV_SEL[1:0] = 10	2.55	2.6	2.65	V
Under voltage falling threshold 4	UV_SEL[1:0] = 11	2.35	2.5	2.65	V
Under voltage rising threshold	UV_SEL[1:0] = xx	3.1	3.2	3.3	V
Reset Generator					
Output High		V_{IO}-0.5			V
Output Low				0.2	V
Output Current			TBD		mA
On Delay Time per Unit Capacitance		1.5	2.5	4	ms/nF
Power Key Input					
High Voltage		0.7*VBAT			V
Low Voltage				0.3*VBAT	V
Control Input Voltage					
Other Control Input High		2.0			V
Other Control Input Low				0.5	

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Thermal Shutdown					
Threshold			150		degree
Hysteresis			40		degree
LDO Enable Response Time			250		µs

12.2.7.7.2 Regulator Output

Parameter	Conditions	Min.	Typical	Max.	Unit
Digital Core Voltage					
Output voltage (V_D)	Register VOSEL=0	1.7	1.8	1.9	V
		~~1.4~~	~~1.5~~	~~1.6~~	V
	Register VO_SEL=1	1.1	1.2	1.3	V
Output current (Id_max)			200		mA
Line regulation				TBD	mV
Load regulation				TBD	mV
Digital IO Voltage					
Output voltage (V_IO)		2.7	2.8	2.9	V
Output current (Iio_max)			100		mA
Line regulation				TBD	mV
Load regulation				TBD	mV
RF Voltage					
Output voltage (V_RF)		2.7	2.8	2.9	V
Output current (Ia_max)			200		mA
Line regulation				TBD	mV
Load regulation				TBD	mV
Output noise voltage	f = 1k Hz to 100 kHz		40		uVrms
Ripple rejection	at 1kHz		65		dB
Analog Voltage					
Output voltage (V_A)		2.7	2.8	2.9	V
Output current (Ia_max)			125		mA
Line regulation				TBD	mV
Load regulation				TBD	mV
Output noise voltage	f = 10 Hz to 100 kHz		50		uVrms
Ripple rejection	10 Hz < freq. < 3 kHz		65		dB

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	3 kHz < freq. < 1 MHz		40		dB
VTCXO Voltage					
Output voltage (V_TCXO)		2.7	2.8	2.9	V
Output current (Itcxo_max)			20		mA
Line regulation				TBD	mV
Load regulation				TBD	mV
Output noise voltage	f = 10 Hz to 100 kHz		50		µVrms
Ripple rejection	10 Hz < freq. < 3 kHz		65		dB
	3 kHz < freq. < 1 MHz		40		dB
RTC Voltage					
Output voltage		2.5	2.6	TBD	V
Output current limit (Irtc_max)			0.6		mA
Off reverse input current			1		µA
External Memory Voltage					
Output voltage (V_M)	VMSEL=L	1.7	1.8	1.9	V
	VMSEL=H	2.7	2.8	2.9	V
Output current (Im_max)			200		mA
Line regulation				TBD	mV
Load regulation				TBD	mV
SIM Voltage					
Output voltage (V_SIM)	Register RG_VSIM_SEL=0	1.71	1.8	1.89	V
	Register RG_VSIM_SEL=1	2.82	3.0	3.18	V
Output current (Isim_max)			80		mA
Line regulation				TBD	mV
Load regulation				TBD	mV
SIM2 Voltage					
Output voltage (V_SIM2)	Register RG_VSIM2_SEL=0	1.71	1.8	1.89	V
	Register RG_VSIM2_SEL=1	2.82	3.0	3.18	V
Output current (Isim2_max)			20		mA
Line regulation				TBD	mV
Load regulation				TBD	mV

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Memory card/Blue-Tooth Voltage					
Output voltage (V_BT)	Register VBT_SEL=L	2.7	2.8	2.9	V
	Register VBT_SEL=H	2.8	3.0	3.2	V
Output current (Ibt_max)			100		mA
Line regulation				TBD	mV
Load regulation				TBD	mV
USB Voltage					
Output voltage (V_USB)		2.97	3.3	3.63	V
Output current (Iusb_max)			100		mA
Line regulation				TBD	mV
Load regulation				TBD	mV
Digital Camera Voltage					
Output voltage (V_CAM_D)	Register VCAM_D_SEL=00	1.4	1.5	1.6	V
	Register VCAM_D_SEL=01	1.7	1.8	1.9	V
	Register VCAM_D_SEL=10	2.4	2.5	2.6	V
	Register VCAM_D_SEL=11	2.7	2.8	2.9	V
Output current (Icamera_max)			75		mA
Line regulation				TBD	mV
Load regulation				TBD	mV
Analog Camera Voltage					
Output voltage (V_CAM_A)	Register VCAM_A_SEL=00	1.2	1.3	1.4	V
	Register VCAM_A_SEL=01	1.4	1.5	1.6	V
	Register VCAM_A_SEL=10	1.7	1.8	1.9	V
	Register VCAM_A_SEL=11	2.7	2.8	2.9	V
Output current (Icamera_max)			150		mA
Line regulation				TBD	mV
Load regulation				TBD	mV

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KEYPAD LED Driver					
Sink Current of Key-Pad LED Driver	Von<0.5V		150		mA
Vibrator Driver					
Output voltage (V_VIBR)	Register VIBR_SEL=00	1.4	1.5	1.6	V
	Register VIBR_SEL=01	1.7	1.8	1.9	V
	Register VIBR_SEL=10	2.4	2.5	2.6	V
	Register VIBR_SEL=11	2.9	3.0	3.1	V
Output current (Ivibr_max)			150		mA
Line regulation				TBD	mV
Load regulation				TBD	mV

12.2.7.7.3 SIM interface

Parameter	Conditions	Min.	Typical	Max.	Unit
Interface to 3 V SIM Card					
Volrst	I = 20 µA			0.4	V
Vohrst	I = -200 µA	0.9*VSIM			V
Volclk	I = 20 µA			0.4	V
Vohclk	I = -200 µA	0.9*VSIM			V
Vihsio , Vohsio	I = ±20 µA	VSIM-0.4			V
Iil	Vil = 0 V			-1	mA
Vol	Iol = 1 mA			0.15*VSIM	V
Interface to 1.8 V SIM Card					
Volrst	I = 20 µA			0.2*VSIM	V
Vohrst	I = -200 µA	0.9*VSIM			V
Volclk	I = 20 µA			0.2*VSIM	V
Vohclk	I = -200 µA	0.9*VSIM			V
Vil				0.15*VSI	V

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				M	
Vihsio , Vohsio	I = ±20 µA	VSIM-0.4			V
Iil	Vil = 0 V			-1	mA
Vol	Iol = 1 mA			0.15*VSIM	V
SIM Card Interface Timing					
SIO pull-up resistance to VSIM		8	10	12	kΩ
SRST, SIO rise/fall times	VSIM = 3, 1.8 V, load with 30 pF			1	µs
SCLK rise/fall times	VSIM = 3 V, CLK load with 30 pF			18	ns
	VSIM = 1.8 V, CLK load with 30 pF			50	ns
SCLK frequency	CLK load with 30 pF	5			MHz
SCLK duty cycle	SIMCLK Duty = 50%, fsimclk = 5 MHz	47		53	%
SCLK propagation delay			30	50	ns

12.2.7.7.4 Charger Circuit

Parameter	Conditions	Min.	Typical	Max.	Unit
AC charger input voltage		4.2		8	V
AC charger detect on threshold (Vchg_on)	VBAT<3.2V	4.2		7	V
	VBAT>=3.2V	VBAT +120mV		7	V
Maximum charging current (AC charging)	VBAT>=3.2V		0.16 / R_{sense}		A
Pre-charging current	VBAT<2.3V		10		mA
	VBAT>=2.3V	TBD	100	TBD	mA
Pre-charging off threshold			3.2		V
Pre-charging off hysteresis			0.3		V
CC mode to CV mode threshold		4.15	4.2	4.25	V
BAT_ON (Vih)		2.4		2.6	V
GATEDRV rising time (T_r)	BAT_ON, or OV	1		5	µs
Over voltage protection threshold (OV)			4.3		V

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12.2.7.7.5 Regulators and Drivers

Item	LDO	Voltage	Current	Description
1	VCORE	1.8V/1.2V / 0.9V	200 mA	Digital core
2	VIO	2.8V	100 mA	Digital IO
3	VRF	2.8V	200 mA	RF chip
4	VA	2.8V	125 mA	Analog baseband
5	VRTC	1.2V	0.6 mA	Real-time clock
6	VM	1.8V / 2.8V	200 mA	External memory, selectable
7	VSIM	1.8V / 3.0V	80 mA	SIM card, selectable
8	VTCXO	2.8V	20 mA	13/26 MHz reference clock
9	VSIM2	1.8V / 3.0V	20 mA	SIM2 card, selectable
10	VUSB	3.3V	100 mA	USB
11	VBT	2.8V / 3.0V	100 mA	Memory card or Bluetooth
12	VCAM_A	1.5V / 1.8V / 2.5V / 2.8V	150 mA	Analog camera power
13	VCAM_D	1.3V / 1.5V / 1.8V / 2.8V	75 mA	Digital camera power

Driver	Type	Current	Description
LED	Open-drain NMOS switch	150 mA	Drives the keypad LEDs
VIBRATOR	Open-drain NMOS switch	150 mA	Drives the vibrator

The output current ratings for the above drivers already include a 50% margin on their nominal current consumption, e.g. if a regulator output is listed as 150 mA, the peak consumption current is 100 mA. In the active state, the phone consumes peak output current at each driver, which must be considered for the thermal design.

12.3 PMU Registers Definition

ADDRESS	TITLE	DESCRIPTION
8301_0800	**PMIC_VRF_CON**	**PMIC Vrf LDO control register**
8301_0804	**PMIC_VIO_CON**	**PMIC Vio LDO control register**
8301_0808	**PMIC_VM_CON**	**PMIC Vm LDO control register**
8301_080C	**PMIC_VRTC_CON**	**PMIC Vrtc LDO control register**

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8301_0810	PMIC_VTCXO_CON	PMIC Vtcxo LDO control register
8301_0814	PMIC_VA_CON	PMIC Va LDO control register
8301_0818	PMIC_VSIM_CON	PMIC Vsim LDO control register
8301_081C	PMIC_VSIM2_CON	PMIC Vsim2 LDO control register
8301_0820	PMIC_VUSB_CON	PMIC Vusb LDO control register
8301_0824	PMIC_VBT_CON	PMIC Vbt LDO control register
8301_0828	PMIC_VCAMD_CON	PMIC Vcamd LDO control register
8301_082C	PMIC_VCAMA_CON	PMIC Vcama LDO control register
8301_0830	PMIC_LDOS_CON	PMIC LDOS control register
8301_0834	PMIC_GPIO_CON	PMIC GPIO control register
8301_0840	PMIC_VCORE_CON0	PMIC Vcore control register 0
8301_0844	PMIC_VCORE_CON1	PMIC Vcore control register 1
8301_0848	PMIC_VCORE_CON2	PMIC Vcore control register 2
8301_084C	PMIC_VCORE_CON3	PMIC Vcore control register 3
8301_0850	PMIC_VCORE_CON4	PMIC Vcore control register 4
8301_0854	PMIC_VCORE_CON5	PMIC Vcore control register 5
8301_0860	PMIC_STARTUP_CON0	PMIC Startup control register 0
8301_0864	PMIC_STARTUP_CON1	PMIC Startup control register 1
8301_0870	PMIC_CHR_CON0	PMIC Charger control register 0
8301_0874	PMIC_CHR_CON1	PMIC Charger control register 1
8301_0878	PMIC_CHR_CON2	PMIC Charger control register 2
8301_087C	PMIC_CHR_CON3	PMIC Charger control register 3
8301_08F0	PMIC_CHR_CON4	PMIC Charger control register 4
8301_08F4	PMIC_CHR_CON5	PMIC Charger control register 5

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8301_0880	PMIC_DRIVER_CON0	PMIC Driver control register 0
8301_0884	PMIC_DRIVER_CON1	PMIC Driver control register 1
8301_0888	PMIC_DRIVER_CON2	PMIC Driver control register 2
8301_088C	PMIC_DRIVER_CON3	PMIC Driver control register 3
8301_0890	PMIC_DRIVER_CON4	PMIC Driver control register 4
8301_0894	PMIC_DRIVER_CON5	PMIC Driver control register 5
8301_08A0	PMIC_VBOOST_CON0	PMIC Vboost control register 0
8301_08A4	PMIC_VBOOST_CON1	PMIC Vboost control register 1
8301_08A8	PMIC_VBOOST_CON2	PMIC Vboost control register 2
8301_08AC	PMIC_VBOOST_CKS	PMIC Vboost clock setting
8301_08B0	PMIC_CLASSD_CON0	PMIC Class-D control register 0
8301_08B4	PMIC_CLASSD_CON1	PMIC Class-D control register 1
8301_08B8	PMIC_CLASSD_CON2	PMIC Class-D control register 2
8301_08BC	PMIC_CLASSD_CON3	PMIC Class-D control register 3
8301_08F8	PMIC_CLASSD_CKS	PMIC Class-D clock setting
8301_08C0	PMIC_TEST_CON0	PMIC TEST control register 0
8301_08C4	PMIC_TEST_CON1	PMIC TEST control register 1
8301_08C8	PMIC_TEST_CON2	PMIC TEST control register 2
8301_08D0	PMIC_OC_CON0	PMIC Over-Current control register 0
8301_08D4	PMIC_OC_CON1	PMIC Over-Current control register 1
8301_08D8	PMIC_OC_CON2	PMIC Over-Current control register 2
8301_08DC	PMIC_OC_CON3	PMIC Over-Current control register 3

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8301_08E0	**PMIC_OC_CON4**	**PMIC Over-Current control register 4**
8301_08E4	**PMIC_OC_CON5**	**PMIC Over-Current control register 5**
8301_08E8	**PMIC_OC_CON6**	**PMIC Over-Current control register 6**
8301_0A00	**ABIST_FQMTR_CON0**	**ABIST Frequency-Meter control register 0**
8301_0A04	**ABIST_FQMTR_CON1**	**ABIST Frequency-Meter control register 1**
8301_0A08	**ABIST_FQMTR_DATA**	**ABIST Frequency-Meter data register**
8301_0A0C	**ABIST_MON_CON0**	**ABIST Monitor control register 0**
8301_0A10	**ABIST_MON_CON1**	**ABIST Monitor control register 1**
8301_0A14	**ABIST_MON_DATA**	**ABIST Monitor data register**
8301_0A18	**ABIST_APC_CON**	**ABIST APC control register**

12.3.1 PMU Register Setting

0x8301_0800 PMIC Vrf LDO Control Register PMIC_VRF_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VRF_STATUS			RG_VRF_OCFB_EN		RG_VRF_ON_SEL			RG_VRF_CAL				RG_ICALRF_EN		RG_VRF_EN_FORCE	RG_VRF_EN
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				R/W		R/W	R/W
Reset	0	0	0	0	0	0	0	0	0000				00		0	0

Set this register for PMIC Vrf LDO circuit configuration controls.

VRF_STATUS Vrf LDO on/off status, excluding force enable.

- **0** Vrf is off
- **1** Vrf is on

RG_VRF_OCFB_EN Vrf over-current fold-back enable

- **0** disable
- **1** enable

RG_VRF_ON_SEL Vrf LDO enable control selection

- **0** enable with SRCLKENA
- **1** enable with RG_VRF_EN

RG_VRF_CAL Vrf LDO output voltage calibration (code in monotonic transfer function)

- **0** 0mV

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1 20mV
2 40mV
3 60mV
4 80 mV
5 100 mV
6 120 mV
7 140 mV
8 -160 mV
9 -140 mV
10 -120 mV
11 -100 mV
12 -80 mV
13 -60 mV
14 -40mV
15 -20mV

RG_ICALRF_EN Vrf LDO bias current calibration code
0 x1.0
1 x0.5
2 x2.0
3 x3.0

RG_VRF_EN_FORCE Vrf LDO force enable control signal
0 disable
1 enable

RG_VRF_EN Vrf LDO enable control signal
0 disable
1 enable

0x8301_0804 PMIC Vio LDO Control Register PMIC_VIO_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIO_STATUS			RG_VIO_OCFB_EN			RG_VD_SENSE_VIO	RG_ANTIUDSH_IO_DN	RG_VIO_CAL				RG_ICALIO_EN		RG_VIO_EN_FORCE	
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				R/W		R/W	R/W
Reset	0	0	0	0	0	0	0	0	0000				00		0	0

Set this register for PMIC Vio LDO circuit configuration controls.

VIO_STATUS Vio LDO on/off status, excluding force enable.
0 Vio is off
1 Vio is on

RG_VIO_OCFB_EN Vio LDO fold-back enable control signal
0 disable

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1 enable

RG_ANTIUDSH_IO_DN Vio LDO anti-undershoot disable control signal

0 enable
1 disable

RG_VD_SENSE_VIO Vio LDO local/remote sense setting

0 Default Local Sense
1 Set to Remote Sense

RG_VIO_CAL Vio LDO output voltage calibration (code in monotonic transfer function)

0 0mV
1 20mV
2 40mV
3 60mV
4 80 mV
5 100 mV
6 120 mV
7 140 mV
8 -160 mV
9 -140 mV
10 -120 mV
11 -100 mV
12 -80 mV
13 -60 mV
14 -40mV
15 -20mV

RG_ICALIO_EN Vio LDO bias current calibration code

0 x1.0
1 x0.5
2 x2.0
3 x3.0

RG_VIO_EN_FORCE Vio LDO force enable control signal

0 Disable
1 Enable

0x8301_0808 PMIC Vm LDO Control Register PMIC_VM_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VM_STATUS			RG_VM_OCFB_EN			RG_VD_SENSE_VM	RG_ANTIUDSH_M_DN	RG_VM_CAL				RG_ICALM_EN		RG_VM_EN_FORCE	
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				R/W		R/W	R/W
Reset	0	0	0	0	0	0	0	0	0000				00		0	0

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Set this register for PMIC Vm LDO circuit configuration controls.

VM_STATUS Vm LDO on/off status, excluding force enable.

- **0** Vm is off
- **1** Vm is on

RG_VM_OCFB_EN Vm LDO fold-back enable control signal

- **0** disable
- **1** enable

RG_VD_SENSE_VM VM LDO local/remote sense setting **(NO USE)**.

- **0** (Default) Local Sense
- **1** Set to Remote Sense

RG_ANTIUDSH_M_DN Vm LDO anti-undershoot disable control signal

- **0** enable
- **1** disable

RG_VM_CAL Vm LDO output voltage calibration (code in monotonic transfer function)

- **0** 0mV
- **1** 20mV
- **2** 40mV
- **3** 60mV
- **4** 80 mV
- **5** 100 mV
- **6** 120 mV
- **7** 140 mV
- **8** -160 mV
- **9** -140 mV
- **10** -120 mV
- **11** -100 mV
- **12** -80 mV
- **13** -60 mV
- **14** -40mV
- **15** -20mV

RG_ICALM_EN Vm LDO bias current calibration code

- **0** x1.0
- **1** x0.5
- **2** x2.0
- **3** x3.0

RG_VM_EN_FORCE Vm LDO force enable control signal

- **0** disable
- **1** enable

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0x8301_080C PMIC Vrtc LDO Control Register PMIC_VRTC_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VRTC_STATUS								RG_VRTC_CAL						RG_VRTC_EN_FORCE	
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0000				0	0	0	0

Set this register for PMIC Vrtc LDO circuit configuration controls.

VRTC_STATUS Vrtc LDO on/off status, excluding force enable.

- **0** Vrtc is off
- **1** Vrtc is on

RG_VRTC_CAL Vrtc LDO output voltage calibration (code in monotonic transfer function)

- **0** 0 mV
- **1** 60 mV
- **2** 120 mV
- **3** 180 mV
- **4** 240 mV
- **5** 300 mV
- **6** 360 mV
- **7** 420 mV
- **8~15** Reserved

RG_VRTC_EN_FORCE Vrtc LDO force enable control signal

- **0** disable
- **1** enable

0x8301_0810 PMIC Vtcxo LDO Control Register PMIC_VTCXO_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VTCXO_STATUS			RG_VTCXO_OCFB_EN	SRCLKEN	RG_VTCXO_ON_SEL			RG_VTCXO_CAL				RG_ICALTCXO_EN		RG_VTCXO_EN_FORCE	RG_VTCXO_EN
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				R/W		R/W	R/W
Reset	0	0	0	0	0	0	0	0	0000				00		0	0

Set this register for PMIC Vtcxo LDO circuit configuration controls.

VTCXO_STATUS Vtcxo LDO on/off status, excluding force enable.

- **0** Vtcxo is off
- **1** Vtcxo is on

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RG_VTCXO_OCFB_EN Vtcxo LDO fold-back enable control signal

0 disable
1 enable

SRCLKEN SRCLKENA to PMIC force enable control signal

0 disable (****controlled by sleep control module)
1 enable

RG_VTCXO_ON_SEL Vtcxo LDO enable control selection signal

0 enable with SRCLKENA
1 enable with RG_VTCXO_EN

RG_VCTXO_CAL Vtcxo LDO output voltage calibration (code in monotonic transfer function)

0 0 mV
1 20 mV
2 40 mV
3 60 mV
4 80 mV
5 100 mV
6 120 mV
7 140 mV
8 -160 mV
9 -140 mV
10 -120 mV
11 -100 mV
12 -80 mV
13 -60 mV
14 -40 mV
15 -20 mV

RG_ICALTCXO_EN Vtcxo LDO bias current calibration code

0 x1.0
1 x0.5
2 x2.0
3 x3.0

RG_VCTXO_EN_FORCE Vtcxo LDO force enable control signal

0 disable
1 enable

RG_VCTXO_EN Vtcxo LDO Enable Control Signal

0 disable
1 enable (****it would force Vtcxo LDO enabled discarding sleep control ==> SRCLKENA)

0x8301_0814 PMIC Va LDO Control Register PMIC_VA_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	VA_STATUS			RG_VA_OCFB_EN		RG_VA_ON_SEL	RG_VD_SENSE_VA		RG_VA_CAL	RG_ICALA_EN	RG_VA_EN_FORCE	
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0000	00	0	0

Set this register for PMIC Va LDO circuit configuration controls.

VA_STATUS Va LDO on/off status, excluding force enable.

- **0** Va is off
- **1** Va is on

RG_VA_OCFB_EN Va LDO fold-back enable control signal

- **0** disable
- **1** enable

RG_VA_ON_SEL Va LDO enable control selection

- **0** always on
- **1** enable with SRCLKENA

RG_VD_SENSE_VA Va LDO voltage sense control selection

- **0** sense from local voltage
- **1** sense from remote voltage

RG_VA_CAL Va LDO output voltage calibration (code in monotonic transfer function)

- **0** 0 mV
- **1** 20 mV
- **2** 40 mV
- **3** 60 mV
- **4** 80 mV
- **5** 100 mV
- **6** 120 mV
- **7** 140 mV
- **8** -160 mV
- **9** -140 mV
- **10** -120 mV
- **11** -100 mV
- **12** -80 mV
- **13** -60 mV
- **14** -40 mV
- **15** -20 mV

RG_ICALA_EN Va LDO bias current calibration code

- **0** x1.0
- **1** x0.5
- **2** x2.0

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3 x3.0

RG_VA_EN_FORCE Va LDO force enable control signal

0 disable

1 enable

0x8301_0818 PMIC Vsim LDO Control Register PMIC_VSIM_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VSIM_STATUS			RG_VSIM_OCFB_EN	VSIM_PWR_SAVING	VSIM_SEL	RG_SIM_DATAL	RG_ANTIUDSH_SIM_DN	RG_VSIM_CAL				RG_ICALSIM_EN		RG_VSIM_EN_FORCE	VSIM_EN
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				R/W		R/W	R/W
Reset	0	0	0	1	0	0	0	0	0000				00		0	0

Set this register for PMIC Vsim LDO circuit configuration controls.

VSIM_STATUS Vsim LDO on/off status, excluding force enable.

0 Vsim is off

1 Vsim is on

RG_VSIM_OCFB_EN Vsim LDO fold-back enable control signal

0 disable

1 enable

VSIM_PWR_SAVING Used for power saving. Since design topology of SIM LS, SIM data out path tends to conduct leakage current when Vsim LDO is not enable if default SIM data output is kept low. If the power saving is enabled, SIM data output will keep high before Vsim LDO is turned on.

0 disable

1 enable

VSIM_SEL Only valid for analog test mode. For normal operation, this LDO voltage select is actually connected to “simsel” port of PMIC SIM circuit. Vsim LDO voltage selection.

0 1.8V

1 3.0V

RG_SIM_DATAL SIO pull-low when enabling the data path (Reference **MT6302**).

0 no pull-low

1 pull-low

RG_ANTIUDSH_SIM_DN Vsim LDO anti-undershoot disable control signal

0 enable

1 disable

RG_VSIM_CAL Vsim LDO output voltage calibration (code in monotonic transfer function)

0 0 mV

1 -20 mV

2 -40 mV

3 -60 mV

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4 -80 mV
5 -100 mV
6 -120 mV
7 -140 mV
8 160 mV
9 140 mV
10 120 mV
11 100 mV
12 80 mV
13 60 mV
14 40 mV
15 20 mV

RG_ICALSIM_EN Vsim LDO bias current calibration code
0 x1.0
1 x0.5
2 x2.0
3 x3.0

RG_VSIM_EN_FORCE Vsim LDO force enable control signal
0 disable
1 enable

VSIM_EN Only valid for analog test mode. For normal operation, this LDO enable is actually connected to "simvcc" port of PMIC SIM circuit.
0 disable
1 enable

0x8301_081C PMIC Vsim2 LDO Control Register PMIC_VSIM2_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VSIM2_STATUS					VSIM2_SEL	RG_SIM2_DATAL	RG_ANTIUDSH_SIM2_DN	RG_VSIM2_CAL				RG_ICALSIM2_EN		RG_VSIM2_EN_FORCE	VSIM2_EN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				R/W		R/W	R/W
Reset	0	0	0	0	0	0	0	0	0000				00		0	0

Set this register for PMIC Vsim2 LDO circuit configuration controls.

VSIM2_STATUS Vsim2 LDO on/off status, excluding force enable.
0 Vsim2 is off
1 Vsim2 is on

VSIM2_SEL Vsim2 LDO voltage selection. Only valid for analog test mode. For normal operation, this LDO voltage select is actually connected to "sim2sel" port of PMIC SIM2 hardware.

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0 1.8V
1 3.0V

RG_VSIM2_DATAL SIO2 pull-low when enabling the data path.

0 no pull-low
1 pull-low

RG_ANTIUDSH_SIM2_DN Vsim2 LDO anti-undershoot disable control signal

0 enable
1 disable

RG_VSIM2_CAL Vsim2 LDO output voltage calibration (code in monotonic transfer function)

0 0 mV
1 -20 mV
2 -40 mV
3 -60 mV
4 -80 mV
5 -100 mV
6 -120 mV
7 -140 mV
8 160 mV
9 140 mV
10 120 mV
11 100 mV
12 80 mV
13 60 mV
14 40 mV
15 20 mV

RG_ICALSIM2_EN Vsim2 LDO bias current calibration code

0 x1.0
1 x0.5
2 x2.0
3 x3.0

RG_VSIM2_EN_FORCE Vsim2 LDO force enable control signal

0 disable
1 enable

VSIM2_EN Only valid for analog test mode. For normal operation, this LDO enable is actually connected to "sim2vcc" port of PMIC SIM2 hardware.

0 Disable
1 Enable

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0x8301_0820 PMIC Vusb LDO Control Register PMIC_VUSB_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VUSB_STATUS			RG_VUSB_OCFB_EN				RG_ANTIUDSH_USB_DN	RG_VUSB_CAL				RG_ICALUSB_EN		RG_VUSB_EN_FORCE	RG_VUSB_EN
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				R/W		R/W	R/W
Reset	0	0	0	0	0	0	0	0	0000				00		0	1

Set this register for PMIC Vusb LDO circuit configuration controls.

VUSB_STATUS Vusb LDO on/off status, excluding force enable.
- **0** Vusb is off
- **1** Vusb is on

RG_VUSB_OCFB_EN Vusb LDO fold-back enable control signal
- **0** disable
- **1** enable

RG_ANTIUDSH_USB_DN Vusb LDO anti-undershoot disable control signal
- **0** enable
- **1** disable

RG_VUSB_CAL Vusb LDO output voltage calibration (code in monotonic transfer function)
- **0** 0 mV
- **1** -20 mV
- **2** -40 mV
- **3** -60 mV
- **4** -80 mV
- **5** -100 mV
- **6** -120 mV
- **7** -140 mV
- **8** 160 mV
- **9** 140 mV
- **10** 120 mV
- **11** 100 mV
- **12** 80 mV
- **13** 60 mV
- **14** 40 mV
- **15** 20 mV

RG_ICALUSB_EN Vusb LDO bias current calibration code
- **0** x1.0
- **1** x0.5

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2 x2.0

3 x3.0

RG_VUSB_EN_FORCE Vusb LDO force enable control signal

0 disable

1 enable

RG_VUSB_EN Vusb LDO enable control signal

0 disable

1 enable

0x8301_0824 PMIC Vbt LDO Control Register PMIC_VBT_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VBT_STATUS			RG_VBT_OCFB_EN		RG_VBT_SEL		RG_ANTIUDSH_BT_DN	RG_VBT_CAL				RG_ICALBT_EN		RG_VBT_EN_FORE	RG_VBT_EN
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				R/W		R/W	R/W
Reset	0	0	0	1	0	0	0	0	0000				00		0	0

Set this register for PMIC Vbt LDO circuit configuration controls.

VBT_STATUS Vbt LDO on/off status, excluding force enable.

0 Vbt is off

1 Vbt is on

RG_VBT_OCFB_EN Vbt LDO fold-back enable control signal

0 disable

1 enable

RG_VBT_SEL Vbt LDO voltage selection

0 2.8V

1 3.0V

RG_ANTIUDSH_BT_DN Vbt LDO anti-undershoot disable control signal

0 enable

1 disable

RG_VBT_CAL Vbt LDO output voltage calibration (code in monotonic transfer function)

0 0 mV

1 -20 mV

2 -40 mV

3 -60 mV

4 -80 mV

5 -100 mV

6 -120 mV

7 -140 mV

8 160 mV

9 140 mV

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10 120 mV
11 100 mV
12 80 mV
13 60 mV
14 40 mV
15 20 mV

RG_ICALBT_EN Vbt LDO bias current calibration code

0 x1.0
1 x0.5
2 x2.0
3 x3.0

RG_VBT_EN_FORCE Vbt LDO force enable control signal

0 disable
1 enable

RG_VBT_EN Vbt LDO enable control signal

0 disable
1 enable

0x8301_0828 PMIC Vcamd LDO Control Register PMIC_VCAMD_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VCAMD_STATUS			RG_VCAMD_OCFB_EN	RG_VCAMD_SEL			RG_ANTIUDSH_CAMD_DN	RG_VCAMD_CAL				RG_ICALCAMD_EN		RG_VCAMD_EN_FORCE	RG_VCAMD_EN
Type	R	R/W	R/W	R/W	R/W		R/W	R/W	R/W				R/W		R/W	R/W
Reset	0	0	0	1	00		0	0	0000				00		0	0

Set this register for PMIC Vcamd LDO circuit configuration controls.

VCAMD_STATUS Vcamd LDO on/off status, excluding force enable.

0 Vcamd is off
1 Vcamd is on

RG_VCAMD_OCFB_EN Vcamd LDO fold-back enable control signal

0 disable
1 enable

RG_VCAMD_SEL Vcamd LDO voltage selection

0 1.3V
1 1.5V
2 1.8V
3 2.8V

RG_ANTIUDSH_CAMD_DN Vcamd LDO anti-undershoot disable control signal

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0 enable
1 disable

RG_VCAMD_CAL Vcamd LDO output voltage calibration (code in monotonic transfer function)

0 0 mV
1 -20 mV
2 -40 mV
3 -60 mV
4 -80 mV
5 -100 mV
6 -120 mV
7 -140 mV
8 160 mV
9 140 mV
10 120 mV
11 100 mV
12 80 mV
13 60 mV
14 40 mV
15 20 mV

RG_ICALCAMD_EN Vcamd LDO bias current calibration code

0 x1.0
1 x0.5
2 x2.0
3 x3.0

RG_VCAMD_EN_FORCE Vcamd LDO force enable control signal

0 disable
1 enable

RG_VCAMD_EN Vcamd LDO enable control signal

0 disable
1 enable

0x8301_082C PMIC Vcama LDO Control Register PMIC_VCAMA_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VCAMA_STATUS			RG_VCAMA_OCFB_EN	RG_VCAMA_SEL				RG_VCAMA_CAL				RG_ICALCAMA_EN		RG_VCAMA_EN_FORCE	RG_VCAMA_EN
Type	R	R/W	R/W	R/W	R/W		R/W	R/W	R/W				R/W		R/W	R/W
Reset	0	0	0	1	00		0	0	0000				00		0	0

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Set this register for PMIC Vcama LDO circuit configuration controls.

VCAMA_STATUS Vcama LDO on/off status, excluding force enable.

- **0** Vcama is off
- **1** Vcama is on

RG_VCAMA_OCFB_EN Vcama LDO fold-back enable control signal

- **0** disable
- **1** enable

VCAMA_SEL Vcama LDO output voltage selection

- **0** 1.5V
- **1** 1.8V
- **2** 2.5V
- **3** 2.8V

RG_VCAMA_CAL Vcama LDO output voltage calibration (code in monotonic transfer function)

- **0** 0 mV
- **1** 20 mV
- **2** 40 mV
- **3** 60 mV
- **4** 80 mV
- **5** 100 mV
- **6** 120 mV
- **7** 140 mV
- **8** -160 mV
- **9** -140 mV
- **10** -120 mV
- **11** -100 mV
- **12** -80 mV
- **13** -60 mV
- **14** -40 mV
- **15** -20 mV

RG_ICALCAMA_EN Vcama LDO bias current calibration code

- **0** x1.0
- **1** x0.5
- **2** x2.0
- **3** x3.0

RG_VCAMA_EN_FORCE Vcama LDO force enable control signal

- **0** disable
- **1** enable

RG_VCAMA_EN Vcama LDO enable control signal

- **0** disable

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1 enable

0x8301_0830 PMIC LDOS Control Register PMIC_LDOS_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OLT_TEST	RG_OCFB_CAL		RG_LDOS_TEST_EN	RG_VOSEL_TEST				RG_LDOS_RSV							
Type	R/W	R/W		R/W	R/W				R/W							
Reset	0	00		0	0000				00000000							

Set this register for PMIC LDOS circuit configuration controls.

RG_OLT_TEST LDO OLT test mode enable

0 normal mode

1 OLT test mode

RG_OCFB_CAL OC foldback level calibration

0 0.75V

1 0.80V

2 0.85V

3 0.90V

RG_LDOS_TEST_EN LDO test mode enable

0 normal mode

1 test mode

RG_VOSEL_TEST Not Used (reserved for future usage).

RG_LDOS_RSV Reserved

0X8301_0834 PMIC GPIO Control Register PMIC_GPIO_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							MTV_EN	RG_GPIO_DRV	RG_VSIM_RSV[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W							
Reset	0	0	0	0	0	0	0	0	00000000							

Set this register for PMIC SIM2 interface as GPIO configuration controls.

MTV_EN Define Mobile TV application, the register is only for test mode. If GPIO in normal function is intended, please refer to “General-purpose IO” chapter

0 Mobile-TV application, SCLK2/SRST2/SIO2 are used as GPIO pins.

1 SIM2 application, SCLK2/SRST2/SIO2 are used as SIM2 interface.

RG_GPIO_DRV SCLK2/SRST2/SIO2 GPIO Driving Strength Control

0 8mA

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1 4mA

RG_VSIM_RSV Reserved

0X8301_0840 PMIC Vcore Control Register 0 PMIC_VCORE_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VCORE_STATUS						RG_VD_SENSE_VCORE	RG_ANTIUDSH_CORE_DN	RG_VCORE_CAL				RG_ICALCORE_EN		RG_VCORE_EN_FORCE	
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				R/W		R/W	R/W
Reset	0	0	0	0	0	0	0	0	0000				00		0	0

Set this register for PMIC Vcore LDO circuit configuration controls.

VCORE_STATUS Vcore LDO on/off status, excluding force enable.

0 Vcore is off

1 Vcore is on

RG_ANTIUDSH_CORE_DN Vcore LDO anti-undershoot disable control signal

0 enable

1 disable

RG_VD_SENSE_VCORE Vcore LDO voltage sense control selection

0 sense from local voltage

1 sense from remote voltage

RG_VCORE_CAL Vcore LDO output voltage calibration (code in monotonic transfer function)

0 0 mV

1 48 mV

2 100 mV

3 148 mV

4 200 mV

5 248 mV

6 300 mV

7 348 mV

8 -400 mV

9 -352 mV

10 -300 mV

11 -252 mV

12 -200 mV

13 -152 mV

14 -100 mV

15 -52 mV

RG_ICALCORE_EN Vcore LDO bias current calibration code

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0 x1.0
1 x0.5
2 x2.0
3 x3.0

VCORE_EN_FORCE Vcore LDO force enable control signal for MCU write.
0 disable
1 enable

0X8301_0844 PMIC Vcore Control Register 1 PMIC_VCORE_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_VCORE_ACC_OUT_INIT				RG_VCORE_PWMB	RG_VCORE_FAST_SLOW	RG_VCORE_ADC_IN_EDGE	RG_VCORE_MODESET
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	1100				1	1	0	1

Set this register for PMIC Vcore DC-DC circuit configuration controls.

RG_VCORE_ACC_OUT_INIT PID compensator integrator initial value setup
(The MSB 4-bits of Integrator output bit-string, default=1100)
0000 0
……
1100 Default
1111 Highest Initial Integrator State.

RG_VCORE_PWMB select PWM bit resolution
0 3 bits
1 4 bits

RG_VCORE_FAST_SLOW PWM switching frequency
0 26MHz divided by 32
1 26MHz divided by 16

RG_ADC_IN_EDGE use positive/negative edge as ADC_COUNTER input
0 negative edge
1 positive edge

RG_VCORE_MODESET Manual mode setting
0 PWM mode
1 PFM mode

0X8301_0848 PMIC Vcore Control Register 2 PMIC_VCORE_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	RG_VCORE_FBEN	RG_VCORE_VOSEL	RG_VCORE_DUTY_INIT	RG_VCORE_GAIND	RG_VCORE_GAINI	RG_VCORE_GAINP	RG_VCORE_SDM_ORDER
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1000	010	100	010	1

Set this register for PMIC Vcore DC-DC circuit configuration controls.

RG_VCORE_FBEN SDM feedback path enable

0 disable

1 enable

RG_VCORE_VOSEL Vcore output voltage select

0 1.4V ~ 2.2V

1 0.8V ~ 1.6V

RG_VCORE_DUTY_INIT DCV test mode monitor select (2MSB: AO_SEL; 2LSB: DO_SEL)

00xx Select AO1 through the Test Mode MUX to be the AO

01xx Select AO2 through the Test Mode MUX to be the AO

10xx Select AO3 through the Test Mode MUX to be the AO

11xx Select AO4 through the Test Mode MUX to be the AO

xx00 Select DO1 through the Test Mode MUX to be the DO

xx01 Select DO2 through the Test Mode MUX to be the DO

xx10 Select DO3 through the Test Mode MUX to be the DO

xx11 Select DO4 through the Test Mode MUX to be the DO

RG_VCORE_GAIND PID derivative gain select

MSB:

00 2

01 4

01 8

11 16

LSB: x 1.5

RG_VCORE_GAINI PID integration gain select

MSB:

00 0.015625

01 0.03125

01 0.0625

11 0.125

LSB: x 1.5

RG_VCORE_GAINP PID proportional gain select

MSB:

00 0.25

01 0.5

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01 1
11 2
LSB: x 1.5

RG_VCORE_SDM_ORDER SDM order selection

0 1st order
1 2nd order

0X8301_084C PMIC Vcore Control Register 3 PMIC_VCORE_CON3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VCORE_DCV_TEST_EN	RG_VCORE_MODESELIA	RG_VCORE_MODECMP	RG_VCORE_MODEEN		RG_VCORE_ADJCKSEL			RG_VCORE_ISEL		RG_VCORE_DCVCKSEL	RG_VCORE_DIRECT_CTRL_EN	VCORE_VFBADJ			
Type	R/W	R/W	R/W	R/W		R/W			R/W		R/W	R/W	R/W			
Reset	0	1	0	01		100			10		1	0	1000			

Set this register for PMIC Vcore DC-DC circuit configuration controls.

RG_VCORE_DCV_TEST_EN DCV test mode enable

0 normal mode
1 test mode

RG_VCORE_MODESEL1A Select average current mode

0 NCD mode
1 average current mode

RG_VCORE_MODECMP Select comparator entering PWM mode

0 low offset comparator
1 auto-zero comparator

RG_VCORE_MODEEN Enable auto mode change

00 manual change mode
01 auto change mode
10 SW (RG_MODESET)
11 auto change mode

RG_VCORE_ADJCKSEL Internal free run ring oscillator frequency adjustment

0 Slowest Frequency
…
4 0 (~ 26MHz, internal)
7 Fastest Frequency

RG_VCORE_ISEL Reference gen bias current select

00 0.25X
01 1.5X

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10 1.0X
11 2.0X

RG_VCORE_DCVCKSEL DCV digital PWM clock source select
0 internal free run ring oscillator
1 external clock

RG_VCORE_DIRECT_CTRL_EN Vcore voltage feedback direct feed-through
0 DVFS
1 direct feed through

VCORE_VFBADJ Vcore output voltage soft adjustment (4 bits resolution) "0000" ~ "1111" 16 step, 50mV/step when not in sleep mode (SRLKENA == 1)
0 0.85V
1 0.90V
2 0.95V
3 1.00V
.....
8 1.25V (default)
.....
13 1.55V
14 1.55V
15 1.60V

0X8301_0850 PMIC Vcore Control Register 4 PMIC_VCORE_CON4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VCORE_RSEL		RG_VCORE_IASEL		RG_VCORE_DCVTRIM			RG_VCORE_NCDOF		RG_VCORE_PFMISEL						
Type	R/W		R/W		R/W			R/W		R/W						
Reset	01		01		011			10		0000110						

Set this register for PMIC Vcore DC-DC circuit configuration controls.

RG_VCORE_RSEL Curdet bias current select
00 32k
01 28k
10 24k
11 18k

RG_VCORE_IASEL Select vavgl
00 50mV
01 100mV
10 150mV
11 200mV

RG_VCORE_DCVTRIM Reference voltage trimming . Each step = 10mV (for Vout=1.2V)

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0 -30 mV
1 -20 mV
2 -10 mV
3 0 mV
4 10mV
5 20 mV
6 30 mV
7 40 mV

RG_VCOE_NCDOF NCD comparator offset

00 -3mV
01 +5mV
10 +12mV
11 +17mV

RG_VCORE_PFMISEL[6:4] PFM max load current select (proportional to Vin)

6 50 Ω
5 100 Ω
4 200 Ω

RG_VCORE_PFMISEL[3:0] PFM max load current select (constant bias)

3 160mA
2 80mA
1 40mA
0 20mA

0X8301_0854 PMIC Vcore Control Register 5 PMIC_VCORE_CON5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VCORE_RSV					RG_VCORE_DCV_SLEW_CTRL			RG_VCORE_DCV_SLEW_CTRL_NMOS			RG_VCORE_CLK_SOURCE_SEL	VCORE_VFBADJ_SLP			
Type	R/W				R/W	R/W			R/W		R/W	R/W	R/W			
Reset	0000				0	000			00		0	0	0000			

Set this register for PMIC Vcore DC-DC circuit configuration controls.

RG_VCORE_RSV Reserved

RG_VCORE_DCV_SLEW_CTRL Power MOS turn on/off slew rate control

0 1.00X
1 0.75X
2 0.50X
3 0.25X

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RG_VCORE_CLK_SOURCE_SEL Select 26MHz clock source for Vcore PWM control

- **0** 26MHz clock directly from CLKSQ (2.8V)
- **1** 26MHz clock from TCXO26M_CK (1.2V) (****which test mux in digital domain)

VCORE_VFBADJ_SLP Vcore output voltage soft adjustment (4 bits resolution) "0000" ~ "1111" 16 step, 50mV/step when in sleep mode (SRLKENA == 0)

- **0** 0.85V
- **1** 0.90V
- **2** 0.95V
- **3** 1.00V
- **.....**
- **8** 1.25V
- **.....**
- **13** 1.50V
- **14** 1.55V
- **15** 1.60V

0x8301_0860 PMIC Start-Up Control Register 0 PMIC_STARTUP_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PWRKEY_DEB	PWRKEY_VCORE			RG_BIAS_GEN_FORCE	RG_IBIASSEL		RG_CK_SEL	RG_OSC_ENB	RG_IBG_SEL		RG_VBG_SEL			RG_UV_SEL	
Type	R	R	R/W	R/W	R/W	R/W		R/W	R/W	R/W		R/W			R/W	
Reset	0	0	0	0	0	00		0	0	00		000			0	

Set this register for PMIC Start-up circuit configuration controls.

PWRKEY_DEB PWRKEY signal status (with de-bounce)

- **0** PWRKEY is low
- **1** PWRKEY is high

PWRKEY_VCORE PWRKEY signal status (without de-bounce)

- **0** PWRKEY is low
- **1** PWRKEY is high

RG_BIAS_GEN_EN_FORCE Force the IBIAS/VBIAS generator on in the test mode

- **0** normal
- **1** force on

RG_IBIASSEL Internal reference current tuning (global bias of PMU)

- **00** VBG/1200K
- **01** VBG/1320K
- **10** VBG/960K
- **11** VBG/1080K

RG_CK_SEL Setting the clock rate of CKMON

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0 ~10kHz
1 ~5kHz

RG_OSC_ENB Enable the oscillator in band-gap block
0 enable
1 disable

RG_IBG_SEL Current setting for band-gap and oscillator
00 +0 (initial setting)
01 +1 step
10 -2 step
11 -1 step

RG_VBG_SEL Band-gap T.C. fine tuning
000 +0 (initial setting)
001 +1 step
010 +2 step
011 +3 step
100 -4 step
101 -3 step
110 -2 step
111 -1 step

RG_UV_SEL UVLO high to low threshold selection
00 2.9V
01 2.75V
10 2.6V
11 follow DDLO

0x8301_0864 PMIC Start-Up Control Register 1 PMIC_STARTUP_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_START_RSV			RG_THR_SEL		RG_VREF_BG		
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			R/W		R/W		
Reset	0	0	0	0	0	0	0	0	000			00		000		

Set this register for PMIC Start-up circuit configuration controls.

RG_START_RSV Reserved

RG_THR_SEL Thermal shut-down threshold fine tuning
00 Initial setting
01 +10˚C
10 -20˚C
11 -10˚C

RG_VREF_BG Reference voltage fine tuning according to VBG

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000 +0 (initial setting)
001 +1 step
010 +2 step
011 +3 step
100 -4 step
101 -3 step
110 -2 step
111 -1 step

0x8301_0870 PMIC Charger Control Register 0 PMIC_CHR_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OV_TH_FREEZE	RG_OV_TH_HIGH	RG_CV_TUNE			RG_CV_RT		RG_CHRON_FORCE	RG_CLASS_D				RG_CHOFST			RG_CHR_EN
Type	R/W	R/W	R/W			R/W		R/W	R/W				R/W			R/W
Reset	0	0	000			00		0	0000				000			0

Set this register for PMIC Charger circuit configuration controls.

RG_OV_TH_FREEZE OV threshold freeze at 4.3V
0 OV threshold auto tuning
1 fixed OV threshold

RG_OV_TH_HIGH Set the OV threshold when RG_OV_TH_FREEZE=1
0 lower
1 higher

RG_CV_TUNE Fine tune the CV voltage according to VREF
000 VBG = 1.200V
001 VBG = 1.205V
010 VBG = 1.210V
011 VBG = 1.215V
100 VBG = 1.180V
101 VBG = 1.185V
110 VBG = 1.190V
111 VBG = 1.195V

RG_CV_RT Coarse tune the CV voltage according to VREF
00 -407mV
01 -667mV
10 0
11 -260mV

RG_CHRON_FORCE Charger force enable control signal
0 disable (normal)

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1 enable (force charge on)

RG_CLASS_D CC mode charge current level

000 50.0mA
001 87.5mA
010 150mA
011 225mA
100 300mA
101 450mA
110 650mA
111 800mA

RG_CHOFST Charging current offset (for CC mode current calibration)

000 +0 step
001 +1 step
010 +2 step
011 +0 step
100 +0 step
101 +0 step
110 -2 step
111 -1 step

RG_CHR_EN Enable charging (CC and CV mode)

0 disable
1 enable

0x8301_0874 PMIC Charger Control Register 1 PMIC_CHR_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CHROV_SEL		RG_OT_CAL					RG_PS_SET	RG_PS_SEL	RG_CAL_CM2		RG_CAL_CM		RG_CAL_PRECC	
Type	R/W	R/W		R/W					R/W	R/W	R/W		R/W		R/W	
Reset	0	00		00000					0	0	00		00		00	

Set this register for PMIC Charger circuit configuration controls.

RG_CHROV_SEL Set the OV level of charger protection

00 5.5V
01 6.0V
10 6.5V
11 7.0V

RG_OT_CAL Calibrate the 24K temperature sensing resistor

0 Not Used
1 Not Used

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RG_PS_SET System power source set, if RG_PS_SEL=1

- **0** VBAT
- **1** AC

RG_PS_SEL System power source selection

- **0** default setting after charger plug in
- **1** according to RG_PS_SET value (VBAT or AC)

RG_CAL_CM2 Increase system LDO Nested-Miller compensation capacitance by

- **00** 0.0 pF
- **01** 0.5 pF
- **10** 1.0 pF
- **11** 1.5 pF

RG_CAL_CM Increase system LDO Miller compensation capacitance by

- **00** 0.0 pF
- **01** 5.0 pF
- **10** 10 pF
- **11** 15 pF

RG_CAL_PRECC Set Pre-CC mode charging current

- **00** 50.0mA
- **01** 87.5mA
- **10** 150mA
- **11** 225mA

0x8301_0878 PMIC Charger Control Register 2 PMIC_CHR_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TESTMODE_POR	CV	BAD_BATT	BAT_ON	CHRDET	OVP	RG_CHR_RCT_RSV						RG_CHR_RSV			
Type	R	R	R	R	R	R	R/W						R/W			
Reset	0	0	0	0	0	0	000000						0000			

Set this register for PMIC Charger circuit configuration controls.

TESTMODE_POR Not in Charging. Reserved. This register is used by PMU to indicate the test mode when being true. Under the test mode, the system reset, power key, and SIM card data input would come from external PMIC, rather than from PMU.

- **0** normal
- **1** test mode

CV CV mode Indicated signal

- **0** normal
- **1** CV mode

BAD_BATT Bad battery indicated signal

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0 normal
1 battery is bad

BAT_ON Battery detected indicated signal
0 battery is removed
1 battery is connected

OVP Charger OVP idicated signal
0 AC < 8V
1 AC > 8V

CHRDET Charger detected indicated signal
0 No charger
1 charger plug-in. The signal is connected to EINT8 (active low), acting as an internal interrupt, that can wake-up base-band chip even in sleep mode.

AC_DET AC power detected. Reserved

RG_CHR_RCT_RSV Reserved

RG_CHR_RSV Reserved

0x8301_087C PMIC Charger Control Register 3 PMIC_CHR_CON3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														WDTIMER_EN	WDTIMER_TD	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Set this register for PMIC Charger circuit configuration controls.

WDTIMER_EN Enable setting for chr_en watch-dog timer
0 disable
1 enable

WDTIMER_TD Time constant setting for chr_en watch-dog timer
00 4.0 Sec
01 8.0 Sec
10 16.0 Sec
11 32.0 Sec

0x8301_08F0 PMIC Charger Control Register 4 PMIC_CHR_CON4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDTIMER_CNT[19:16]														WDTIMER_FLAG	WDTIMER_INT_EN
Type	R				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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Reset	0000				0	0	0	0	0	0	0	0	0	0	0	0

Set this register for PMIC Charger circuit configuration controls.

WDTIMER_CNT Counter value for chr_en watch-dog timer (high bit 19 ~ 16)

WDTIMER_FLAG Time-out flag for chr_en watch-dog timer

Read:

0 no time-out status

1 has time-out status

Write:

1 clear time-out status flag to 0

WDTIMER_INT_EN Interrupt enable setting for chr_en watch-dog timer.

0 disable

1 enable

0x8301_08F4 PMIC Charger Control Register 5 PMIC_CHR_CON5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDTIMER_CNT[15:0]															
Type	R															
Reset	00000000_00000000															

Set this register for PMIC Charger circuit configuration controls.

WDTIMER_CNT Counter value for chr_en watch-dog timer (low bit 15 ~ 0)

0x8301_0880 PMIC Driver Control Register 0 PMIC_DRIVER_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KPLED_STATUS	ISINK1_STATUS	ISINK2_STATUS	ISINK3_STATUS	ISINK4_STATUS				RG_KPLED_SEL			RG_KPLED_FORCE_OFF	KPLED_EN	RG_KPLED_TYPE	RG_ISINKS_FORCE_OFF	RG_ISINKS_EN
Type	R	R	R	R	R	R/W	R/W	R/W	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	000			0	0	0	0	0

Set this register for PMIC Start-up circuit configuration controls.

KPLED_STATUS KPLED on/off status

0 off

1 on

ISINK4_STATUS ISINK4 on/off status

0 off

1 on

ISINK3_STATUS ISINK3 on/off status

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0 off
1 on

ISINK2_STATUS ISINK2 on/off status
0 off
1 on

ISINK1_STATUS ISINK1 on/off status
0 off
1 on

RG_KPLED_SEL KPLED Number Select (00: 1 set, 011: 4 sets for WLED, 4 sets for RLED; 111: 4 sets for WLED, 8 sets for RLED).
000 1 sets for WLED, 1 sets for RLED
011 4 sets for WLED, 4 sets for RLED
111 4 sets for WLED, 8 sets for RLED

RG_KPLED_FORCE_OFF KPLED force off
0 normal
1 force off

KPLED_EN KPLED driver enable control signal
0 disable
1 enable
*** **KPLED** is controlled by **KPLED_EN** & **PWM2** output signal. About PWM control setting please reference "**Pulse-Width Modulation Outputs.doc**".

RG_KPLED_TYPE KPLED type select
0 WLED
1 RLED

RG_ISINKS_FORCE_OFF ISINK1~4 force off
0 normal
1 force off

RG_ISINKS_EN ISINK1~4 driver enable control signal
0 disable
1 enable

0x8301_0884 PMIC Driver Control Register 1 PMIC_DRIVER_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_ISINKS_CHSEL						RG_ISINKS_VR_SEL	RG_ISINKS_DIMM				
Type	R/W	R/W	R/W	R/W	R/W				R/W	R/W	R/W	R/W				
Reset	0	0	0	0	0000				0	0	0	00000				

Set this register for PMIC Driver circuit configuration controls.

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RG_ISINKS_CHSEL Select ISINK1~4 individually (normal or test)

- **0001** ISINK1 Turn ON
- **0010** ISINK2 Turn ON
- **0100** ISINK3 Turn ON
- **1000** ISINK4 Turn ON

RG_ISINKS_VR_SEL Reference select (???)

- **0** 0.4V
- **1** 0.6V

RG_ISINKS_DIMM Same 32 level dimming code for ISINK1~4 (normal or test)

- **00000** 1/32 x of target current level
- **00001** 2/32 x of target current level
- **00010** 3/32 x of target current level
- **00011** 4/32 x of target current level
- **....**
- **11110** 31/32 x of target current level
- **11111** 32/32 x of target current level

0x8301_0888 PMIC Driver Control Register 2 PMIC_DRIVER_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_ISINKS_VLED_STEP			RG_ISINKS_IRSET_CAL				
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W	R/W				
Reset	0	0	0	0	0	0	0	0	00		0	00000				

Set this register for PMIC Driver circuit configuration controls.

RG_ISINKS_VLED_STEP Coarse 4 step current level for ISINK1~4

- **00** 5.0mA
- **01** 10mA
- **10** 15mA
- **11** 20mA

RG_ISINKS_IRSET_CAL Fine tune current level for ISINK1~4

- **00000** 1+1/2
- **00001** 1+1/2+1/32
- **00010** 1+1/2+1/16
- **00011** 1+1/2+1/16+1/32
- **....**
- **10000** 1
- **10001** 1+1/32
- **10010** 1+1/16
- **10011** 1+1/16+1/32

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11110 1+1/4+1/8+1/16
11111 1+1/4+1/8+1/16+1/32

0x8301_088C PMIC Driver Control Register 3 PMIC_DRIVER_CON3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_BL_RSV			RG_BL_DIMM_DUTY					RG_BL_BGSEL			RG_BL_MODE	RG_BL_CALI_EN	RG_BL_VGEN_FORCEON	RG_VBOOST_EN	RG_BL_EN
Type	R/W			R/W					R/W			R/W	R/W	R/W	R/W	R/W
Reset	000			00000					000			0	0	0	0	0

Set this register for PMIC Driver circuit configuration controls.

RG_BL_RSV Reserved
RG_BL_DIMM_DUTY 32 Level Dimming Level
0000 Lowest BL reference voltage level.
1111 Highest BL reference voltage level.
RG_BL_BGSEL 8 evel BG Select
000 Lowest BL reference voltage level.
111 Highest BL reference voltage level.
RG_BL_MODE BL MODE, 0: APP1, 1: APP2
0 BL MODE1 => ISINK1~4 are used.
1 BL MODE2 => ISINK1~4 are not used but ISINK1 used as the sensing resistor feedback node.
RG_BL_CALI_EN Turn on BL Current Calibration (Application-II)
0 Dis-able BL Current Calibration.
1 Force the BL Current Calibration ON
RG_BL_VGEN_FORCEON Force Turn on VGEN in BL (Application-II)
0 Not need to force the VGEN ON.
1 Force the VGEN ON.
RG_VBOOST_EN Turn on BOOST1
0 Not need to turn on BOOST1 for BL application.
1 Turn on BOOST1 for BL application.
RG_BL_EN Turn on BL
0 Do not turn on BL
1 Turn on BL

0x8301_0890 PMIC Driver Control Register 4 PMIC_DRIVER_CON4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	VIBR_STATUS			RG_VIBR_OCFB_EN					RG_VIBR_CAL	RG_VIBR_SEL	RG_VIBR_EN_FORCE	VIBR_EN
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0000	00	0	0

Set this register for PMIC Driver circuit configuration controls.

VIBR_STATUS Vibr regulator on/off status

- **0** Vibr is off
- **1** Vibr is on

RG_VIBR_OCFB_EN Vibr regulator fold-back enable control signal

- **0** disable
- **1** enable

RG_VIBR_CAL Vibr regulator output voltage calibration (code in monotonic transfer function)

- **0** 0 mV
- **1** 20 mV
- **2** 40 mV
- **3** 60 mV
- **4** 80 mV
- **5** 100 mV
- **6** 120 mV
- **7** 140 mV
- **8** -160 mV
- **9** -140 mV
- **10** -120 mV
- **11** -100 mV
- **12** -80 mV
- **13** -60 mV
- **14** -40 mV
- **15** -20 mV

RG_VIBR_SEL Vibr regulator output voltage selection

- **0** VIBR=1.5V
- **1** VIBR=1.8V
- **2** VIBR=2.5V
- **3** VIBR=3.0V

RG_VIBR_EN_FORCE Vibr regulator force enable control signal

- **0** disable
- **1** enable

VIBR_EN Vibr regulador enable control signal

- **0** disable

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1 enable

*** **VIBR** is controlled by **VIBR_EN** & **PWM3** output signal. About PWM control setting, please reference "**Pulse-Width Modulation Outputs.doc**".

0x8301_08A0 PMIC Boost Control Register 0 PMICV_BOOST_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VBOOST_TRK_STATUS	VBOOST_STATUS			RG_VBOOST_CAL				RG_VBOOST_TUNE						RG_VBOOST_SS_SPEED	RG_VBOOST_SYNC_EN
Type	R/W	R/W	R/W	R/W	R/W				R/W				R/W	R/W	R/W	R/W
Reset	0	0	0	0	0000				0000				0	0	0	0

Set this register for PMIC Vboost circuit configuration controls.

VBOOST_STATUS Vboost regulator on/off status

0 Vboost is off

1 Vboost is on

VBOOST_TRK_STATUS Vboost regulator trk on/off status (???)

0 Not BATT HIGH

1 BATT HIGH Set!

RG_VBOOST_CAL Vboost output voltage calibration (5mV/step)

0000 -0mV

0001 -5mV

0010 -10mV

....

1000 +0mV

1001 +5mV

1010 +10mV

....

RG_VBOOST_TUNE Vboost output voltage tuning 3.2V~5.45V (0.15V/step)

0000 3.20V

0001 3.35V

0010 3.50V

....

1110 5.30V

1111 5.45V

RG_VBOOST_SS_SPEED Soft-start speed control

0 normal speed

1 2/3 speed

RG_VBOOST_SYNC_EN Enable internal sync. diode

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0 disable
1 enable

0x8301_08A4 PMIC Boost Control Register 1 PMIC_VBOOST_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_VBOOST_TRKOC_CAL				RG_VBOOST_DIO_SR_CON				RG_VBOOST_PRE_SR_CON				RG_VBOOST_ISNS_CAL		
Type	R/W	R/W			R/W	R/W			R/W	R/W			R/W	R/W		
Reset	0	000			0	000			0	000			0	000		

Set this register for PMIC Vboost circuit configuration controls.

RG_VBOOST_TRKOC_CAL BATTHIGH OC Trigger Level (Not Used)
0 Lowest BATTHIGH OC Level
...
7 Highest BATTHIGH OC Level

RG_VBOOST_DIO_SR_CON Pre-driver for PMOS slew-rate control
0 Default Value
1 add 3x Driving Force
2 add 6x Driving Force
3 add 9x Driving Force
4 add 6x Driving Force
5 add 15x Driving Force
6 add 15x Driving Force
7 add 18x Driving Force

RG_VBOOST_PRE_SR_CON Pre-driver slew-rate control
0 Default Value
1 add 2x Driving Force
2 add 4x Driving Force
3 add 6x Driving Force
4 add 8x Driving Force
5 add 10x Driving Force
6 add 12x Driving Force
7 add 14x Driving Force

RG_VBOOST_ISNS_CAL Over-current Threshould Control
0 Default Value
1 -5%
2 -10%
3 -15%
4 Default Value
5 +5%

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6 +10%
7 +15%

0x8301_08A8 PMIC Boost Control Register 2 PMIC_VBOOST_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VBOOST_RSV								RG_VBOOST_TEST_SEL				RG_VBOOST_TEST_EN		RG_VBOOST_DISCLK	RG_VBOOST_FORCEON_CLK
Type	R/W								R/W				R/W	R/W	R/W	R/W
Reset	00000000								0000				0	0	0	0

Set this register for PMIC Boost circuit configuration controls.

RG_VBOOST_RSV Reserved

RG_VBOOST_TEST_SEL Vboost test mode monitor select

00xx Select DO1 through the Test Mode MUX to be the DO
01xx Select DO2 through the Test Mode MUX to be the DO
10xx Select DO3 through the Test Mode MUX to be the DO
11xx Select DO4 through the Test Mode MUX to be the DO
xx00 Select AO1 through the Test Mode MUX to be the AO
xx01 Select AO2 through the Test Mode MUX to be the AO
xx10 Select AO3 through the Test Mode MUX to be the AO
xx11 Select AO4 through the Test Mode MUX to be the AO

RG_VBOOST_TEST_EN Vboost test mode enable

0 normal mode
1 test mode

RG_VBOOST_DISCLK Force the internal oscillator (@4.3V) off ➔ **Dominate! Only for debug mode.**

0 normal mode
1 force off

RG_VBOOST_FORCEON_CLK Froce the internal oscillator (@4.3V) on

0 normal mode
1 force on

0x8301_08AC PMIC Vboost Clock Setting Register PMIC_VBOOST_CKS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											VBOOST_CKS					
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					
Reset	0	0	0	0	0	0	0	0	0	0	000000					

Set this register for PMIC Vboost circuit clock setting controls.

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VBOOST_CKS The Vboost divided clock setting registers.

- **0** power-down
- **1~15** reserved.
- **16~36** CLKSQ_26_CK/(16~36)
- **37~63** reserved

0x8301_08B0 PMIC Class-D Control Register 0 PMIC_CLASSD_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SPK_RSV						RG_SPKAB_OBIAS		RG_SPKAB_DEPOP_EN	RG_SPKAB_OC_EN	RG_SPKAB_SENDED	RG_SPKAB_FLOAT	RG_SPKMODE	RG_SPK_EMODE	RG_SPK_RST	RG_SPK_EN
Type	R/W	R/W		R/W	R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	00		0	0	0	00		0	0	0	0	0	0	0	0

Set this register for PMIC Class-D circuit configuration controls.

RG_SPK_RSV[3] see RG_SPK_EMODE

RG_SPK_RSV[2:1] Class-D mode controller bias current select

- **0** x1
- **1** x1
- **2** X0.75
- **3** X0.5

RG_SPK_RSV[0] Class-D differential input test mode select

- **0** input from AU_MOUTR and HALFV
- **1** input from PAD_FMINR and PAD_FMINL

RG_SPKAB_OBIAS Class-AB mode output stage bias current select

- **0** 3.225mA
- **1** 6.381mA
- **2** 9.533mA
- **3** 12.684mA

RG_SPKAB_DEPOP_EN Class-AB mdoe anti-pop for buffer output enable (not used)

- **0** Reserved for Future Usage
- **1** Reserved for Future Usage

RG_SPKAB_OC_EN Class-AB mode over-current protection enable

- **0** disable over-current protection
- **1** enable over-current protection

RG_SPKAB_SENDED Class-AB mode single-ended buffer output (not used)

- **0** Reserved for Future Usage
- **1** Reserved for Future Usage

RG_SPKAB_FLOAT Class-AB mode output floating during power down (not used)

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0 Reserved for Future Usage
1 Reserved for Future Usage
RG_SPKMODE speaker driver mode select
0 Class-D mode
1 Class-AB mode
RG_SPK_EMODE Class-D output falling edge extended mode
{RG_SPK_RSV[3], RG_SPK_EMODE}
00 no extension
01 no extension
10 lead extension
11 lag extension
RG_SPK_RST Class D reset
0 normal mode
1 reset mode
RG_SPK_EN Class-D enable
0 disable
1 enable

0x8301_08B4 PMIC Class-D Control Register 1 PMIC_CLASSD_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPK_DTCP				SPK_DTCN				RG_SPK_DTIP				RG_SPK_DTIN			
Type	R				R				R/W				R/W			
Reset	0000				0000				0000				0000			

Set this register for PMIC Class-D circuit configuration controls.

SPK_DTCP Class-D DT Code for P switches (High Side)
0000 11.9ns (maximum dead time)
....
1111 2.654ns (minimum dead time)
SPK_DTCN Class-D DT Code for N switches (Low Side)
0000 11.9ns (maximum dead time)
....
1111 2.654ns (minimum dead time)
RG_SPK_DTIP Class-D PMOS dead time control code
0000 11.9ns (maximum dead time)
....
1111 2.654ns (minimum dead time)
RG_SPK_DTIN Class-D NMOS dead time control code
0000 11.9ns (maximum dead time)
....

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1111 2.654ns (minimum dead time)

0x8301_08B8 PMIC Class-D Control Register 2 PMIC_CLASSD_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_SPK_CCODE				RG_SPK_CMODE		RG_SPK_PMODE	RG_SPK_DTCAL	RG_SPK_PCHG		RG_SPK_DMODE	
Type	R/W	R/W	R/W	R/W	R/W				R/W		R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0000				00		0	0	00		00	

Set this register for PMIC Class-D circuit configuration controls.

RG_SPK_CCODE Class-D modulation frequency control code (1000: min freq; 0111 max freq)

0000 1.042MHz

…

…

1111 1.685MHz

RG_SPK_CMODE Class-D modulation frequency control mode

0X use SPKR_CCODE

10 use triangle wave for spread spectrum

11 use PRNG wave for spread spectrum

RG_SPK_PMODE Class-D PFD mode enable for reducing EMI

0 disable class D PFD mode

1 enable class D PFD mode

RG_SPK_DTCAL Class-D dead time calibration enable for auto mode

0 enable dead time calibration for auto mode

1 disable dead time calibration for auto mode

RG_SPK_PCHG Class-D PFD mode overlap time (10:min, 01:max)

00 103ns

01 55.67ns

10 39.09ns

11 30.47ns

RG_SPK_DMODE Class-D dead time control mode

00 FB:forced, use SPKR_DTIN, SPKR_DTIP

01 FB:auto, use SPKR_DTCN, SPKR_DTCP

10 FF:forced, use SPKR_DTIN, SPKR_DTIP

11 FF:auto, use SPKR_DTCN, SPKR_DTCP

0x8301_08BC PMIC Class-D Control Register 3 PMIC_CLASSD_CON3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name						RG_SPK_VOL			RG_SPK_OSCISEL	RG_SPK_OC_EN	RG_SPK_SLEW	RG_SPK_EN_VIEW_VREF	RG_SPK_EN_VIEW_CLK
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	000	0	0	0	0	00	0	0

Set this register for PMIC Class-D circuit configuration controls.

RG_SPK_VOL Class-D / Class-AB volume control (3dB/step)

	Class-D	**Class-AB**
000	6 dB	0 dB
001	9 dB	3 dB
010	12 dB	6 dB
011	15 dB	9 dB
100	18 dB	12 dB
101	21 dB	15 dB
110	24 dB	18 dB
111	27 dB	21 dB

RG_SPK_OSCISEL class D OSC frequency half

- **0** Fsw=Fnom
- **1** Fsw=0.5*Fnom

RG_SPK_OC_EN Claas-D over-current protection enable

- **0** enable
- **1** disable

RG_SPK_SLEW Class-D slew rate control

- **00** 2/4 (default)
- **01** 1/4
- **10** 4/4
- **11** 3/4

RG_SPK_EN_VIEW_VREF Mointor Class-D reference voltage enable

- **0** monitor integrator output common mode voltage
- **1** monitor SAW tooth Threshold voltage

RG_SPK_EN_VIEW_CLK Mointor Class-D clock enable

- **0** disable
- **1** enable

0x8301_08F8 PMIC Class-D Clock Setting Register PMIC_CLASSD_CKS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											CLASSD_CKS					
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					

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Reset	0	0	0	0	0	0	0	0	0	0	000000					

Set this register for PMIC Class-D circuit clock setting controls.

CLASSD_CKS The Class-D divided clock setting registers.

- **0** power-down
- **1~15** reserved.
- **16~36** CLKSQ_26_CK/(16~36)
- **37~63** reserved

0x8301_08C0 PMIC TEST Control Register 0 PMIC_TEST_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_INT_NODE_MUX		
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	000		

Set this register for PMIC TEST circuit configuration controls.

INT_NODE_MUX MUX the PMU internal nodes to be monitored by AUXADC. The function is reserved for the testing purpose.

- **0** GND (reserved)
- **1** GND (reserved)
- **2** GND (reserved)
- **3** VREG12D_DCV (DC-DC internal LDO voltage)
- **4** internal charger BGR voltage
- **5** ratioed Battery voltage
- **6** ratioed ISENSE voltage
- **7** ratioed CHRIN voltage

0x8301_08C4 PMIC TEST Control Register 1 PMIC_TEST_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_TPSEL_E				RG_TPSEL						RG_TP_BUCK		RG_TP_LED			
Type	R/W				R/W				R/W	R/W	R/W		R/W			
Reset	0000				0000				0	0	00		0000			

Set this register for PMIC TEST circuit configuration controls.

RG_TPSEL_E Need Special Care of setting!!

[3] Reserved for Future Usage (not used).

[2] = 0

[1:0] MUX three groups of four signals to the internal **test-ins**.

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00 Normal
01 BAT_ON → tsin4; GND → tsin3; PMU_RSTB → tsin2; GND → tsin1
10 CHRDET → tsin4; OVP → tsin3; CHRDET_DIS_LATCH → tsin2; UVLO → tsin1
11 NORMAL → tsin4; CV → tsin3; TEST_MODE_POR1 → tsin2; VMSEL_INT → tsin1

[2] = 1
VM_STATUS → tsin4; VRF_EN → tsin3; VTCXO_EN → tsin2; VA_EN → tsin1

RG_TPSEL Define Normal and other 7 test modes.

0000 NORMAL

[3] Once get into this "ANA_TESTMODE", **MUST** set RG_TPSEL=0!! AND **MUST** set SIM1/2 CLK/RST High impedance!!
0 output internal signal to outside
1 signal input from outside into IC (**NOT ALLOWED HERE!!**)

[2:0] Define normal and other 7 test modes
001 TestMode1: CHR signals are muxed to testpins
010 TestMode2: CHR signals are muxed to testpins
011 TestMode3: CHR signals are muxed to testpins
100 TestMode4: CHR signals are muxed to testpins
110 TestMode5: CHR signals are muxed to testpins
110 TestMode6: STARTUP signals are muxed to testpins
111 TestMode7: **test-ins** signals are muxed to testpins

RG_TP_BUCK Use to mux buck signals to outside through PAD_LED_R
00 Normal
01 vreg12d_vcore1 → OUT1_TST; AO_VCORE → AO_DCV; DO1_VCORE → DO1_DCV; DO2_VCORE → DO2_DCV; DO3_VCORE → DO3_DCV; DO4_VCORE → DO4_DCV; buck_en_vcore1 → BUCK_EN_DCV; GND → buck_rsv_dcv.
10 VR600 → OUT1_TST; AO_VBOOST → AO_DCV; DO1_VBOOST → DO1_DCV; DO2_VBOOST → DO2_DCV; DO3_VBOOST → DO3_DCV; DO4_VBOOST → DO4_DCV; VBOOST_STATUS → BUCK_EN_DCV; GND → buck_rsv_dcv.
11 GND → OUT1_TST; GND → AO_DCV; SPKP_OCP → DO1_DCV; SPKP_OCN → DO2_DCV; SPKM_OCP → DO3_DCV; SPKM_OCN → DO4_DCV; RG_SPK_EN → BUCK_EN_DCV; GND → buck_rsv_dcv.

RG_TP_LED Use to mux internal (shown above) DCV-signals to PAD_LED_R. The KP_LED **MUST** be Shutdown!!
0 Normal
1 G_REF goes to PAD_LED_R
…
14 PMU_RSTB_INT goes to PAD_LED_R
15 (Special) PAD_LED_R input a DC voltage to be the internal THR_VTH_EXT signal.

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0x8301_08C8 PMIC TEST Control Register 2 PMIC_TEST_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_TESTMODE_RSV								RG_ISENSE_OUT_EN	RG_VBAT_OUT_EN	RG_PMU_TMR_EN	RG_PMU_TMSEL				
Type	R/W								R/W	R/W	R/W	R/W				
Reset	00000000								0	0	0	00000				

Set this register for PMIC TEST circuit configuration controls.

RG_TESTMODE_RSV Reserved

RG_ISENSE_OUT_EN Pass ISENSE voltage to one of the AUXADC channel

- **0** disable
- **1** enable

RG_VBAT_OUT_EN Pass Battery voltage to one of the AUXADC channel

- **0** disable
- **1** enable

RG_PMU_TMR_EN Voltage divide-by-2 enable signal between PMU and AUXADC

- **0** Not divide-by-2
- **1** Divide-by-2 enabled!

RG_PMU_TMSEL PMU internal signal selection control; send to AUXADC

- **00000** The 1st MUX control bit
- ....
- **11111** The 32th MUX control bit

0x8301_08D0 PMIC Over-Current Control Register 0 PMIC_OC_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VA_OC_INT_EN	VA_OC_AUTO_OFF	VA_OC_GEAR		VM_OC_INT_EN	VM_OC_AUTO_OFF	VM_OC_GEAR		VIO_OC_INT_EN	VIO_OC_AUTO_OFF	VIO_OC_GEAR		VRF_OC_INT_EN	VRF_OC_AUTO_OFF	VRF_OC_GEAR	
Type	R/W	R/W	R/W		R/W	R/W	R/W		R/W	R/W	R/W		R/W	R/W	R/W	
Reset	0	0	00		0	0	00		0	0	00		0	0	00	

Set this register for PMIC Over-Current circuit configuration controls.

VA_OC_INT_EN Enable bit of Va over-current interrupt if the VA_OC_FLAG been asserted.

- **0** disable
- **1** enable

VA_OC_AUTO_OFF Enable to power-off the Va automatically if the VA_OC_FLAG been asserted.

- **0** disable
- **1** enable

VA_OC_GEAR The deglitch time constant for Va over-current status from PMIC to generate VA_OC_FLAG.

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00 100 uS
01 200 uS
10 400 uS
11 800 uS

VM_OC_INT_EN Enable bit of Vm over-current interrupt if the VM_OC_FLAG been asserted.
0 disable
1 enable

VM_OC_AUTO_OFF Enable to power-off the Vm automatically if the VM_OC_FLAG been asserted.
0 disable
1 enable

VM_OC_GEAR The deglitch time constant for Vm over-current status from PMIC to generate VM_OC_FLAG.
00 100 uS
01 200 uS
10 400 uS
11 800 uS

VIO_OC_INT_EN Enable bit of Vio over-current interrupt if the VIO_OC_FLAG been asserted.
0 disable
1 enable

VIO_OC_AUTO_OFF Enable to power-off the Vio automatically if the VIO_OC_FLAG been asserted.
0 disable
1 enable

VIO_OC_GEAR The deglitch time constant for Vio over-current status from PMIC to generate VIO_OC_FLAG.
00 100 uS
01 200 uS
10 400 uS
11 800 uS

VRF_OC_INT_EN Enable bit of Vrf over-current interrupt if the VRF_OC_FLAG been asserted.
0 disable
1 enable

VRF_OC_AUTO_OFF Enable to power-off the Vrf automatically if the VRF_OC_FLAG been asserted.
0 disable
1 enable

VRF_OC_GEAR The deglitch time constant for Vrf over-current status from PMIC to generate VRF_OC_FLAG.
00 100 uS
01 200 uS
10 400 uS
11 800 uS

0x8301_08D4 PMIC Over-Current Control Register 1 PMIC_OC_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	VTCXO_OC_INT_EN	VTCXO_OC_AUTO_OFF	VTCXO_OC_GEAR													
Type	R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	00		0	0	0	0	0	0	0	0	0	0	0	0

Set this register for PMIC Over-Current circuit configuration controls.

VTCXO_OC_INT_EN Enable bit of Vtcxo over-current interrupt if the VTCXO_OC_FLAG been asserted.

- **0** disable
- **1** enable

VTCXO_OC_AUTO_OFF Enable to power-off the Vtcxo automatically if the VTCXO_OC_FLAG been asserted.

- **0** disable
- **1** enable

VTCXO_OC_GEAR The deglitch time constant for Vtcxo over-current status from PMIC to generate VTCXO_OC_FLAG.

- **00** 100 uS
- **01** 200 uS
- **10** 400 uS
- **11** 800 uS

0x8301_08D8 PMIC Over-Current Control Register 2 PMIC_OC_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VCAMA_OC_INT_EN	VCAMA_OC_AUTO_OFF	VCAMA_OC_GEAR		VCAMD_OC_INT_EN	VCAMD_OC_AUTO_OFF	VCAMD_OC_GEAR		VUSB_OC_INT_EN	VUSB_OC_AUTO_OFF	VUSB_OC_GEAR		VBT_OC_INT_EN	VBT_OC_AUTO_OFF	VBT_OC_GEAR	
Type	R/W	R/W	R/W		R/W	R/W	R/W		R/W	R/W	R/W		R/W	R/W	R/W	
Reset	0	0	00		0	0	00		0	0	00		0	0	00	

Set this register for PMIC Over-Current circuit configuration controls.

VCAMA_OC_INT_EN Enable bit of Vcama over-current interrupt if the VCAMA_OC_FLAG been asserted.

- **0** disable
- **1** enable

VCAMA_OC_AUTO_OFF Enable to power-off the Vcama automatically if the VCAMA_OC_FLAG been asserted.

- **0** disable
- **1** enable

VCAMA_OC_GEAR The deglitch time constant for Vcama over-current status from PMIC to generate VCAMA_OC_FLAG.

- **00** 100 uS
- **01** 200 uS
- **10** 400 uS

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11 800 uS

VCAMD_OC_INT_EN Enable bit of Vcamd over-current interrupt if the VCAMD_OC_FLAG been asserted.

0 disable

1 enable

VCAMD_OC_AUTO_OFF Enable to power-off the Vcamd automatically if the VCAMD_OC_FLAG been asserted.

0 disable

1 enable

VCAMD_OC_GEAR The deglitch time constant for Vcamd over-current status from PMIC to generate VCAMD_OC_FLAG.

00 100 uS

01 200 uS

10 400 uS

11 800 uS

VUSB_OC_INT_EN Enable bit of Vusb over-current interrupt if the VUSB_OC_FLAG been asserted.

0 disable

1 enable

VUSB_OC_AUTO_OFF Enable to power-off the Vusb automatically if the VUSB_OC_FLAG been asserted.

0 disable

1 enable

VUSB_OC_GEAR The deglitch time constant for Vusb over-current status from PMIC to generate VUSB_OC_FLAG.

00 100 uS

01 200 uS

10 400 uS

11 800 uS

VBT_OC_INT_EN Enable bit of Vbt over-current interrupt if the VBT_OC_FLAG been asserted.

0 disable

1 enable

VBT_OC_AUTO_OFF Enable to power-off the Vbt automatically if the VBT_OC_FLAG been asserted.

0 disable

1 enable

VBT_OC_GEAR The deglitch time constant for Vbt over-current status from PMIC to generate VBT_OC_FLAG.

00 100 uS

01 200 uS

10 400 uS

11 800 uS

0x8301_08DC PMIC Over-Current Control Register 3 PMIC_OC_CON3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	VSIM_OC_INT_EN	VSIM_OC_AUTO_OFF	VSIM_OC_GEAR	VBOOST_OC_INT_EN	VBOOST_OC_AUTO_OFF	VBOOST_OC_GEAR	VIBR_OC_INT_EN	VIBR_OC_AUTO_OFF	VIBR_OC_GEAR	SPK_OC_INT_EN	SPK_OC_AUTO_OFF	SPK_OC_GEAR
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	00	0	0	00	0	0	00	0	0	00

Set this register for PMIC Over-Current circuit configuration controls.

VSIM_OC_INT_EN Enable bit of Vsim over-current interrupt if the VSIM_OC_FLAG been asserted.
- **0** disable
- **1** enable

VSIM_OC_AUTO_OFF Enable to power-off the Vsim automatically if the VSIM_OC_FLAG been asserted.
- **0** disable
- **1** enable

VSIM_OC_GEAR The deglitch time constant for Vsim over-current status from PMIC to generate VSIM_OC_FLAG.
- **00** 100 uS
- **01** 200 uS
- **10** 400 uS
- **11** 800 uS

VBOOST_OC_INT_EN Enable bit of Vboost over-current interrupt if the VBOOST_OC_FLAG been asserted.
- **0** disable
- **1** enable

VBOOST_OC_AUTO_OFF Enable to power-off the Vboost automatically if the VBOOST_OC_FLAG been asserted.
- **0** disable
- **1** enable

VBOOST_OC_GEAR The deglitch time constant for Vboost over-current status from PMIC to generate VBOOST_OC_FLAG.
- **00** 100 uS
- **01** 200 uS
- **10** 400 uS
- **11** 800 uS

VIBR_OC_INT_EN Enable bit of VIBR over-current interrupt if the VIBR_OC_FLAG been asserted.
- **0** disable
- **1** enable

VIBR_OC_AUTO_OFF Enable to power-off the VIBR automatically if the VIBR_OC_FLAG been asserted.
- **0** disable
- **1** enable

VIBR_OC_GEAR The deglitch time constant for VIBR over-current status from PMIC to generate VIBR_OC_FLAG.
- **00** 100 uS
- **01** 200 uS
- **10** 400 uS

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11 800 uS

SPK_OC_INT_EN Enable bit of SPK over-current interrupt if the SPK_OC_FLAG been asserted.

0 disable

1 enable

SPK_OC_AUTO_OFF Enable to power-off the SPK automatically if the SPK_OC_FLAG been asserted.

0 disable

1 enable

SPK_OC_GEAR The deglitch time constant for SPK over-current status from PMIC to generate SPK_OC_FLAG.

00 100 uS

01 200 uS

10 400 uS

11 800 uS

0x8301_08E0 PMIC Over-Current Control Register 4 PMIC_OC_CON4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VCAMA_STBTD		VCAMD_STBTD		VUSB_STBTD		VBT_STBTD		VSIM_STBTD		VIBR_STBTD	
Type	R/W	R/W	R/W	R/W	R/W		R/W		R/W		R/W		R/W		R/W	
Reset	0	0	0	0	00		00		00		00		00		00	

Set this register for PMIC Over-Current circuit configuration controls.

VCAMA_STBTD The delay time constant for Vcama soft start

00 200 uS

01 400 uS

10 600 uS

11 800 uS

VCAMD_STBTD The delay time constant for Vcamd soft start

00 200 uS

01 400 uS

10 600 uS

11 800 uS

VUSB_STBTD The delay time constant for Vusb soft start

00 200 uS

01 400 uS

10 600 uS

11 800 uS

VBT_STBTD The delay time constant for Vbt soft start

00 200 uS

01 400 uS

10 600 uS

11 800 uS

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VSIM_STBTD The delay time constant for Vsim soft start

- **00** 200 uS
- **01** 400 uS
- **10** 600 uS
- **11** 800 uS

VIBR_STBTD The delay time constant for VIBR soft start

- **00** 200 uS
- **01** 400 uS
- **10** 600 uS
- **11** 800 uS

0x8301_08E4 PMIC Over-Current Control Register 5 PMIC_OC_CON5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VA_OC_FLAG	VM_OC_FLAG	VIO_OC_FLAG	VRF_OC_FLAG	VTCXO_OC_FLAG				VCAMA_OC_FLAG	VCAMD_OC_FLAG	VUSB_OC_FLAG	VBT_OC_FLAG	VSIM_OC_FLAG	VBOOST_OC_FLAG	VIBR_OC_FLAG	SPK_OC_FLAG
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Set this register for PMIC Over-Current circuit configuration controls.

VA_OC_FLAG The flag informs some Va over current status have been asserted.

Read:

- **0** no over status
- **1** some over status

Write:

- **1** clear over status flag to 0

VM_OC_FLAG The flag informs some Vm over current status have been asserted.

Read:

- **0** no over status
- **1** some over status

Write:

- **1** clear over status flag to 0

VIO_OC_FLAG The flag informs some Vio over current status have been asserted.

Read:

- **0** no over status
- **1** some over status

Write:

- **1** clear over status flag to 0

VRF_OC_FLAG The flag informs some Vrf over current status have been asserted.

Read:

- **0** no over status

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1 some over status

Write:

1 clear over status flag to 0

VTCXO_OC_FLAG The flag informs some Vtcxo over current status have been asserted.

Read:

0 no over status

1 some over status

Write:

1 clear over status flag to 0

VCAMA_OC_FLAG The flag informs some Vcama over current status have been asserted.

Read:

0 no over status

1 some over status

Write:

1 clear over status flag to 0

VCAMD_OC_FLAG The flag informs some VCAMD over current status have been asserted.

Read:

0 no over status

1 some over status

Write:

1 clear over status flag to 0

VUSB_OC_FLAG The flag informs some Vusb over current status have been asserted.

Read:

0 no over status

1 some over status

Write:

1 clear over status flag to 0

VBT_OC_FLAG The flag informs some Vbt over current status have been asserted.

Read:

0 no over status

1 some over status

Write:

1 clear over status flag to 0

VSIM_OC_FLAG The flag informs some Vsim over current status have been asserted.

Read:

0 no over status

1 some over status

Write:

1 clear over status flag to 0

VBOOST_OC_FLAG The flag informs some Vboost over current status have been asserted.

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Read:

0 no over status

1 some over status

Write:

1 clear over status flag to 0

VIBR_OC_FLAG The flag informs some VIBR over current status have been asserted.

Read:

0 no over status

1 some over status

Write:

1 clear over status flag to 0

SPK_OC_FLAG The flag informs some SPK over current status have been asserted.

Read:

0 no over status

1 some over status

Write:

1 clear over status flag to 0

0x8301_08E8 PMIC Over-Current Control Register 6 PMIC_OC_CON6

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SPK_OC_WND		SPK_OC_TRG	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	00		00	

Set this register for PMIC Over-Current circuit configuration controls.

SPK_OC_WND Decision window setting for SPK over current status.

00 16uS

01 32uS

10 64uS

11 128uS

SPK_OC_TRG Threshold setting in the decision window for SPK over current status.

00 1/2

01 1/4

10 1/8

11 1/16

0x8301_08EC PMIC Over-Current Control Register 7 PMIC_OC_CON7

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VA_OC_STATUS	VM_OC_STATUS	VIO_OC_STATUS	VRF_OC_STATUS	VTCXO_OC_STATUS				VCAMA_OC_STATUS	VCAMD_OC_STATUS	VUSB_OC_STATUS	VBT_OC_STATUS	VSIM_OC_STATUS	VBOOST_OC_STATUS	VIBR_OC_STATUS	SPK_OC_STATUS

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Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Set this register for PMIC Over-Current circuit configuration controls.

VA_OC_STATUS The status informs some Va over current status have been asserted.
- **0** no over status
- **1** some over status

VM_OC_STATUS The status informs some Vm over current status have been asserted.
- **0** no over status
- **1** some over status

VIO_OC_STATUS The status informs some Vio over current status have been asserted.
- **0** no over status
- **1** some over status

VRF_OC_STATUS The status informs some Vrf over current status have been asserted.
- **0** no over status
- **1** some over status

VTCXO_OC_STAUS The status informs some Vtcxo over current status have been asserted.
- **0** no over status
- **1** some over status

VCAMA_OC_STATUS The status informs some Vcama over current status have been asserted.
- **0** no over status
- **1** some over status

VCAMD_OC_STATUS The status informs some VCAMD over current status have been asserted.
- **0** no over status
- **1** some over status

VUSB_OC_STATUS The status informs some Vusb over current status have been asserted.
- **0** no over status
- **1** some over status

VBT_OC_STATUS The status informs some Vbt over current status have been asserted.
- **0** no over status
- **1** some over status

VSIM_OC_STATUS The status informs some Vsim over current status have been asserted.
- **0** no over status
- **1** some over status

VBOOST_OC_STATUS The status informs some Vboost over current status have been asserted.
- **0** no over status
- **1** some over status

VIBR_OC_STATUS The status informs some VIBR over current status have been asserted.
- **0** no over status
- **1** some over status

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SPK_OC_STATUS The status informs some SPK over current status have been asserted.
- **0** no over status
- **1** some over status

0x8301_0A00 ABIST Frequency-Meter Control Register 0 ABIST_FMTR_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FQMTR_EN	FQMTR_RST					FQMTR_WINSET									
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W									
Reset	0	0	0	0	0	0	0000000000									

Set this register for ABIST Frequency-Meter circuit configuration controls.

FQMTR_EN ABIST frequency-meter enable control signal
- **0** disable
- **1** enable

FQMTR_RST ABIST frequency-meter reset control signal
- **0** normal operation
- **1** reset

FQMTR_WINSET ABIST frequency-meter measurement window setting (= numbers of FIXED clock cycles)

0x8301_0A04 ABIST Frequency-Meter Control Register 1 ABIST_FMTR_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												FQMTR_FCKSEL	FQMTR_TCKSEL			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0000			

Set this register for ABIST Frequency-Meter circuit configuration controls.

FQMTR_FCKSEL ABIST frequency-meter FIXED clock selection
- **0** CLKSQ 26MHz clock
- **1** TEST clock from PAD_JTCK

FQMTR_TCKSEL ABIST frequency-meter TESTED clock selection
- **0** idle
- **1** CLKSQ 26MHz clock
- **2** MPLL 104~113MHz clock
- **3** UPLL 104MHz clock
- **4** USB PHY 30MHz clock
- **5** PMU test clock 0
- **6** PMU test clock 1

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7 RTC XOSC 32KHz clock
8~15 Reserved

0x8301_0A08 ABIST Frequency-Meter Data Register ABIST_FMTR_DATA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FQMTR_BUSY				FQMTR_DATA											
Type	R	R/W	R/W	R/W	R											
Reset	0	0	0	0	0000_0000_0000											

Set this register for ABIST Frequency-Meter Data registers.

FQMTR_BUSY ABIST frequency-meter busy status
0 FQMTR is ready
1 FQMTR is busy

FQMTR_DATA ABIST frequency-meter measurement data
****** Frequency(TESTED clock) = Frequency(FIXED clock) * FQMTR_DATA[11:0]/FQMTR_WINSET[9:0]**

0x8301_0A0C ABIST Monitor Control Register 0 ABIST_MON_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ABIST_FINISH	ABIST_PASS							ABIST_MON_CFG			ABIST_MON_SEL				
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	11111				

Set this register for ABIST Monitor circuit configuration controls.

ABIST_FINISH MCU writes to indicate ATE that test program is finished.
0 test is going
1 test is finished

ABIST_PASS MCU writes to indicate ATE that test program is pass or fail (ATE would check it at ABIST_FINISH == 1)
0 test is fail
1 test is pass

ABIST_MON_CFG ABIST monitor flags output mode select
0 monitor signals output mode
1 MCU program debug mode (output ABIST_MON_OUT[7:0])

ABIST_MON_SEL ABIST monitor flags output select

	MON[7] (LPA0)	MON[6] (LRSTB)	MON[5] (BPI_BUS5)	MON[4] (BPI_BUS4)	MON[3] (BPI_BUS3)	MON[2] (BPI_BUS2)	MON[1] (BPI_BUS1)	MON[0] (BPI_BUS0)

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0	0	VSDM_CK	VRXPH1_6P5M_CK	VRXPH2_6P5M_CK	VRXSIN	VRXZIN	VTXSOUT	VTXZOUT
1	0	0	0	0	0	ASDM_CK	AYDL[8]	AYDR[8]
2	AYDL[7]	AYDL[6]	AYDL[5]	AYDL[4]	AYDL[3]	AYDL[2]	AYDL[1]	AYDL[0]
3	AYDR[7]	AYDR[6]	AYDR[5]	AYDR[4]	AYDR[3]	AYDR[2]	AYDR[1]	AYDR[0]
4	0	0	EDGERFRX_PWDB	ESDM_CK	EDGERFRX_BNI	EDGERFRX_BPI	EDGERFRX_BNQ	EDGERFRX_BPQ
5	0	0	GTX_PWDB	GTX_SCLK	GTX_DDI[9]	GTX_DDI[8]	GTX_DDQ[9]	GTX_DDQ[8]
6	GTX_DDI[7]	GTX_DDI[6]	GTX_DDI[5]	GTX_DDI[4]	GTX_DDI[3]	GTX_DDI[2]	GTX_DDI[1]	GTX_DDI[0]
7	GTX_DDQ[7]	GTX_DDQ[6]	GTX_DDQ[5]	GTX_DDQ[4]	GTX_DDQ[3]	GTX_DDQ[2]	GTX_DDQ[1]	GTX_DDQ[0]
8	0	0	0	0	0	GSMBBTX_SWITCH_INPUT	GSMBBTX_COMPI	GSMBBTX_COMPQ
9	0	0	0	0	APC_PWDB	APC_TG	APC_BUS[9]	APC_BUS[8]
10	APC_BUS[7]	APC_BUS[6]	APC_BUS[5]	APC_BUS[4]	APC_BUS[3]	APC_BUS[2]	APC_BUS[1]	APC_BUS[0]
11	AUX_ST	AUX_CS_B	AUX_DIN	AUX_TPD_LATCH	AUX_SEL[3]	AUX_SEL[2]	AUX_SEL[1]	AUX_SEL[0]
12	0	0	AUX_PWDB	AUX_SCLK	AUX_COMP	AUX_PENIRQ	AUX_SFSO	AUX_SDO
13	MTV_EN	VSIM_EN	VSIM_SEL	SIMRST	SIMCLK	SIMDATA_OE	SIMDATA_IN	SIMDATA_OUT
14	MTV_EN	VSIM2_EN	VSIM2_SEL	SIM2RST	SIM2CLK	SIM2DATA_OE	SIM2DATA_IN	SIM2DATA_OUT
15	0	VCORE_STATUS	VRTC_STATUS	VA_STATUS	VM_STATUS	VIO_STATUS	VRF_STATUS	VTCXO_STATUS
16	0	0	VCAMA_STATUS	VCAMD_STATUS	VUSB_STATUS	VBT_STATUS	VSIM_STATUS	VSIM2_STATUS
17	FREQ_COUNT_PMU0	FREQ_COUNT_PMU1	0	VA_OC_STATUS	VM_OC_STATUS	VIO_OC_STATUS	VRF_OC_STATUS	VTCXO_OC_STATUS
18	VCAMA_OC_STATUS	VCAMD_OC_STATUS	VUSB_OC_STATUS	VBT_OC_STATUS	VSIM_OC_STATUS	VBOOST_OC_STATUS	VIBR_OC_STATUS	SPK_OC_DET
19	C2A_INTERNAL_PWM	C2A_INTERNAL_PWM2	PMU_OC_INT	VA_OC_INT	VM_OC_INT	VIO_OC_INT	VRF_OC_INT	VTCXO_OC_INT
20	VCAMA_OC_INT	VCAMD_OC_INT	VUSB_OC_INT	VBT_OC_INT	VSIM_OC_INT	VBOOST_OC_INT	VIBR_OC_INT	SPK_OC_INT
21	PWRKEY_VCORE	PWRKEY_DEB	TEST_MODE_POR	OVP	CHRDET	BAT_ON	CV	BAT_BATT
22	VBOOST_STATUS	VBOOST_TRK_STATUS	KPLED_STATUS	VIBR_STATUS	ISINK1_STATUS	ISINK2_STATUS	ISINK3_STATUS	ISINK4_STATUS
23	SPK_OC_DET	SPK_OC_CNTDET	VCAMA_STB	VCAMD_STB	VUSB_STB	VBT_STB	VSIM_STB	VIBR_STB
24	0	CLKSQ_26M_CK	USB_CLK_INT	FMCU_CK	FDSP_CK	FUSB_CK	FGSM_CK	F48M_CK
25	0	0	0	0	0	FMCU_CK	MPLL_FHPRD	MPLL_CLKSWPRD
26	F32K_CK	0	0	0	0	FQMTR_BUSY	FQMTR_CK	CLK26M_CK

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27	VCORE_VFB ADJ[3]	VCORE_VFB ADJ[2]	VCORE_VFB ADJ[1]	VCORE_VFB ADJ[0]	CLKSQ_CKSE L	KPLED_EN	VIBR_EN	SRCLKEN_V CORE
28	0	SRCLKEN_V TCXO	VUPG[5]	VUPG[4]	VUPG[3]	VUPG[2]	VUPG[1]	VUPG[0]
29	VRF_EN	VTCXO_EN	VCAMA_EN	VCAMD_EN	VUSB_EN	VBT_EN	VBOOST_EN	SPK_EN
30	MPLL_FBDIV [7]	MPLL_FBDIV [6]	MPLL_FBDIV [5]	MPLL_FBDIV [4]	MPLL_FBDIV [3]	MPLL_FBDIV [2]	MPLL_FBDIV [1]	MPLL_FBDIV [0]
31	CHR_EN	CALRC[2]	CALRC[1]	CALRC[0]	BIAS_PWDB	COMP_PWDB	DAC_PWDB	FILTER_PWD B

0x8301_0A10 ABIST Monitor Control Register 1 ABIST_MON_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ABIST_MON_OUT							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W							
Reset	0	0	0	0	0	0	0	0	00000000							

Set this register for ABIST Monitor circuit configuration controls.

ABIST_MON_OUT ABIST monitor debug output

0x8301_0A18 ABIST APC-DAC Control Register ABIST_APC_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ABIST_APC_SETEN					ABIST_APC_SETTG	ABIST_APC_SETBUS									
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W									
Reset	0	0	0	0	0	0	0000000000									

Set this register for ABIST APC-DAC circuit configuration controls.

ABIST_APC_SETEN ABIST APC-DAC manual setting mode

- **0** normal mode
- **1** manual setting mode

ABIST_APC_SETTG ABIST APC-DAC manual setting for APC_TG

ABIST_APC_SETBUS ABIST APC-DAC manual setting for APC_BUS

12.4 Programming Guide

12.4.1 BBRX Register Setup

The register used to control analog base-band receiver is ACIF_BBRX_CON.

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12.4.2 Programmable Biasing Current

To maximize the yield in modern digital process, the receiver features providing 5-bit 32-level programmable current to bias internal analog blocks. The 5-bits registers CALBIAS[4:0] is coded with 2's complement format.

12.4.2.1 Offset / Gain Calibration

The base-band downlink receiver (RX), together with the base-band uplink transmitter (TX) introduced in the next section, provides necessary analog hardware for DSP algorithm to correct the mismatch and offset error. The connection for measurement of both RX/TX mismatch and gain error is shown in **Figure 110**, and the corresponding calibration procedure is described below.

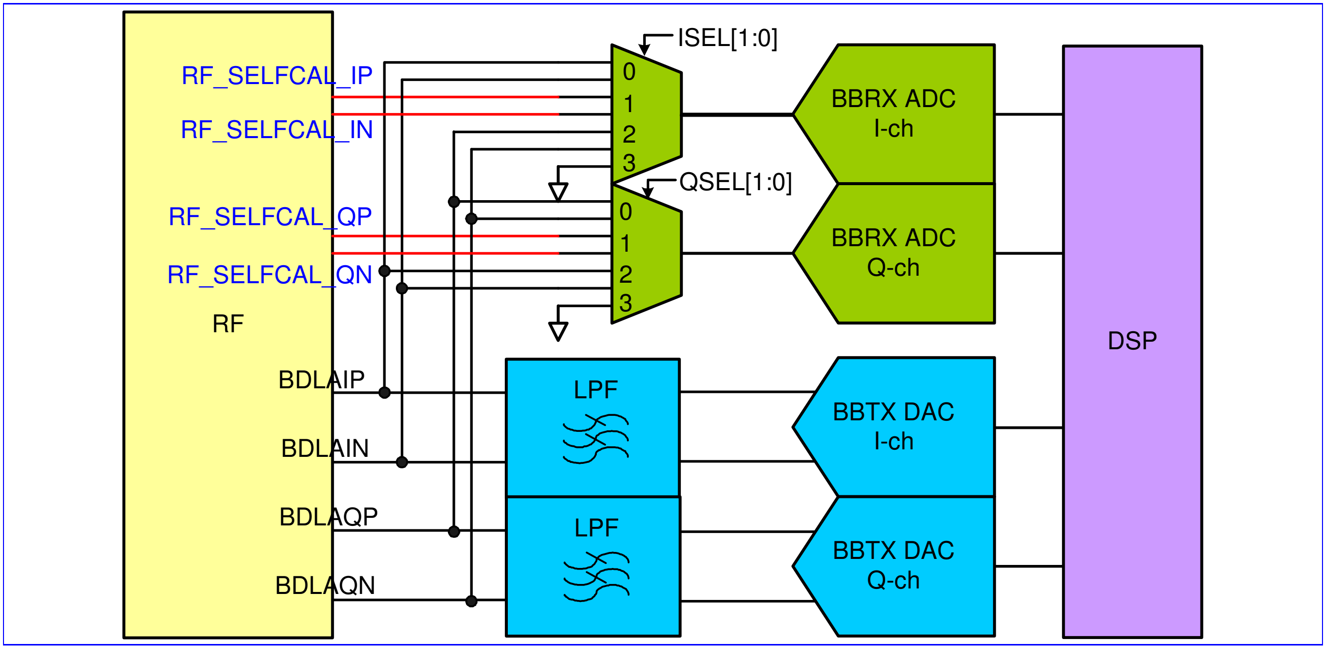

Figure 110 Base-band A/D and D/A Offset and Gain Calibration

12.4.2.2 Downlink RX Offset Error Calibration

The RX offset measurement is achieved by selecting grounded input to A/D converter (set ISEL [1:0] ='11' and QSEL [1:0] ='11' to select channel 3 of the analog input multiplexer, as shown in **Figure 111**. The output of the ADC is sent to DSP for further offset cancellation. The offset cancellation accuracy depends on the number of samples being converted. That is, more accurate measurement can be obtained by collecting more samples followed by averaging algorithm.

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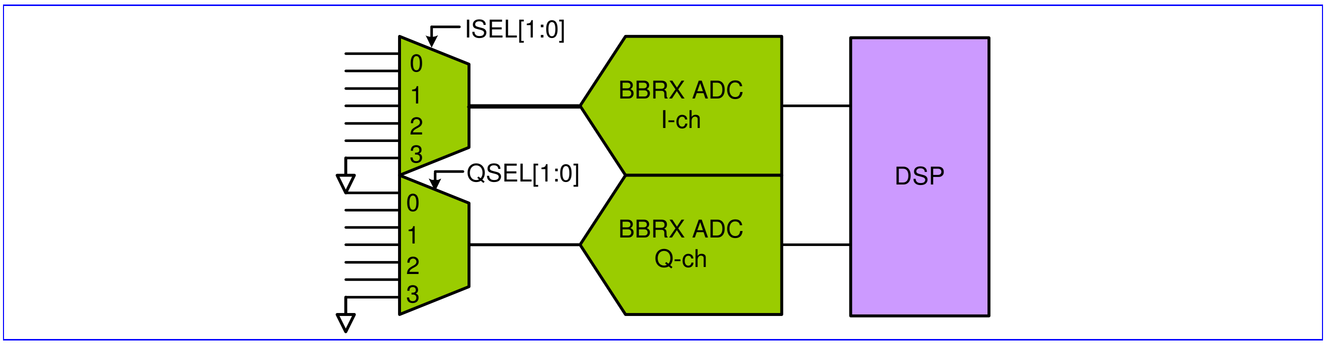

Figure 111 Downlink ADC Offset Error Measurement

12.4.2.3 Downlink RX and Uplink TX Gain Error Calibration

To measure the gain mismatch error, both I/Q uplink TXs should be programmed to produce full-scale pure sinusoidal waves output. Such signals are then fed to downlink RX for A/D conversion, in the following two steps.

A. The uplink I-channel output are connected to the downlink I-channel input, and the uplink Q-channel output are connected to the downlink Q-channel input. This can be achieved by setting ISEL [1:0] ='00' and QSEL [1:0] ='00' (shown in **Figure 112** (A))..

B. The uplink I-channel output are then connected to the downlink Q-channel input, and the uplink Q-channel output are connected to the downlink I-channel input. This can be achieved by setting ISEL [1:0] ='10' and QSEL [1:0] ='10' (shown in **Figure 112** (B)).

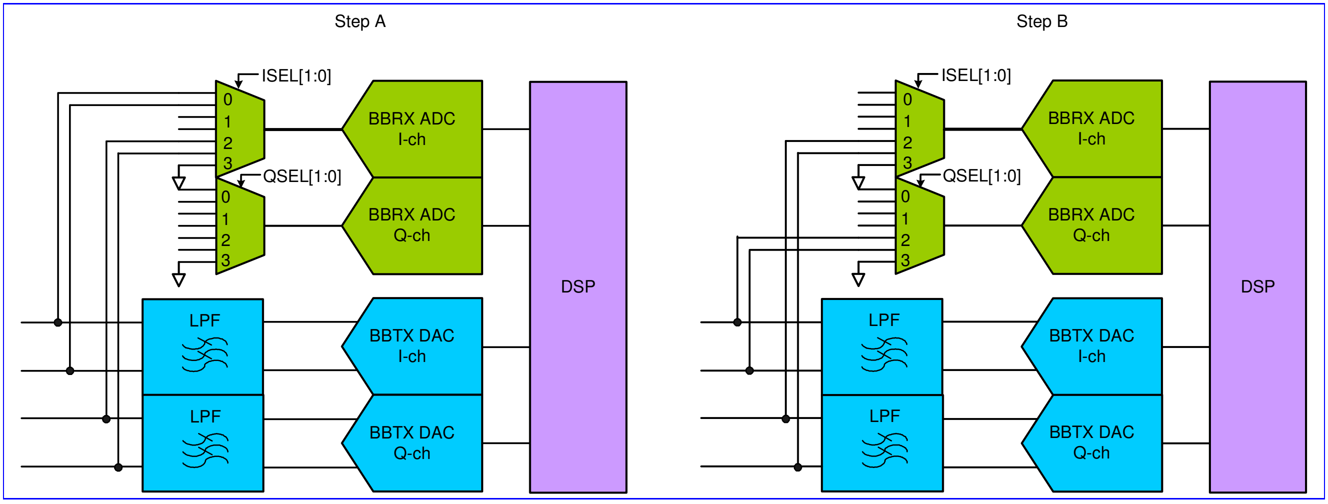

Figure 112 Downlink RX and Up-link TX Gain Mismatch Measurement (A) I/Q TX connect to I/Q RX (B) I/Q TX connect to Q/I RX

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Once above successive procedures are completed, RX/TX gain mismatch could be easily obtained because the amplitude mismatch on RX digitized result in step A and B is the sum and difference of RX and TX gain mismatch, respectively.

The gain error of the downlink RX can be corrected in the DSP section and the uplink TX gain error can be corrected by the gain trimming facility that TX block provide.

12.4.2.4 Uplink TX Offset Error Calibration

Once the offset of the downlink RX is known and corrected, the offset of the uplink TX alone could be easily estimated. The offset error of TX should be corrected in the digital domain by means of the programmable feature of the digital GMSK modulator.

Finally, it is important that above three calibration procedures should be exercised in order, that is, correct the RX offset first, then RX/TX gain mismatch, and finally TX offset. This is owing to that analog gain calibration in TX will affect its offset, while the digital offset correction has no effect on gain.

12.4.2.5 RF TX path DC Calibration

This can be achieved by setting ISEL [1:0] =’01’ and QSEL [1:0] =’01’. Please check RF part for the details setting.

12.4.3 BBTX Register Setup

The register used to control analog base-band transmitter is ACIF_BBTX_CON0 and ACIF_BBTX_CON1.

12.4.3.1 Output Gain Control

The output swing of the uplink transmitter is controlled by register GAIN[2:0] coded in 2’s complement with about 0.6 dB per step. When TRIMI[3:0] / TRIMQ[3:0] = 0 the swing is listed in **Table 87**, defined to be the difference between positive and negative output signal.

GAIN[2:0]	Output Swing	For AVDD=2.8 (V)
+3 (011)	AVDD*0.453 (+2.0 dB)	1.27
+2 (010)	AVDD*0.418 (+1.3 dB)	1.17
+1 (001)	AVDD*0.386 (+0.6 dB)	1.08
+0 (000)	AVDD*0.360 (+0.0 dB)	1.00
-1 (111)	AVDD*0.336 (-0.6 dB)	0.94

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-2 (110)	AVDD*0.310 (-1.3 dB)	0.87
-3 (101)	AVDD*0.286 (-2.0 dB)	0.80
-4 (100)	AVDD*0.267 (-2.6 dB)	0.74

Table 87 Output Swing Control Table

12.4.3.2 Output Gain Trimming

I/Q channels can also be trimmed separately to compensate gain mismatch in the base-band transmitter or the whole transmission path including RF module. The gain trimming is adjusted in 16 steps spread from -0.96dB to +0.84dB (**Table 88**), compared to the full-scale range set by GAIN[2:0].

TRIMI [3:0] / TRIMQ [3:0]	Gain Step (dB)
+7 (0111)	0.84
+6 (0110)	0.72
+5 (0101)	0.60
+4 (0100)	0.48
+3 (0011)	0.36
+2 (0010)	0.24
+1 (0001)	0.12
+0 (0000)	0.00
-1 (1111)	-0.12
-2 (1110)	-0.24
-3 (1101)	-0.36
-4 (1100)	-0.48
-5 (1011)	-0.60
-6 (1010)	-0.72
-7 (1001)	-0.84
-8 (1000)	-0.96

Table 88 Gain Trimming Control Table

12.4.3.3 Output Common-Mode Voltage

The output common-mode voltage is controlled by CMV [2:0] with about 0.08*AVDD step, as listed in the following table.

CMV [2:0]	Common-Mode Voltage

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+3 (011)	AVDD*0.62
+2 (010)	AVDD*0.58
+1 (001)	AVDD*0.54
+0 (000)	AVDD*0.50
-1 (111)	AVDD*0.46
-2 (110)	AVDD*0.42
-3 (101)	AVDD*0.38
-4 (100)	AVDD*0.34

Table 89 Output Common-Mode Voltage Control Table

12.4.3.4 Programmable Biasing Current

The transmitter features providing 4-bit 9-level programmable current to bias internal analog blocks.

12.4.3.5 Smoothing Filter Characteristic

The 3rd–order Butterworth smoothing filter is used to suppress the image at DAC output: it provides more than 40dB attenuation at the 4.433MHz sampling frequency. To tackle with the digital process component variation, programmable cutoff frequency control bits CALRCSEL [2:0] are included. User can directly change the filter cut-off frequency by different CALRCSEL value (coded with 2's complement format and with a default value 0). In addition, an internal calibration process is provided, by setting START CALRC to high and CALRCCNT to an appropriate value (default is 11). After the calibration process, the filter cut-off frequency is calibrated to 350kHz +/- 50 kHz and a new CALRCOUT value is stored in the register. During the calibration process, the output of the cell is high-impedance.

12.4.4 APC-DAC Register Setup

The register used to control the APC DAC is ACIF_APC_CON, which providing 4-bit 9-level programmable current to bias internal analog blocks. The 4-bits registers APC_CALI [3:0] is coded with 2's complement format.

12.4.5 Auxiliary A/D Conversion Register Setup

The register used to control the Aux-ADC is ACIF_AUX_CON0. For this register, which providing 2-bit 4-level programmable current to bias internal analog blocks.

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12.4.6 Voice-band Blocks Register Setup

The registers used to control AMB are ACIF_VOICE_CON0, ACIF_VOICE_CON1, ACIF_VOICE_CON2, and ACIF_VOICE_CON3. For these registers, please refer to chapter "Analog Chip Interface".

12.4.6.1 Reference Circuit

The voice-band blocks include internal bias circuits, a differential voltage reference circuit and a single-end microphone bias circuit. Internal bias current could be calibrated by varying VCALI[4:0] (coded with 2's complement format).

For proper operation, there should be an external 47nF capacitor connected to output pin AU_VCM. The VCM voltage (~1.4V, typical)**.** The following table illustrates typical 0dBm0 voltage when uplink/downlink programmable gains are unity. For other gain setting, 0dBm0 reference level should be scaled accordingly.

Symbol	Parameter	Min	Typical	Max	Unit
$V_{0dBm0,UP}$	0dBm0 Voltage for Uplink Path, Applied Differentially Between Positive and Negative Microphone Input Pins		0.2V		V-rms
$V_{0dBm0,Dn}$	0dBm0 voltage for Downlink Path, Appeared Differentially Between Positive and Negative Power Amplifier Output Pins		0.6V		V-rms

Table 90 0dBm0 reference level for unity uplink/downlink gain

The microphone bias circuit generates a single-ended output voltage on AU_MICBIAS_P for external electret type microphone. Typical output voltage is 1.9 V. The max current supplied by microphone bias circuit is 2mA.

12.4.6.2 Uplink Path

Uplink path of voice-band blocks includes an uplink programmable gain amplifier and a sigma-delta modulator.

12.4.6.2.1 Uplink Programmable Gain Amplifier

Input to the PGA is a multiplexer controlled by VCFG [3:0], as described in the following table. In normal operation, only AC coupling is suggested if amplification of input signal is desired

Control Signal	Function	Descriptions
VCFG[0]	Input Selector	0: Input 0 (From AU_VIN0_P / AU_VIN0_N) selected 1: Input 1 (From AU_VIN1_P / AU_VIN1_N) selected

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VCFG[1]	Input Selector	1: Input FM (From AU_FMINL / AU_FMINR) Is Selected
VCFG[2]	Coupling Mode	0: AC Coupling (for testing purpose) 1: DC Coupling
VCFG[3]	Gain Mode	0: Amplification Mode (gain range -20~43 dB) 1: Bypass Mode

Table 91 Uplink PGA input configuration setting

The PGA itself provides programmable gain (through VUPG[5:0]) with step of 1.0 dB, as listed in the following table.

VUPG [5:0]	Gain	VUPG [5:0]	Gain
111111	43 dB	011111	11dB
111110	42 dB	011110	10dB
111101	41 dB	011101	9dB
111100	40 dB	011100	8dB
111011	39 dB	011011	7dB
111010	38 dB	011010	6dB
111001	37 dB	011001	5dB
111000	36 dB	011000	4dB
110111	35 dB	010111	3dB
110110	34 dB	010110	2dB
110101	33 dB	010101	1dB
110100	32 dB	010100	0dB
110011	31 dB	010011	-1dB
110010	30 dB	010010	-2dB
110001	29 dB	010001	-3dB
110000	28 dB	010000	-4dB
101111	27 dB	001111	-5dB
101110	26 dB	001110	-6dB
101101	25 dB	001101	-7dB
101100	24 dB	001100	-8dB
101011	23 dB	001011	-9dB
101010	22 dB	001010	-10dB
101001	21 dB	001001	-11dB
101000	20dB	001000	-12dB
100111	19 dB	000111	-13dB

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100110	18 dB	000110	-14dB
100101	17 dB	000101	-15dB
100100	16 dB	000100	-16dB
100011	15 dB	000011	-17dB
100010	14 dB	000010	-18dB
100001	13 dB	000001	-19dB
100000	12dB	000000	-20 dB

Table 92 Uplink PGA gain setting (VUPG[5:0])

The following table illustrates typically the 0dBm0 voltage applied at the microphone inputs, differentially, for several gain settings.

VCFG [3] ='0'		VCFG [3] ='1' (only valid for input 1)	
VUPG [5:0]	0dBm0 (V-rms)	VUPG [5:0]	0dBm0 (V-rms)
111100	2mV	XXXXXX	0.2V
101000	20mV		
100000	50mV		
010100	0.2V		

Table 93 0dBm0 voltage at microphone input pins

12.4.6.2.2 Sigma-Delta Modulator

Analog-to-digital conversion in uplink path is made with a second-order sigma-delta modulator (SDM) whose sampling rate is 6500KHz. Output signals are coded in either one-bit or RSD format, optionally controlled by VRSDON register.

For test purpose, one can set VADCINMODE to HI to form a look-back path from downlink DAC output to SDM input. The default value of VADCINMODE is zero.

12.4.6.3 Downlink Path

Downlink path of voice-band blocks includes a digital to analog converter (DAC) and two programmable output power amplifiers.

12.4.6.3.1 Digital to Analog Converter

The DAC converts input bit-stream to analog signal by sampling rate of 4096kHz. . Besides, it performs a 2nd-order 40kHz butterworth filtering. The DAC receives input signals from DSP by set VDACINMODE = 0. It can also take inputs from SDM output by setting VDACINMODE = 1.

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12.4.6.3.2 Downlink Programmable Power Amplifier

Voice-band analog blocks include two identical output power amplifiers with programmable gain. Amplifier 0 and amplifier 1 can be configured to either differential or single-ended mode by adjusting VDSEND[0] and VDSEND[1], respectively. In single-ended mode, when VDSEND[0] =1, output signal is present at AU_VOUT0_P pin respect to ground. Same as VDSEND[1] for AU_VOUT1_P pin.

For the amplifier itself, programmable gain setting is described in the following table.

VDPG0[3:0] / VDPG1[3:0]	Gain
1111	8dB
1110	6dB
1101	4dB
1100	2dB
1011	0dB
1010	-2dB
1001	-4dB
1000	-6dB
0111	-8dB
0110	-10dB
0101	-12dB
0100	-14dB
0011	-16dB
0010	-18dB
0001	-20dB
0000	-22dB

Table 94 Downlink power amplifier gain setting

Control signal VFLOAT, when set to ‘HI’, is used to make output nodes totally floating in power down mode. If VFLOAT is set to ‘LOW” in power down mode, there will be a resistor of 50k ohm (typical) between AU_VOUT0_P and AU_VOUT0_N, as well as between AU_VOUT0_P and AU_VOUT0_N.

The amplifiers deliver signal power to drive external earphone. The minimum resistive load is 28 ohm and the upper limit of the output current is 50mA. On the basis that 3.14dBm0 digital input signal into downlink path produces DAC output differential voltage of 0.87V-rms (typical), the following table illustrates the power amplifier output signal level (in V-rms) and signal power for an external 32 ohm

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resistive load.

VDPG[3:0]	Output Signal Level (V-rms)	Output Signal Power (mW / dBm)
0010	0.11	0.37/-4.3
0110	0.27	2.28/3.6
1010	0.69	14.8/11.7
1110	1.74	94.6/19.8

Table 95 Output signal level/power for 3.14dBm0 input. External resistive load = 32 ohm

The following table illustrates the output signal level and power for different resistive load when VDPG =1110.

RLOAD	Output Signal Level (V-rms)	Output Signal Power (mW / dBm)
30	1.74	101/20
100	1.74	30.3/14.8
600	1.74	5/7

Table 96 Output signal level/power for 3.14dBm0 input, VDPG =1110

12.4.6.4 Power Down Control

Each block inside audio mixed-signal blocks features dedicated power-down control, as illustrated in the following table.

Control Signal	Descriptions
VBIAS_PWDB	Power Down Reference Circuits (Active Low)
VLNA_PWDB	Power Down Uplink PGA (Active Low)
VADC_PWDB	Power Down Uplink SDM (Active Low)
VDAC_PWDB	Power Down DAC (Active Low)
VOUT0_PWDB	Power Down Downlink Power Amp 0 (Active Low)
VOUT1_PWDB	Power Down Downlink Power Amp 1 (Active Low)

Table 97 Voice-band blocks power down control

12.4.7 Audio-band Blocks Register Setup

The registers used to control audio blocks are ACIF_AUDIO_CON0, ACIF_AUDIO_CON1, ACIF_AUDIO_CON2 and ACIF_AUDIO_CON3. For these registers, please refer to chapter “Analog

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Chip Interface”

12.4.7.1 Output Gain Control

Audio blocks include stereo audio DACs and programmable output power amplifiers. The DACs convert input bit-stream to analog signal by sampling rate of Fs*128 where Fs could be 32kHz, 44.1kHz, or 48kHz. Besides, it performs a 2nd-order butterworth filtering. The two identical output power amplifiers with programmable gain are designed to driving external AC-coupled single-end speaker. The minimum resistor load is 16 ohm and the maximum driving current is 50mA. The programmable gain setting, controlled by APGR[3:0] and APGL[3:0], is the same as that of the voice-band amplifiers.

Unlike voice signals, 0dBFS defines the full-scale audio signals amplitude. Based on bandgap reference voltage again, the following table illustrates the power amplifier output signal level (in V-rms) and signal power for an external 16 ohm resistive load.

APGR[3:0]/ APGL[3:0]	Output Signal Level (V-rms)	Output Signal Power (mW / dBm)
0010	0.055	0.19/-7.2
0110	0.135	1.14/0.6
1010	0.345	7.44/8.7
1110	0.87	47.3/16.7

Table 98 Output signal level/power for 0dBFS input. External resistive load = 16 ohm

12.4.7.2 Mute Function and Power Down Control

By setting AMUTER (AMUTEL) to high, right (left) channel output will be muted.

Each block inside audio mixed-signal blocks features dedicated power-down control, as illustrated in the following table.

Control Signal	Descriptions
ABIAS_PWDB	Power Down Reference Circuits (Active Low)
ADACL_PWDB	Power Down L-Channel DAC (Active Low)
ADACR_PWDB	Power Down R-Channel DAC (Active Low)
AOUTL_PWDB	Power Down L-Channel Audio Amplifier (Active Low)
AOUTR_PWDB	Power Down R-Channel Audio Amplifier (Active Low)

Table 99 Audio-band blocks power down control

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12.4.8 Multiplexers for Audio and Voice Amplifiers

- The audio/voice amplifiers feature accepting signals from various signal sources including AU_FMINR/AU_FMINL pins, that aimed to receive stereo AM/FM signal from external radio chip:

1) Voice-band amplifier 0 accepts signals from voice DAC output only.
2) Voice-band amplifier 1 accepts signal from either voice DAC, audio DAC, or AM/FM radio input pins (controlled by register VBUF1SEL[]). For the last two cases, left and right channel signals will be summed together to form a mono signal first.
3) Audio left/right channel amplifiers receive signals from either voice DAC, audio DAC, or AM/FM radio input pins (controlled by registers ABUFSELL[2:0] and ABUFSELR[2:0]), too. Left and right channel amplifiers will produce identical output waveforms when receiving mono signals from voice DAC.

12.4.9 Preferred Microphone and Earphone Connections

In this section, preferred microphone and earphone connections are discussed.

Differential connection of microphone is shown below. This is the application circuits compatible with previous products. C1 and Rin form an AC coupling and high-pass network. C1*Rin should be chosen such that the in-band signal will not be attenuated too much. For differential minimum resistance of 13k ohm, minimum value of C1 is 170nF for less than 1dB attenuation at 300Hz. R2 is determined by microphone sensitivity. C2 and R2 form another low-pass filter to filtering noise coming from microphone bias pins. Pole frequency less than 50Hz is recommended.

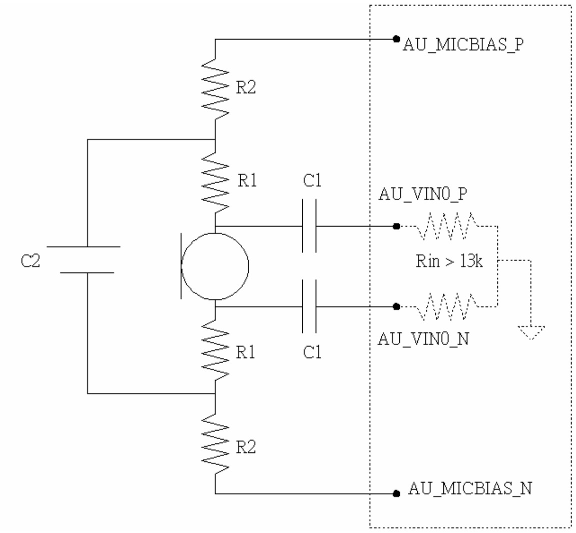

Figure 113 Differential Microphone Connection

Another suggested connection method of microphone is shown below. R1 is chosen based on

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microphone sensitivity requirement. C1 and Rin form an AC coupling and high-pass network. R2 needs proper adjustment to obtain the best noise performance on the voice uplink input terminals.

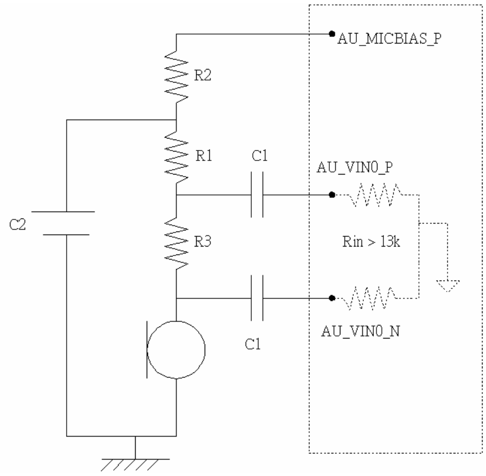

Figure 114 Single-ended Microphone Connection

For earphone, both connections can be used. The application circuit shown in **Figure 114** is highly recommended to achieve the better performance.

12.4.10 Clock Squarer Register Setup

The register used to control clock squarer is CLKSQ_CON. For this register, please refer to chapter "Clocks".

12.4.11 Phase-Locked Loop Register Setup

For registers control the PLL, please refer to chapter "Clocks" and "Software Power Down Control"

12.4.11.1 Frequency Setup

The DSP/MCU PLL itself could be programmable to output either 52MHz or 104MHz clocks. Accompanied with additional digital dividers, 13/26/39/52/65/78/104 MHz clock outputs are supported.

12.4.11.2 Programmable Biasing Current

The PLLs feature providing 5-bit 32-level programmable current to bias internal analog blocks. The 5-bits registers CALI [4:0] is coded with 2's complement format.

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12.4.12 32-khz Crystal Oscillator Register Setup

For registers that control the oscillator, please refer to chapter “Real Time Clock” and “Software Power Down Control”.

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